LOW-VOLTAGE LOW-POWER BULK DRIVEN LOGIC GATES

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Abstract: To realize any combinational and sequential circuit either synchronous or asynchronous gates are the essential components .Low power, low voltage circuits are increasing in demand. In this work various logic gates are implemented using bulk driven technology and there performance are discussed here with corresponding to power. Finally a comparison with the conventional gates has been presented. The performance of the circuit is verified by Cadence Tool, using a standard 0.18 µm CMOS process . The circuits demonstrates low power dissipation .
Keywords: bulk driven, CMOS, Low power, Vdd

1 INTRODUCTION

The increasing demand for efficient portable electronic equipment has pushed the industry to produce circuit designs with very low power consumption.The general trend followed is the lowering of the supply voltage and scaling down of the device geometry to make the device faster with minimal power consumption [1]. The main obstacle in the supply reduction of circuits is the threshold voltage. Bulk-driven (BD), sub-threshold operation, floating gate (FG) and quasi-FG (QFG) are some of the widely used techniques to overcome the threshold voltage limitation [2].

Among the above stated approaches, this paper focuses on the BD mechanism. It not only requires low supply voltage, but the desired performance is achieved without requiring extra circuitry which saves chip area as well as cost. The threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available nowadays. The MOS transistor is a four terminal device; it is mostly used as a three terminal device since the bulk terminal is tied either to the source terminal otherwise to the drain terminal, to VSS or to VDD. A good solution to overcome the threshold voltage is to use the Bulk-driven principle [3]. The principle of the Bulk-driven is that; the gate-source voltage is set to a value sufficient to create an inversion layer. An input signal is applied to the bulk terminal of the MOSFET. In this way, the threshold voltage can be either reduced or removed from the signal path. The operation of the Bulk-driven MOS transistor is much like a JFET i.e. a depletion type device, it can work under negative, zero, or even slightly positive biasing condition. The main advantage of the bulk-driven MOSFET over a Conventional MOSFET is that the threshold voltage requirements are removed .

1.1 Brief Description of Bulk driven Approach

For a conventional gate-driven MOS transistor, we have to overcome the threshold voltage Vth to let it operate. As the feature size of modern CMOS processes scaling down, the maximum allowable power supply continuously decreases, but the threshold voltage does not scale down with the same rate. The bulk-driven technique, which uses bulk terminal as signal input, is a promising method as it achieves enhanced performance without having to modify the existing structure of MOSFET.For a traditional MOSFET, it is mandatory to meet the requirement of VGS > Vth in order to make the MOSFET function in the triode or saturation region. In contrast, the bulk-driven technique allows even smaller voltage to be set at the input terminal but still generate saturation

voltage at the output. Bulk node gives the designer an extra degree of freedom

1.2 Proposed Bulk driven Gates

All the proposed gates are implemented using the bulk driven technology The bulk-driven technique may remove the limitation of threshold voltage effectively by controlling weak positive bias between bulk and source of transistors, thereby reducing the total supply voltage of circuits. Furthermore, it is completely compatible with the standard CMOS process. Hence, the bulk-driven technique is attracting more and more attention as an important method for low-voltage low-power design.

Bulk Driven CMOS inverter :(BD-CMOS)

When Vin is high and equal to low supply voltage VDD and Vbn (i.e. 0.4V), the BD-NMOS transistor is on, while the BD-PMOS is off. A direct path exists between Vout and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V) and the bulk of PMOS connect with the ground, BD-NMOS and BD-PMOS transistors are off and on, respectively. A path exists between VDD and Vout, yielding a high output voltage. The gate clearly functions as an inverter.

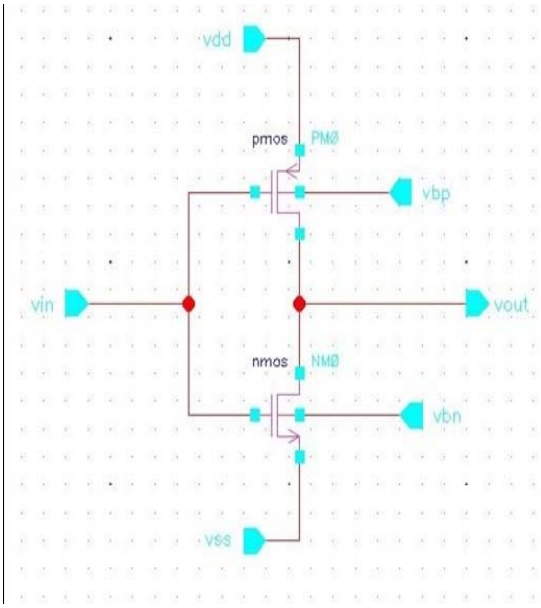

Fig 1 BD-CMOS Inverter

The output waveform shown in Fig 2 shows the correctness of the output of BD Inverter gate.

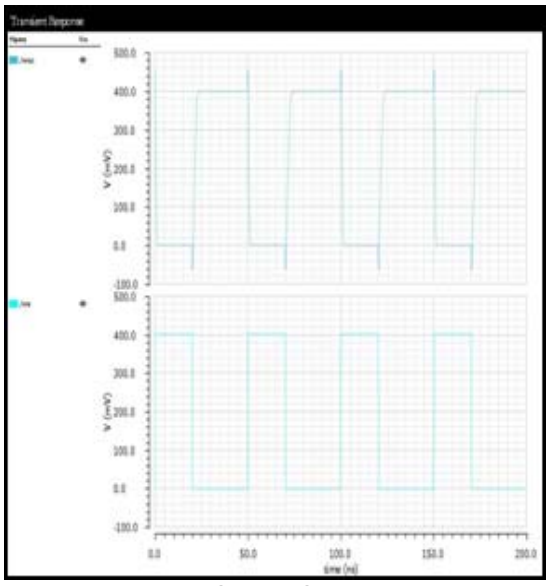

Fig 2 Waveform of BD INVERTER

Bulk Driven NAND gate:

In this we use two complementary pairs of BD-CMOS inverter, one for each of the inputs A and B, and create the NMOS and PMOS arrays according to the needed outputs. In this slightly positive supply connects with bulk of NMOSFETS and the bulk of PMOSFETS connect with the ground. There is only a single case where the output is 0. This occurs when both inputs are at logic 1 values i.e. A=B=VDD, since BD-NMOSFETS connect the output node to ground. If either input is low , then Vout=VDD indicating that the output node must be connected to the power supply. In these cases we use two BD-PMOSFETS in parallel.

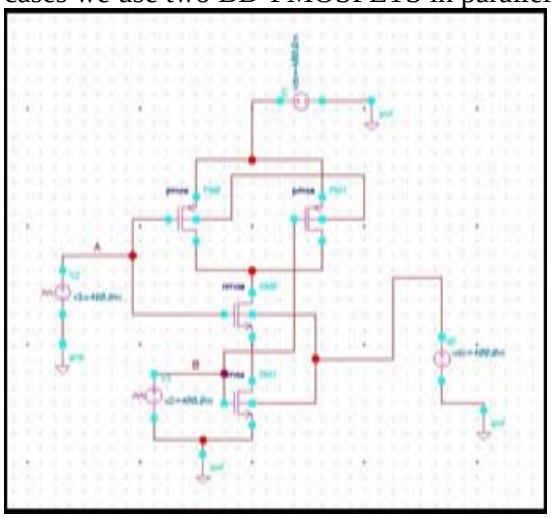

Fig 3 BD-NAND gate

The output waveform shown in Fig 4 shows the correctness of the output of BD NAND gate.

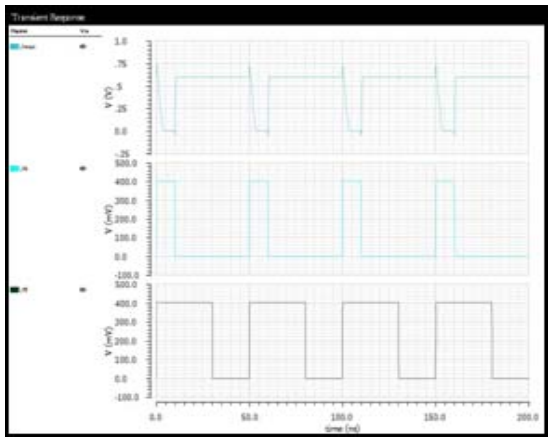

Fig 4 Waveform of BD NAND gate

Bulk Driven NOR gate:

In this we use two complementary pairs of BD-CMOS inverter, one for each of the inputs A and B, and create the NMOS and PMOS arrays according to the needed outputs. In this slightly positive supply connect with bulk of NMOSFETS and the bulk of PMOSFETS connect with the ground. When either one or both inputs are high i.e. when the BD-NMOS network creates a conducting path between the output node and ground, the BD-PMOS network is cut-off. If both input is low i.e. when the BD-NMOS network is cut-off, the BD-PMOS network creates a conducting path between the output node and power supply voltage VDD.

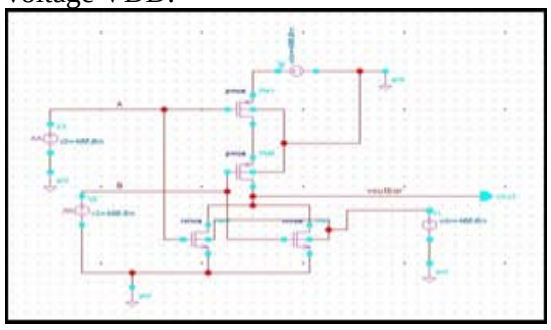

Fig 5 BD-NOR gate

The output waveform shown in Fig 6 shows the correctness of the output of BD NOR gate

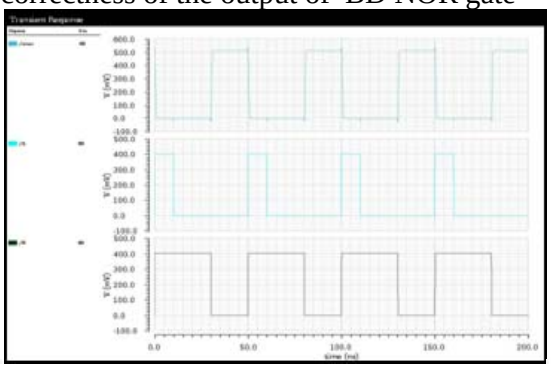

Fig 6 Waveform of BD NOR gate

Bulk Driven AND gate:

In this we use two complementary pairs of BD-CMOS inverter, one for each of the inputs A and B, and create the NMOS and PMOS arrays according to the needed outputs. In this slightly positive supply connects with bulk of NMOSFETS and the bulk of PMOSFETS connect with the ground. There is only a single case where the output is 1. This occurs when both inputs are at logic 1 values i.e. A=B=VDD, since BD-NMOSFETS connect the output node to ground and BD-CMOS inverter at the output invert the output voltage.. If either input is low , then Vout=0 indicating that the output node must be connected to the power supply and BD-CMOS inverter at the output invert the output voltage. In these cases we use two BD-PMOSFETS in paralle

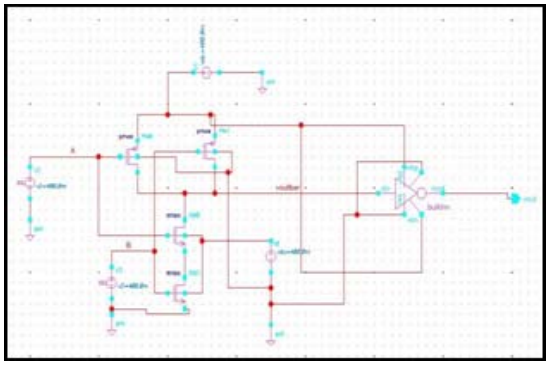

Fig 7 BD-AND gate

The output waveform shown in Fig 8 shows the correctness of the output of BD AND gate

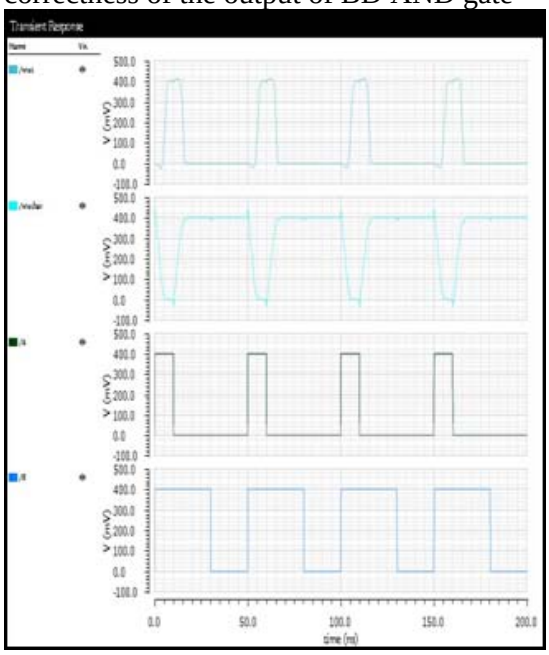

Fig 8 Wave form BD AND gate

Bulk Driven OR gate:

In this we use two complementary pairs of BD-CMOS inverter, one for each of the inputs A and B, and create the NMOS and PMOS arrays according to the needed outputs. In this slightly positive supply connect with bulk of NMOSFETS and the bulk of PMOSFETS connect with the ground. When either one or both inputs are high i.e. when the BD-NMOS network creates a conducting path between the output node and ground, the BD-PMOS network is cut-off and BD-CMOS inverter at the output node invert the voltage of the output node. If both input is low i.e. when the BD-NMOS network is cut-off, the BD-PMOS network creates a conducting path between the output node and power supply voltage VDD and BD-CMOS inverter at the output node invert the voltage of the output node.

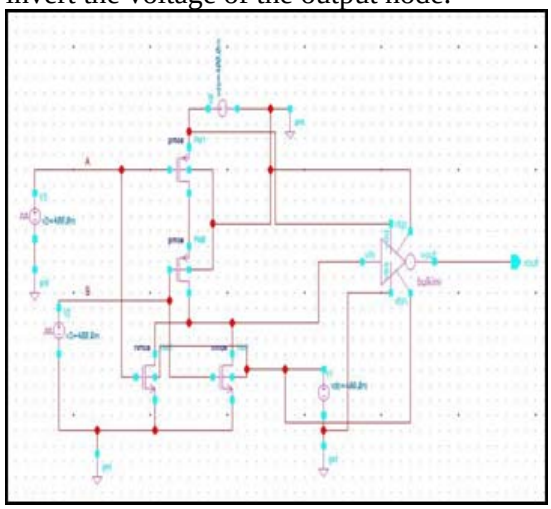

Fig 9 BD-OR gate

The output waveform shown in Fig 10 shows the correctness of the output of BD OR gate

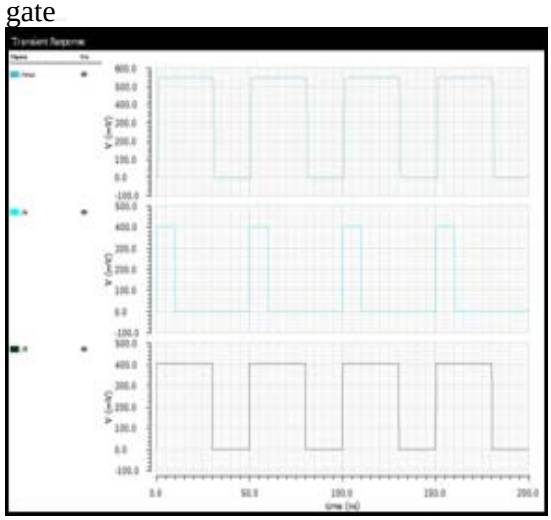

Fig 10 Waveform of BD OR gate

BD XOR gate:

XOR gate is known as non-equivalance checker because when the input A and B are not different or equivalent then the output is high. To realize XOR gate in BD-CMOS we have to realize the function f = AxorB = A'B+AB' as BD-CMOS logic always generate inverted logic.

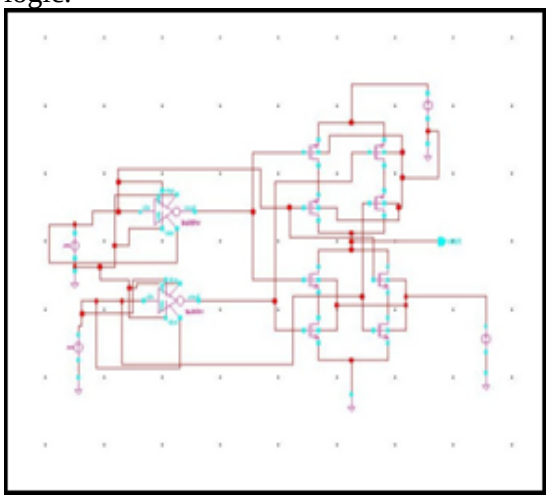

Fig 11 BD XOR gate

The output waveform shown in Fig 12 shows the correctness of the output of BD XOR gtae.

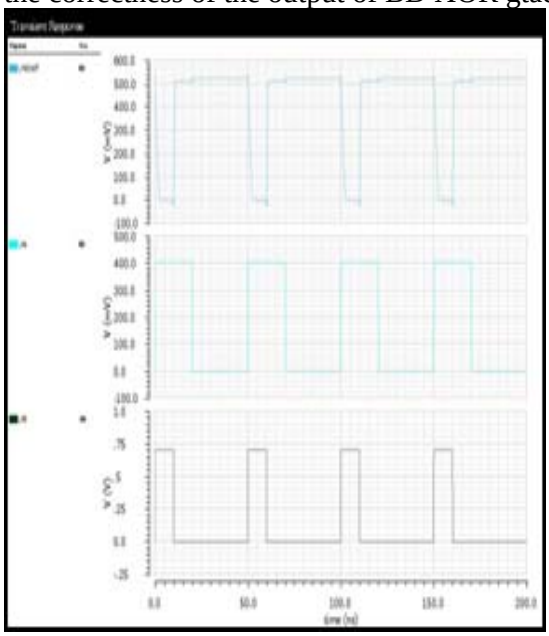

Fig 12 Waveform of BD XOR gate

II. SIMULATION RESULTS AND ANALYSIS

The above proposed bulk driven gates was simulated in 180 nm CMOS process using Cadence Tool. The output waveform shown for all the discussed gated shows the correctness of the bulk driven gates and the parameter , power of bulk driven and conventional gates are obtained and compared for the input frequency 50 ns and pulse width 20 ns are listed in table 1.

Table1 : Power comparison of various logic gates

	Gates	Supply (V)	I/P (V)	Vbn (V)	Vbp (V)	Power (nW)
Conventional	Inverter	0.8	0.8	-	-	117.9
	AND	0.6	0.6	-	-	196.2
	OR	0.6	0.6	-	-	193.3
	NAND	0.6	0.6	-	-	99.92
	NOR	0.6	0.6	-	-	95.4
	EX-OR	0.6	0.6	-	-	398.1
Bulk driven	Inverter	0.4	0.4	0.4	0.4	34.51
	AND	0.4	0.4	0.4	0.4	138.1
	OR	0.4	0.4	0.4	0.4	131.3
	NAND	0.4	0.4	0.4	0.4	46.51
	NOR	0.4	0.4	0.4	0.4	94.56
	EX-OR	0.4	0.4	0.4	0.4	182.4

III Conclusion: It is observed that the conventional gates do not work less then the applied voltages where as the bulk driven gates work on the voltages which is less then the conventional voltages of logic gates and the power consumption is also less without any additional circuitry .So these gates can be used where there is requirement of low voltage and less power consumption with no compromise in the output performance .

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