3T XOR GATE DESIGN USING IDDG MOSFET

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Abstract— This paper presents a new design of 3 transistor XOR by using Double Gate MOSFET. Proposed gate has been designed using Independent Driven Double Gate and compared with 3T XOR implemented using Symmetrical Driven Double Gate in sub threshold region. The simulation and comparison analysis results in to low power consumption of the proposed design with various performance parameters. The entire simulation has been carried out on EDA tool at 45nm process technology.

Index Terms—3T XOR, IDDG, MOSFET, SDDG

I. INTRODUCTION

In 1965 Gordon Moore [1] predicted that the number of transistors per chip mould be just doubled in approximately two years. When channel length of the device shrinks, the close proximity between Drain to Source reduce the ability of the Gate electrode to control the potential distribution and flow of current in the channel. So, conventional bulk MOSFET cannot be scaled down at lower nanometer technologies to achieve low power systems.

The Double Gate MOSFET is electrostatically superior to a Single Gate MOSFET because two gates are used to control the channel from both sides. The two gates together control roughly twice as much current as a single gate [2]. The current driving capability of Double Gate MOSFET is twice that of planner CMOS and hence Double Gate MOSFET can be operated at much lower input and threshold voltage [3]. Depending upon the way that gate voltage are applied, Double Gate MOSFET may be categorized as 2 types: A Double Gate MOSFET is said to be symmetric when both gates have the same work function and a single input voltage is applied to both gates, otherwise it is called Asymmetric Double Gate MOSFET [4].

As MOS integrated circuit technology has evolved to exploit smaller device structures, it has become progressively more important in recent years to look more closely at the minority carriers present under the gate when the gate voltage is less than threshold voltage, i.e. in what is called the “Sub-threshold” region [5]. These carriers cannot be totally neglected, and play an important role in device and circuit performance. It is recognized that they also enable a very useful mode of MOSFET operation, and that the sub-threshold region of operation is an important as the traditional cut-off, linear and saturation region of operation. XOR gate is basic building block of digital circuits like 1-bit Full-Adder, Subtractor, and Multiplier [6]. The new proposed 3T XOR Gate with IDDG MOSFET fulfill the demand of sub threshold operation at various operating conditions. To construct Double Gate, two single gate MOSFET Transistors have been connected in parallel in such a way their Source and Drain are connected together [7].

The paper ordered as follows: Basic introduction about Double Gate MOSFET is including in session I. Session II illustrates the 3T

XOR Gate by using SDDG MOSFET. Session III contain new design of 3T XOR Gate driven by Independent Driven Double Gate MOSFET. Session VI show simulations and comparison of SDDG and IDDG MOSFET designs and session V conclude the paper.

II. 3T XOR GATE DESIGN USING SYMMETRICALLY DRIVEN DOUBLE GATE MOSFET

Fig. 1 show the 3T XOR Gate circuit Design using Symmetrically Driven Double Gate MOSFET. This SDDG XOR Gate has been designed as the modified version of single Gate 3T XOR Gate design [8].

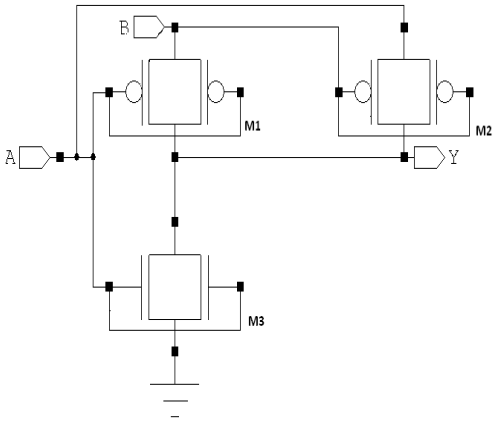

Fig. 1 Schematic of 3T XOR gate using SDDG MOSFET

The operation of SDDG design is like a 2-input XOR Gate. Unlike conventional single gate MOSFET in SDDG design has double control of gate of both n-SDDG MOSFET and p-SDDG MOSFET that leads to enhance the performance in term of I_{on} and I_{off} current. In this circuit minimum sizing is used for n-SDDG MOSFET and p-SDDG MOSFET transistors are taken as 1/1.

III. PROPOSED 3T XOR GATE DESIGN USING INDEPENDENT DRIVEN DOUBLE GATE MOSFET

Fig. 2 shows the schematic of 3T XOR Gate designed using Independent Driven Double Gate MOSFET. This design comprises of two p-types Double Gate MOSFET and one n-type Double Gate MOSFET. As IDDG gives the liberty of biasing the two gates independently therefore taking such benefit in the proposed design, the two gates of M2 transistor has been connected with each other whereas M1 and M3 have different gate biasing.

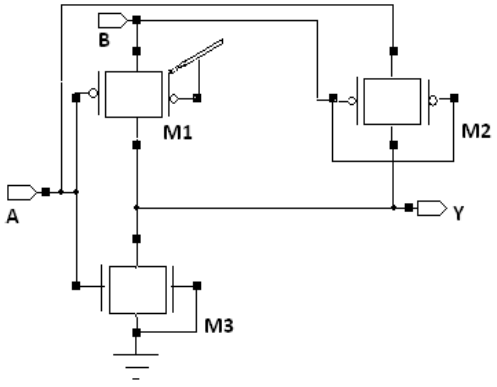

Fig. 2 Schematic of 3T XOR gate using IDDG MOSFET

In the circuit shown in Fig. 2 back gate of M1 is connected to V_{DD} as well as back gate of M3 is connected to Ground unlike in Fig. 1 where all the transistors are connected with varying inputs. Because of these fixed back gates in the proposed design the power consuming transitions will be less which results in to less switching activity and hence less power consumption in compare to its peer designs. The aspect ratio of all the transistors has been chosen (1/1), increasing beyond this increases the power consumption as well as on-chip area with no betterment in threshold loss. Hence, to achieve low power design such aspect ratio i.e.; (1/1) is the best suitable option.

IV. SIMULATIONS AND COMPARISON

Both the circuits have been simulated using EDA tool at 45nm process technology in sub threshold region with same testing conditions.

A. *Variation with Voltage*

For performing sub threshold operation supply voltage is taken less than the threshold voltage. The input voltage variation range is from 0.16V to 0.26V. Comparison is taken at room temperature i.e. 25°C and 100MHz frequency.

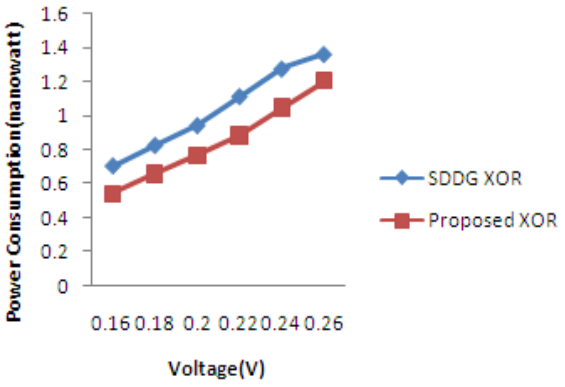

Fig. 3 Power Consumption with increasing Voltage

The graph shown in Fig. 3 illustrates that the power consumption of proposed IDDG 3T XOR is approximately 21% less than the SDDG XOR cell which experimentally supports the text in Section III. Therefore, the proposed XOR cell can be a better option for low power device design.

B. *Variation with frequency*

On increasing the operating frequency power consumption also increases as both the performance parameters are proportional to each other [9], the same has also been supported by the simulation results plotted in the graphical form in Fig.4. For performing sub threshold operation input voltage has been taken 0.2V at room temperature 25°C. Frequency variation range is taken from 100MHz to 350MHz.

In Fig. 4 it is shown that power consumption changes with varying Frequency. Initially at 100 MHz the difference in power consumption of the two designs is less but as the frequency increased this gap also increases significantly. This as a result depicts that the proposed design will be a better option for high frequency applications.

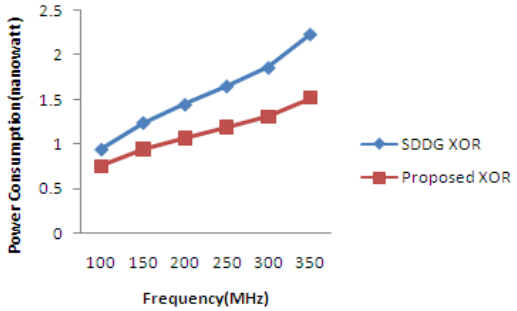

Fig. 4 Power consumption with varying Frequency

C. *Variation with Temperature*

Variations with temperature are compared at constant frequency 100MHz and input voltage 0.2V. Temperature variation range is taken from -10°C to 80°C.

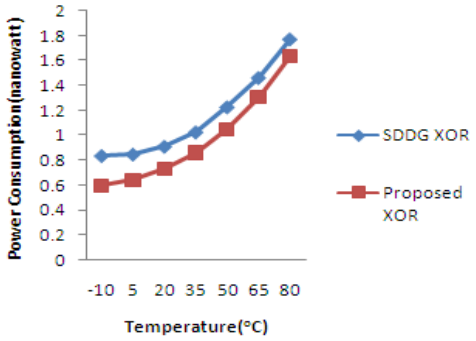

Fig. 5 Power consumption with increasing Temperature

As the simulations have been carried out in sub threshold region i.e.; voltage applied is much less than the threshold voltage of the MOSFETs, therefore, electric field generated is also less. At low electric field current and temperature are proportional with each other. Hence, as a result power consumption increases with increase in temperature [10].

Fig. 5 shows that increase in temperature shrinks the gap between power consumption of

IDDG XOR cell and SDDG XOR cell is but keeping the proposed design at lower scale i.e.; 15% less as compared to SDDG 3T XOR Gate design. Therefore, the proposed XOR cell is more temperature sustainable in comparison to SDDG cell.

V. CONCLUSION

To implement new topologies, conventional MOSFET devices have been replaced with Double Gate MOSFET devices which show improved performance. By simulation results it has been demonstrated that IDDG MOSFET is more promising for future ultra-low power systems in comparison to SDDG MOSFET. Comparison of SDDG XOR gate with proposed IDDG XOR cell show that the XOR designed using IDDG MOSFET outperforms in sub threshold operation. The circuits have been compared at 45nm technology in sub threshold region for various operating conditions. The analysis of the simulated results confirms the practicability of IDDG MOSFET technique in digital circuits design.

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