A CALCULATIVE ANALYSIS OF CHANNEL UTILIZATION USING HIERARCHICAL IP ADDRESSING SCHEME(HIPAS)

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Abstract— Network on Chip (NoC) is one of the best communication architecture that uses efficient characteristics in topology, switching, routing and flow control. Wormhole routing using virtual channel concept has been a popular switching technique in the new generation NoC architectures. Routing process creates logical connection between nodes in a network so that packets sent by node can reach their destination. Moreover there is a problem with selection of best routing path and efficient utilization of channel or link for a network. Larger overhead while routing and transmitting a packet within the network causes decrease in the number of transmitted information bits, which in turn causes to degrade the channel utilization.

We present a mathematical model for the computation of channel utilization using Hierarchical IP Addressing Scheme(HIPAS) for NoC applications and a routing strategy to avoid the randomness in the selection of path. The HIPAS provides that the overhead bits can be minimised in the packet and users can be facilitated to transmit more number of true information bits to the destination. The mathematical model shows that how the overall utilization of channel increases using this scheme.

Keywords: NoC, Wormhole Routing, HIPAS, Channel utilization.

I. INTRODUCTION

Design of the chip design has four distinct aspects: computation, memory, communication, and I/O. As processing power has increased and data intensive applications have emerged, the challenge of the communication aspect in single-chip systems, Systems-on-Chip (SoC), has attracted increasing attention. The architecture of NoC enables the topology to be configured based on the application currently running on the chip. The reconfigurable NoC architecture is evaluated in [8], which shows a huge decrease in power consumption to static mesh topology. This survey treats a prominent concept for communication in SoC known as Network-on-Chip (NoC). Users, system designers and researchers are often interested in knowing the expected performance of system. From user perspective this is often phrased as either "which system will get my data there most effectively for my needs?" or "which system will deliver the most data per unit time?" System designer are often interested in selecting the

most effective architecture or designer constraints for a system, which drive its final performance [4]. And the researchers interest is to always find and propose an efficient architecture for routing.

In most cases the benchmark of what a system is capable of or its maximum performance is what the user or designer is interested in.

Keeping all these points in mind, NoC is proposed as an emerging paradigm for on chip communication networks [4]. NoC does not constitute an explicit new alternative for intra chip communication but is rather a concept which presents a unification of on chip communication solutions [2].

Fig. 1 [2] shows a simple structure as 4x4 mesh which provides global chip level communication. Cores (IP blocks) are used to generate packets or message, which they want to transmit. The purpose of the network adapter (NA) is to interface the core to the network and make communication services transparently available with a minimum of effort from the core. Network adaptor provides interface between a routing node and IP block. Routing nodes represent a router which implements the routing strategy.

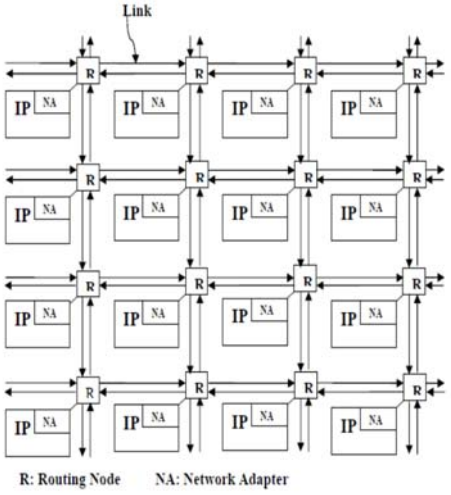


Fig. 1Topological illustration of a 4-by-4 mesh structured NoC

Links connect the routers, providing a physical media to communicate with each other directly[5]. The routers used, are generally wormhole routers with virtual channel concept for flow control. The concept of virtual channel will increase the throughput of network [6].

Addresses can be determined in two ways, either bound with hardware during the manufacturing process or assigned on demand by addressing protocols. Using the various on-demand addressing protocols it can be categorized further into centralized and distributed. The first one employs a central addressing coordinator and the latter one does not respectively. There are currently two types of distributed addressing schemes, flat and hierarchical [7].

• Flat Addressing The majority of MANET routing protocols employ a flat addressing mechanism as the nodes are not static and are in a ad hoc network . In a flat network, addresses are randomly assigned to nodes; therefore, the distribution of addresses is unrelated to the network topology. Although the addressing process is easy, a flat address structure always makes it hard to build a path between two arbitrary nodes.

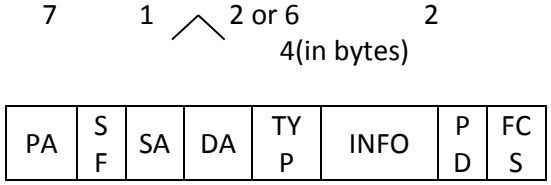
• Hierarchical Addressing A hierarchical addressing scheme can make the path discovery process easier due to its systematic structure. The distribution of hierarchical addresses also does not need a central coordinator; however, it causes the waste of address resources if the network grows irregularly. The ZigBee tree structure is such an example that is commonly used in WSNs. In addition, networks do not reserve addresses for the nodes roaming out of range. This feature of hierarchical addressing makes it more adaptable for the static networks rather than for mobile networks.

The HIPAS for NoC applications will facilitate a user to transmit more messages with lesser overhead bits to other users [1]. In this HIPAS, the IP connected to router is assigned a global address in such a way that a global address of two directly connected IP's must have only single bit difference. And so, the number of bit changes in the global address of two IPs will indicate the distance between them. The number of overhead bits required will be dependent on this distance.

Further, we propose a calculative model for computation of overall channel utilization along with a new factor called channel utility factor. Variation of the overall channel utilization with respect to distance and processing delay is also been observed.

II. HIERARCHICAL IP ADDRESSING SCHEME

In computer networks, the messages are transmitted in forms of packets or frames. The number of bits in a packet are given as $N_b=N/P$, where N are the total number of bits in a message and P are the number of packets in the message. Every packet (whether it belongs to any set of protocol), belongs to any source and destination pair, carries some overhead (N_a+N_o) (including Source address and Destination address and other pre information and post information bits). As example Ethernet packet frame has the structure given in Fig.2 [1].



PA:Preamble SF:Start Frame
SA:Source Address
DA:Destination Address TYP:Type
INFO:Information
PD:Pad

Fig. 2 Ethernet Frame

Now the packet that has to travel over the link consists of $N_p=N_a+N_o+N_b$.

While using HIPAS every IP connected to routers in NoC (mesh topology) is assigned a global address in such a way that the global addresses of two directly connected IP's must have only single bit difference as shown in fig.3 for 16 IP's with internal port address of 4 bit.

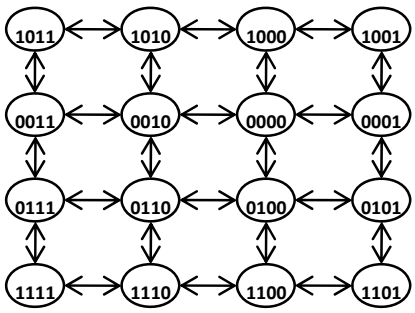


Fig.3 An example of Hierarchical IP Addressing Scheme

This property of HIPAS gives the efficient performance while transmitting the packets from one user to another. Fig.4 shows the Basic mechanism of HIPAS for transmission of packets from one IP to other IP, in a network [1]. Now when IP sends its packets to router, it will contain source address, destination address and some other constants (as shown in fig.2). The router will extract the source and destination address from the packet and with the help of look up table it will decide the complete path from source to destination by using travelling address (TA). If b is the number of bits required to resolve the internal port address of a single router, then to address the complete path having distance d with n=d+1 number of router in the path is given as TA= (d+1)*b. At destination port destination router will find the global address of source IP by reversely traversing the travelling address in look up tables. By doing so we can transmit more number of message bits in packets, as wormhole routing header flit contain only Travelling address not Source global address and Destination global address [1].

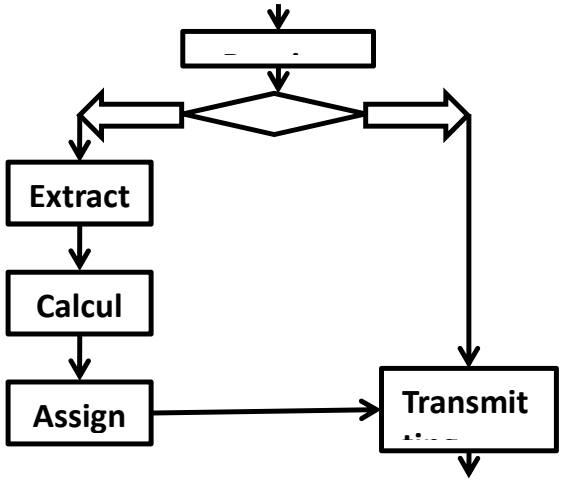


Fig.4 Basic mechanism of HIPAS

III. MATHEMATICAL MODEL

In this model, packets are generated with source and destination address, and are transferred from one router to another towards their destination [3]. The routers are capable of taking decision in selection of path .Now the channel utility factor which measures the amount of true information transferred over the link of capacity C bits/sec is given as-

Channel utility factor, $U_{cuf} = \frac{N_b}{N_p}$

$= \frac{[N_p - (N_a + N_o)]}{N_p}$

Using HIPAS N_a is replaced by travelling address (TA) for (d+1) routers having internal port address b, which is given as

$$TA = (d+1)\, b$$

So, $U_{cuf} = 1 - \frac{(N_a + N_o)}{N_p}$

$= 1 - \frac{(d+1)b + N_o}{N_p}$

Now, Overall channel utilization of a channel or link for any network can be given as the function of

1. Useful data transmission time

   $T = \frac{\text{Useful data transmitted}}{\text{Utilized channel capacity}} = \frac{N_b}{CC^u}$

2. Delay overhead, suppose it is Y.
3. Activity factor

   $\eta = \frac{x}{Z} = \frac{\text{count of all active IPs}}{\text{count of all IPs}}$

   where x is the count of all active stations.

Combining all these overall channel utilization, U_{ocu} given as-

$$U_{ocu} = \frac{xT}{xT+Y}$$

Considering the processing delay at each router equal to α, which is the time taken in receiving the packet flit, decoding the address information and transmitting it further. Also considering that packet is passed sequentially in the same logical order as their physical address is, then the net processing delay = (d+1).α. (Where the number of routers between source and destination can be given by n =d+1),

This processing delay will add up to net delay overhead and so the channel utilization will be

$$U_{ocu} = \frac{xT}{xT+Y+(d+1)\alpha}$$

Now, putting the value of T, we have

$$U_{ocu} = \frac{x.\frac{N_m}{C^u}}{x\frac{N_b}{CC^u}+[Y+(d+1)\alpha]}$$

$$= \frac{x.\, N_m}{x.\, N_b + [Y+(d+1)\alpha]CC^u}$$

As the utilized channel capacity (which indicates flow of true information over the channel of capacity C (bits/sec)) given as

$$CC^u = U_{ch} \cdot C$$

Now the U_{ocu} is given as-

$$U_{ocu} = \frac{x.\, N_b}{x.\, N_b + [Y+(d+1)\alpha]C.\frac{N_b}{N_p}}$$

$$U_{ocu} = \frac{x.N_p}{x.N_p + [Y+(d+1)\alpha]C}$$

Put the value of x from activity factor, then-

$$U_{ocu} = \frac{\eta z N_p}{\eta z N_p + [Y+(d+1)\alpha]C}$$

This is the expression for the overall utilization of channel.

IV. CONCLUSIONS

This analysis shows a clear fact that channel can be utilized to its maximum if the activity factor or in turn the numbers of active IPs are more. For the smaller values of activity factor, the overall channel utilization can be achieved for smaller values of processing delay. HIPAS requires less overhead and addressing bits for transmitting the true information. By the addressing scheme used in Fig. 3 we are reducing the mesh topology into a logical Torus topology and that too without using any interconnection. This provides us the torus advantage in a mesh environment. Future work can be emphasized on how to reduce the processing delay at each routing node. Also processing delay will be the function of traffic intensity, so it can be analyzed further.

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