A HIGH SPEED ∑Δ ANALOG TO DIGITAL CONVERTER FOR A GENERAL PURPOSE RF FRONT END IN 90NM-TECHNOLOGY

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Abstract:
In this report a transistor-level design of a GHz ∑Δ analog-to-digital converter for an RF front end is proposed. The design is current driven, where the integration is done directly over two capacitances and it contains no operational amplifiers. The clock frequency used for verification was 2.5 GHZ and the output bandwidth was 10 MHz. The system is flexible in that the number of internal bits can be scaled easily and in this report a three-bit system yielding an SNR of 76.5 dB as well as a four-bit system yielding an SNR of 82.5 dB are analyzed.
Keywords: ADC, Opamp, SNR.

Introduction:
A software defined radio is a communication system that can be used for a wide range of frequency bands and modulation techniques by changing the software that runs on the system but not changing the hardware. An important part in this system is a wide-band analog-to-digital converter (ADC) that produces a digital signal that can be processed by the software. One approach for this ADC is a ∑Δ-design that uses oversampling with a much higher clock frequency than the output frequency in order to reduce the quantization noise of the ADC.

ADC Characterization:
There are several different parameters that are important when analyzing the noise contribution of an analog-to-digital converter.

SNR = Signal-to-noise-ratio describes the relation between the signal power and the noise and is defined as
[SNR = 10 log10(Ps/Pn) (dB)].
SFDR = Spurious-free dynamic range. Harmonics of input frequencies and intermodulation products of two or more input frequencies can cause large unwanted signals at other frequencies. These signals are called spurious signals and the relation between the largest spurious signal and the input signal is called SFDR and is defined as
[SFDR = 10 log10(Ps/Pd,max) (dB)].
SINAD = Signal-to-noise-and distortion describes the relation between the signal power and the power of all other frequencies within the channel, both from noise and spurious signals. SINAD is defined as [SINAD = 10log10(Ps/Pn+d) (dB)].
ENOB = Effective number of bits and stands for the resolution in bits that is possible to achieve after the signal has been digitalized. ENOB is directly related to SINAD since both noise and spurious signals can affect the output. ENOB can be defined as
[ENOB = (SINAD – 1.76)/6.02 (dB)].
When a signal is quantized, an error is introduced. The average of this error is half that of one quantization step and a N-bit quantization leads to an SNR of:
[SNRquantization = 6.02N + 1.76 (dB)].
This noise is spread evenly over the frequency spectrum from 0 to the Nyquist frequency of the sampling frequency, fs/2 . If the signal is sampled at a much higher frequency than the signal frequency and subsequently low-pass

filtered, a large proportion of the noise can be filtered out. The resulting SNR with an oversampling factor of OSR = fs/(2fbw) is :
[SNRoversampling = 6.02N + 1.76 + 10 log10 OSR (dB)]

∑Δ ADCs:

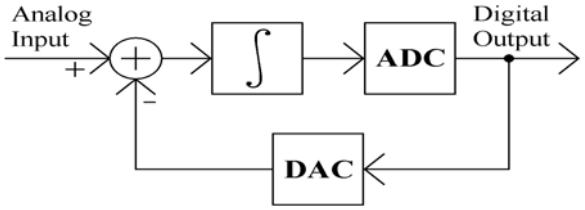

Figure 1. ∑Δ-ADC

The quantization noise of the ADC can be significantly reduced by different types of feedback. In a ∑Δ structure, the output error is integrated and subsequently quantized for the next output. With this structure each output error will affect the subsequent outputs and as a result the average error will be reduced. In a ∑Δ-ADC the total noise in the system is increased compared to the case of non-feedback ADC but the noise is lower at lower frequencies and higher at higher frequencies. With this noise-shaping a larger proportion of the quantization noise can be filtered out in a low-pass filter and with the same OSR result in a higher SNR than in a non-feedback system:
[SNR∑Δ = 6.02N + 1.76 − 5.17 + 30 log10 OSR (dB)].

Harmonics and Intermodulation Products:

Non-linear properties of a system cause distortion to the output signal. These distortions cause unwanted harmonics to appear at integer multiples of the input frequency (2fin, 3fin, 4fin . . .). In a differential system the even-order harmonics of the positive branch and the negative branch of the system will cancel each other out so that only the odd multiples of fin will appear at the output. When two signals are fed through a system at the same time, they and their harmonics will mix with each other causing intermodulation products at the output. The largest of these intermodulation products will appear at f1+f2 and f1−f2 called second-order intermodulation products or ID2. Further intermodulation products will appear at 2f1 − f2 and 2f2 − f1 called third-order intermodulation products, ID3 and to a lesser extent also ID4, ID5 and so on. If two signals with frequencies close together, in the middle of a frequency band are passed through a system, the third-order will also occur within the band. Because of this ID3 can be a big problem and a common way to test a system's linearity is through a two-tone test.

Basic Hardware Design:

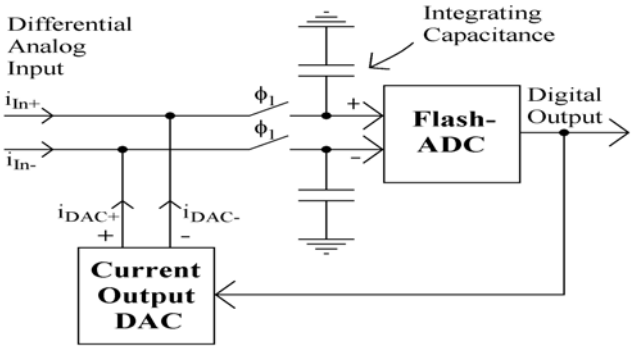

Figure 2. Principle schematic of the proposed design.

The proposed structure is a differential first-order ∑Δ-loop with three or four internal bits. The integration in the loop is done over two capacitances, one for each path of the differential system. The input to the system is two equally large but opposite currents, either from a transconductance amplifier or as a current output from a mixer. The peak currents of these inputs are not allowed to be larger than 1.584 mA differentially, the same as the maximum feedback from the DAC. If the inputs are larger than this the DAC can no longer compensate for the input signals and the voltage levels of the integrating capacitances will grow out of control. The design is made in a 90nm technology and all transistors used in the design are of low threshold voltage type in order to reduce the on-resistance of switches and to improve the allowed output voltage swing of the DAC. The supply voltage, Vdd of the system is 1.2 V. To avoid leak-through from the dump capacitances to the integrating capacitances, non-overlapping clocks,Φ1 and Φ2 have been used.

Integrator and Charge dump:

The integrating part of the loop is done over two capacitances connected to Gnd, one for the positive and one for the negative side of the differential system. The differential voltage of the integrating capacitances will change during positive phase of Φ1 according to:
Δvdiff = ((iIn,diff − iDAC,diff)/Cintegration)*(Tclock/2) V.
During the negative phase of the Φ1 clock, the integrating capacitances are disconnected from the input and from the DAC. If the currents are

not taken care of the voltages of nodes A and B will quickly approach Gnd or Vdd and the nodes would have to be recharged to the voltage levels of the integrating capacitances at the start of each integration phase. This would introduce a noise in the system and different strategies could be employed to minimize this noise:

1. The input and the DAC could be turned off.
2. Since ia = −ib nodes A and B could be short-circuited so the currents would cancel each other out during the negative phase of the Φ1 clock.
3. The currents ia and ib could be fed to dump capacitances of the same size as the integrating capacitances.

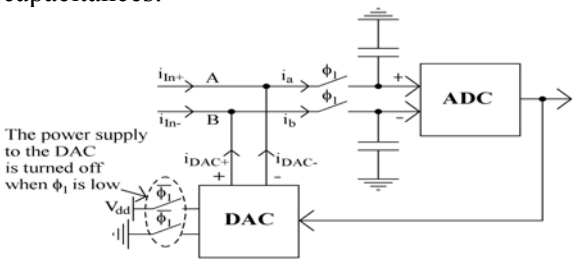

Figure 3. The 1st strategy.

The first strategy has two drawbacks. The first is that for the current sources and current sinks to be turned off, their connections with Vdd and Gnd respectively have to be switched off. This would reduce their allowed voltage swing. The second drawback is that since the transistors at the outputs of the DAC are relatively large, it would take some time for them to be able to deliver their correct output currents after each rising edge of the Φ1 clock. One benefit of this strategy would be that since ia and ib are turned off when they are not needed, no power would be wasted during the negative phase of the Φ1 clock and the overall power consumption and heat generation of the circuit would decrease.

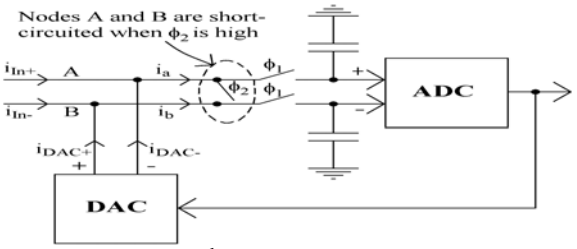

Figure 4. The 2nd Strategy

The second strategy also suffers from a few drawbacks. During the positive phase of the Φ2 clock, a transmission gate would short circuit nodes A and B and the currents ia and ib would cancel each other out. One problem with this strategy is that at every rising edge of the Φ1 clock, the voltage levels of nodes A and B would have to be recharged from Vdd/2 to the voltage levels of the integrating capacitances. Another problem is that the nonzero on-resistance of the short-circuit switch would lead to a difference between the voltage levels of node A and node B equal to ia · Rswitch. Since the switch resistance can be in the order of 50 and the current ia in the order of 0.2 mA the voltage difference could be as large as 10 mV and not negligible compared with the overall maximum voltage swing of 200 mV.

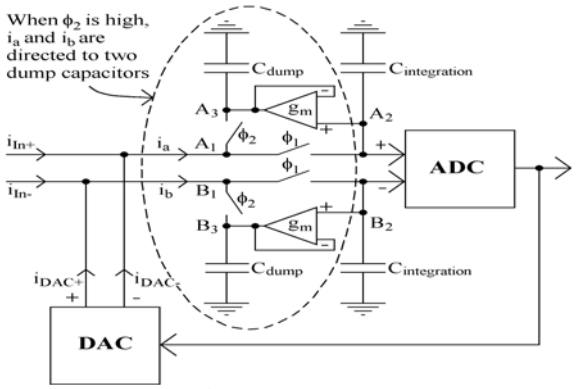

Figure 5. The 3rd strategy.

The third strategy is the one implemented in this design. The currents ia and ib are directed to two dump capacitances during the positive phase of the Φ2 clock. Since ia and ib on average are approximately as large during a positive phase of the Φ1 clock as in the following positive phase of the Φ2 clock, the voltage levels of the dump capacitances (A3 and B3) will trace those of the integrating capacitances (A2 and B2) with only a small error. At a rising edge of the Φ1 clock, the output of the DAC, nodes A1 and B1 will have to be recharged to the voltage levels of A2 and B2. At this time, the voltage levels of nodes A1 and B1 are the same as the voltage levels of A3 and B3 and therefore it is [(vA3−vA2)·CA1]/ Cintegration and[(vB3−vB2)·CB1]/ Cintegration , at the rising edge of the Φ1 clock that determines the amount of added noise during the transition.

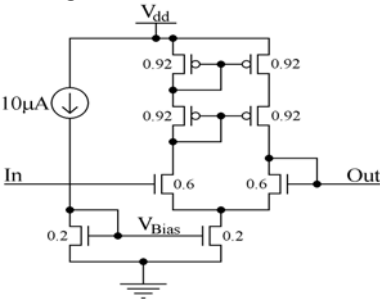

Figure 6. Schematic view of the transconductance amplifiers.

It is important that the two clocks Φ1 and Φ2 do not overlap in order to avoid leak-through from the dump capacitances to the integrating capacitances. The drawbacks with this approach are the need for two extra space-consuming capacitances and the added power consumption of the amplifiers.

Transmission Gates:

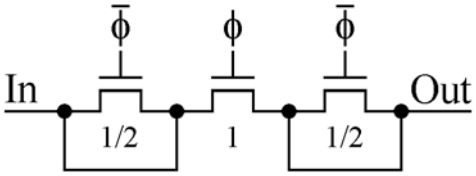

Figure 7. Schematic of a n-MOS switch with compensating transistors to reduce clock feed-through.

When a MOS-transistor is used as a switch and the transistor switches, the change in gate voltage affects the source and drain of the transistor through the gate-drain and gate-source capacitances. To avoid this leak-through, compensating transistors, half the size of the switch transistor can be connected to each side of the switch transistor (see figure 3.8). The drains and sources of these compensating transistors should be short-circuited because it is only the capacitive property of the transistors that is used and the gate connections should be connected to the complement of the gate connection of the switch transistors. With this set-up each time charge leaks through from or to the gate of the switching transistor, an equal amount of charge will leak in the opposite direction to or from the compensating transistors. This design greatly reduces the clock feed-through.

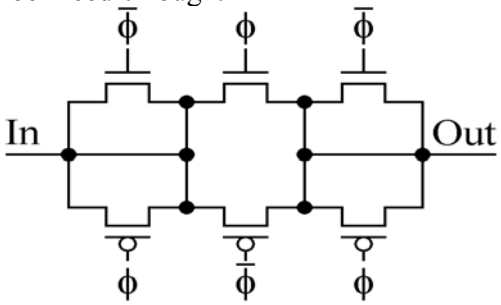

Figure 8. Schematic of a complete transmission gate.

Schematic of Integrator Charge and Dump:

As you can see in no compensating transistors have been added to the input node in order to keep the input capacitance low. In order to keep the voltage levels of the integrating capacitances from drifting due to offset errors of the current inputs, or from mismatch errors between the pull-up and pull-down elements of the DAC, two resistors have been added, one from each integrating capacitance to Vdd/2. The common-mode amplification of the transconductance amplifiers compensate in a similar way for drift in voltage levels of the dump capacitances.

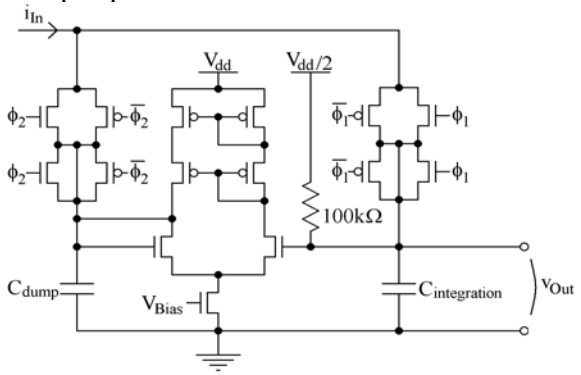

Figure 9. Schematic of the integrator and charge dump.

DAC (Current Sources and Sinks):

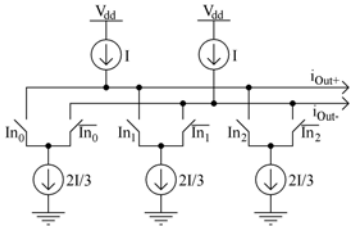

Figure 10. Principle structure of a two-bit DAC.

To achieve high enough linearity at the output of the current sources and current sinks regardless of the voltage levels at the output nodes, a cascode structure has been chosen. Because a high output impedance is desired but at the same time a low output capacitance the first transistor in the source or sink is chosen both wide and long to get a high impedance and the transistor closest to the output, the cascode transistor is chosen relatively small to get a low capacitance at the output node. Because both transistors in the current sources and sinks must be in saturation for the output current to be linear a cascade structure reduces the allowed output voltage swing.

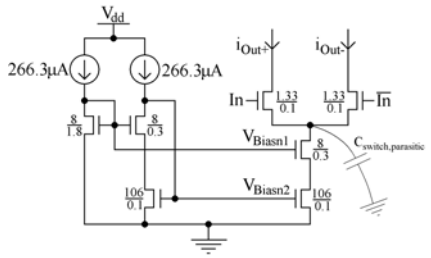

Figure 11. Schematic view of a pull-down element of a three-bit DAC.

Flash ADC:

A flash-ADC is an ADC with (quantization levels - 1) comparators that compares the input voltage to different reference voltages to decide the digital output. This is a fast design but since the number of comparators is 2number of bits−1, it is not practical to use when high resolution is needed. The Flash-ADC in this design has not been realized on a schematic level but programmed in AHDL, Altera Hardware Description Language. During the positive phase of the Φ2 clock the flash-ADC evaluates the differential analog input and at the falling edge of the clock delivers a digital thermometer coded output, as well as the complement of the output.

Value	Three-bit	Four-bit
15		111111111111111
13		011111111111111
11		001111111111111
9		000111111111111
7	1111111	000011111111111
5	0111111	000001111111111
3	0011111	000000111111111
1	0001111	000000011111111
-1	0000111	000000001111111
-3	0000011	000000000111111
-5	0000001	000000000011111
-7	0000000	000000000001111
-9		000000000000111
-11		000000000000011
-13		000000000000001
-15		000000000000000

Table 1. Thermometer code for a three- and for a four-bit flash-ADC.

Verification:

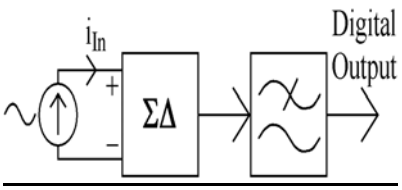

Figure 12. Test setup.

Two tone test: Figure 4. shows the output power spectrum from the DAC with two input signals each with -6 dBfs signal power. Since it is the maximum amplitude of the input signal and not the total signal power that decides when the DAC can no longer compensate for the input signal, this is the maximum input allowed to the ∑Δ.

Out of band blocker: If the gain of the low noise amplifier before the ADC in the receiver chain can be varied, the input signal to the ADC can be kept at a level for optimum operation. In this case the maximum allowed blocker-to-signal relationship for an out-of-band blocker can be expected to be Pblocker−PSINAD=0dB −SNRmin (dB) where SNRmin is the minimum SNR according specifications of the standard used and PSINAD=0dB is the 0 dB intersection. For a three-bit ADC the maximum blocker-to-signal relationship is −3 dBfs − (−78.2 dBfs) − SNRmin = 75.2 − SNRmin dB and for a four-bit ADC the relationship is 79.9 − SNRmin dB.

In band blocker: Because some harmonics of a blocker signal with a frequency lower than fbw/3 appear within the band (see figure 4.5 (a)), the maximum blocker-to-signal allowed in the system for an in-band blocker will be lower than for a out-of-band blocker. The maximum blocker-to-signal relationship for an n-band blocker in a three-bit ADC is 64.1 − SNRmin dB and for a four-bit ADC the relationship is 71.8 − SNRmin dB. Nonlinearities in the mixer and in the LNA before the ADC will further degrade the maximum in-band blocker-to-signal relationship.

Resolution: When a signal with a frequency lower than fbw/3 is sent to the ADC, the harmonics of that signal will appear inside the output band and SINAD will be reduced. In the case of a 1.1 MHz input signal, SINAD is reduced to 62.0 dB for a three-bit ADC, allowing a resolution of 10.3 effective number of bits and to 75.0 dB for a four-bit ADC, allowing a resolution of 12.1 effective number of bits. If we compare SNR instead of SINAD for a 1.1 MHz input and a 9.1 MHz input we can see that the SNR is roughly the same for both input signals and it is therefore apparent that this reduction comes from the harmonics of the input signal. Nonlinearities in the mixer and in the LNA before the ADC will further degrade SINAD.

Noise:

In VLSI design parasitic capacitances are usually a big problem. In this design the part that is most sensitive to parasitic capacitances is the output node of the DAC combined with the output node of the element that generates the input signal to the system. In particular it is very important to keep the capacitance of the pull-down elements low because each time one of these switches, the voltage level of this node has to change from that of one dump capacitance to that of the other.

The voltage levels of an integrating capacitance will have an uncertainty with a variance of kT/Cintegration where T is the absolute temperature and k is the Bolzmann constant after each integration period because of the resistive properties of the transmission gate and of thermal noise. Because the flash-ADC has two inputs and each of these is subject to thermal noise, the total noise variance is twice that of the noise variance of one capacitance. The thermal noise is spread evenly over the entire output spectrum from 0 to the Nyquist frequency of the sampling frequency, fsample/2. In this system the integrating capacitances are dimensioned to Cintegration = 1.33 pF to keep the thermal noise 6 dB below the quantization noise of a 13-bit output from a four-bit ∑Δ-ADC. In a three-bit ∑Δ-ADC with a 12-bit output, the capacitances as well as all transistors and bias currents in the system could be reduced to 1/4 size and still keep the thermal noise 6 dB below the quantization noise.

Conclusion and Future works:

In this report I have shown that it is possible to design a GHz ∑Δ-ADC suitable for an RF front-end. This design has an SNR of 76.5 dB for a first order ∑Δ- loop with three internal bits capable of handling a 75.2 − SNRmin dB out-of-band blocker-to-signal relationship and a 64.1 − SNRmin dB in-band blocker-to-signal relationship. For a four-bit system the SNR is 82.5 dB and the system is capable of handling a 79.9−SNRmin dB out-of-band blocker-to-signal relationship and a 71.8− SNRmin dB in-band blocker-to-signal relationship.

Future work could include: Increase the output swing of the DAC to increase Vfs and thus reduce the capacitance sizes needed due to thermal noise. Reduce the output capacitances of the pull-down elements of the DAC to reduce the non-linear properties of the ∑Δ. Introduce a current output mixer as the source of input signal to the ∑Δ. It is important to note that due to its design, the ∑Δ-loop mixes the input signal with the clock signal and care has to be taken to avoid noise around the same frequency as the clock frequency.

	Design characteristics	
	three-bit ADC	four-bit ADC
SNR	76.5 dB	82.5 dB
SINAD	64.1 dB	75.0 dB
Maximum OB blocker	75.2 − SNRmin dB	79.9 − SNRmin dB
Maximum IB blocker	64.1 − SNRmin dB	71.8 − SNRmin dB
Theoretical	12.6 bits	13.6 bits
ENOB	12.4 bits	13.5 bits
ENOB from SNR	10.3 bits	12.1 bits
ENOB from SINAD		

Table 2. Characteristics of the two designs analyzed in this report.

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