ANALYSIS OF SINGLE-PHASE Z-SOURCE INVERTER

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Abstract: This paper deals with the analysis of a single-phase Z-source inverter with common ground between the source and load. It gives the output same as that for full-bridge inverter for the specified input using only two switches. One-cycle control strategy is used as controlling technique for this topology. The topology is analysed using load and no load condition and verified by the simulation results.

Index Terms—Converter, one cycle control, single phase Z source inverter, Z source inverter.

1. INTRODUCTION

The traditional power converters are basically of two types: voltage-source converters and current source converters. These can be used in single phase as well as three-phase power converters. This paper mainly focuses on a single-phase power conversion. The traditional voltage-source converters and current-source converters have certain disadvantages associated with them. In case of voltage-source (V-source) converters, it acts as a buck (step-down) converter for DC to AC power conversion and as a boost (step-up) converter for AC to DC power conversion. In case of current source (I-source) power converter, it acts as a boost converter for DC to AC power conversion and as a buck converter for AC to DC power conversion. Thus, V-source and I-source power converter can be used as either as a boost or a buck converter and not as a buck-boost converter. Moreover, in case of a three-phase power conversion, if both the upper and lower switches of the same leg are simultaneously turned ON either by purpose or by electromagnetic interference, a shoot-through occurs and the converter is damaged [1].

For single-phase power conversion, the basic topologies used include the bridge topologies. Fig. 1(a) and (b) shows full bridge inverter and half bridge inverter topologies resp. In case of full bridge inverter, four switches are used to get desired output voltage, whereas in case of half bridge inverter topology only two switches are used. But the output voltage obtained in half bridge inverter topology is half the input voltage.

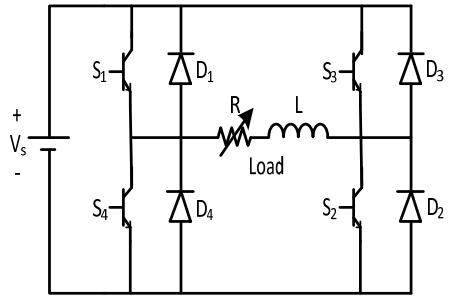


Fig. 1 (a): Full bridge inverter

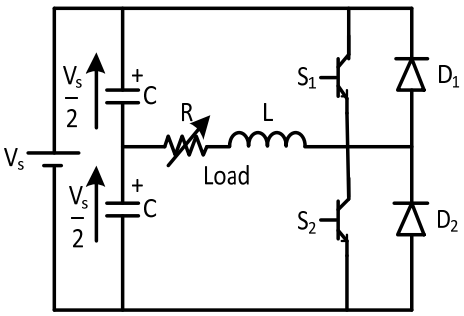


Fig. 1 (b): Half bridge inverter

Due to the use of more switches, full bridge inverter topology is costly. All the disadvantages mentioned above of the traditional V-source, I-source and bridge converter topologies are overcome by the use of Z-source (impedance source) converters.

2. Z-SOURCE CONVERTER

The impedance source or Z-source converter provides the unique features which overcomes the disadvantages of the traditional voltage source converters and current source converters. Fig (2) shows the basic structure of Z-source converter topology. It employs the unique impedance network which is used to couple the converter circuit to the power source (may be voltage source or current source), load or another converter. It can be used for implementing DC to AC, AC to DC, DC to DC or AC to AC power conversion with both the step-down and step-up features [1].

In basic topologies, Z-source networks are symmetrical. The basic impedance network consists of two identical inductors L_1 and L_2 and two identical capacitors C_1 and C_2 connected in X-shape as shown in Fig.2 providing coupling between the power source and load. The impedance network is the energy storing element for the converter. The same impedance network can be used in a single-phase or three-phase Z-source converter topology. Depending on the type of power supply used, Z-source converter is either voltage-fed Z-source converter or current-fed Z-source converter. In case of 3-phase converters, a voltage-fed Z-source converter has an unique feature of allowing both the upper and lower power switches of the same phase-leg to be turned ON simultaneously without damaging the converter [2].

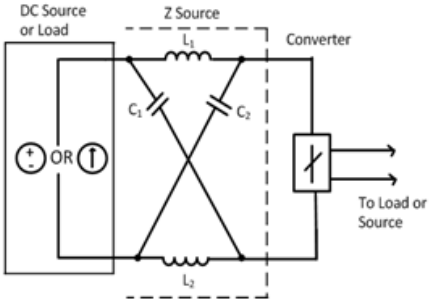
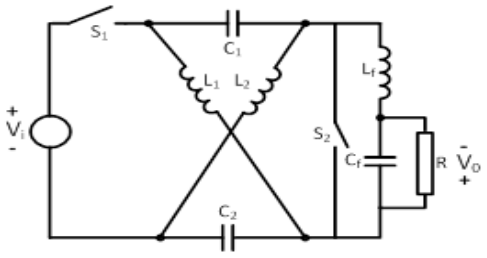
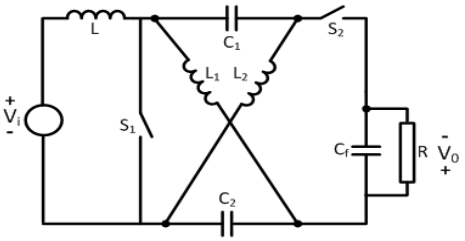


Fig. 2: Basic structure of Z-source converter



(a)



(b)

Fig. 3: 1-ph Z-source converter topologies
(a) Voltage-fed (b) Current-fed

The single-phase Z-source inverter consists of two switches and impedance source network giving the output same as that of the full bridge inverter with reduced number of switches. Fig. 3(a) and 3(b) shows the basic topologies of single-phase Z-source converter: (a) Voltage-fed and (b) Current-fed resp. The two switches S1 and S2 are tuned ON and OFF in complement. The relationship between the voltage gain and duty ratio D of the voltage-source and current-source topologies, respectively, is given by

$$\frac{Vo}{Vi} = \frac{D}{2D-1} \qquad (1)$$

and

$$\frac{Vo}{Vi} = \frac{2D-1}{D-1} \qquad (2)$$

From equation (1), when voltage gain is plotted against duty ratio, it shows that the Z-source converter acts as both step-up and step-down converter. This is a unique feature of Z-source inverter as compared to other inverters. From fig 3(a) and 3(b), it can be seen that these topologies need separate grounding for source and load and hence it cannot be used in cases where a common grounding is required for source and load. This paper deals with a single-phase Z-source inverter topology with common ground between the source and load [3]. One-cycle controlled strategy is adopted as a control strategy for this topology [4].

3. SINGLE-PHASE Z-SOURCE INVERTER TOPOLOGY WITH COMMON GROUND

Fig.4 shows the single-phase Z-source inverter topology having common ground between the input and the output. The Z-source network employed in this topology is unsymmetrical unlike the basic Z-source inverter topology

discussed above. The proposed topology constitutes an unsymmetrical impedance network consisting of two inductors L_1 and L_2 and a single capacitor C, DC voltage source V_i, two switches S_1 and S_2 and filter capacitor C_f. This topology uses only two switches unlike full-bridge inverter which uses 4 switches while keeping the voltage transfer ratio the same as for the full-bridge inverter topology.

The two switches S_1 and S_2 act in complement to each other. Assuming 'D' to be the duty ratio and 'T' to be the switching period, switch S_1 is ON for DT period and switch S_2 is ON for the period (1-D)T. So, there exist two switching states in one switching cycle which are shown in Fig. 5(a) and 5(b).

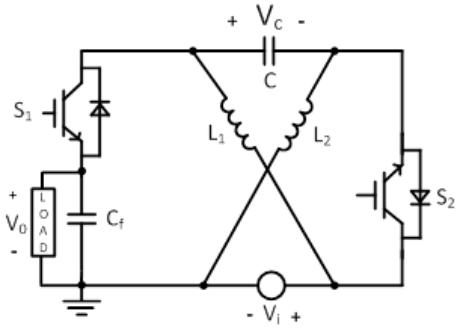
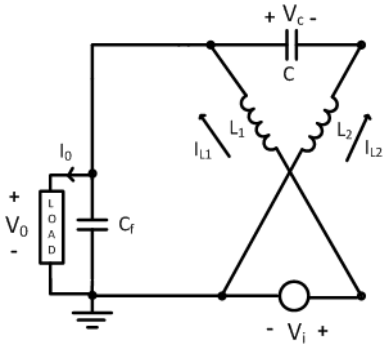
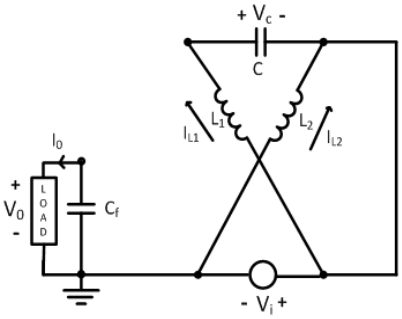


Fig.4: 1-ph Z-source inverter topology with common ground



(a)



(b)

Fig. 5: Equivalent circuits (a) State 1 (b) State 2

For the period DT, from fig. 5(a), the equations can be written as,

$$L_1 \frac{di_{L1}}{dt} = V_i - v_o$$

$$L_2 \frac{di_{L2}}{dt} = v_c - v_o$$

$$C \frac{dv_c}{dt} = -i_{L2}$$

$$C_f \frac{dv_o}{dt} = i_{L1} + i_{L2} - i_0 \qquad (3)$$

For the period (1-D)T, from fig. 5(b), the equations can be written as,

$$L_1 \frac{di_{L1}}{dt} = -v_c$$

$$L_2 \frac{di_{L2}}{dt} = -v_i$$

$$C \frac{dv_c}{dt} = i_{L1}$$

$$C_f \frac{dv_o}{dt} = -i_0 \qquad (4)$$

Averaging equations (3) and (4) over time period T, we write,

$$L_1 \frac{di_{L1}}{dt} = D(V_i - v_o) - (1-D)\, v_c$$

$$L_2 \frac{di_{L2}}{dt} = D(v_c - v_o) - (1-D)\, v_i$$

$$C \frac{dv_c}{dt} = -Di_{L2} + (1-D)\, i_{L1}$$

$$C_f \frac{dv_o}{dt} = D(i_{L1} + i_{L2}) - i_o \qquad (5)$$

From the above equations and the circuit, the steady state equations can be written as,

$$v_C = V_i \qquad (6)$$

$$\frac{v_o}{V_i} = \frac{2D-1}{D} \qquad (7)$$

$$i_{L1} = i_o \qquad (8)$$

$$i_{L2} = \frac{1-D}{D} i_{L1} \quad (9)$$

From equation (7), it can be seen that the network performs buck-boost conversion with changing polarity when D < 0.5. Also, it acts as a buck inverter for D > 0.5 with the output polarity same as that of the input. For small value of duty ratio, the circuit is affected more by external factors. For this topology, duty ratio ranges from 1/3 to 1 and hence it acts as a buck inverter. From equation (9), we get the relation between two inductor currents, which depends on the duty ratio. For the minimum value of duty ratio, we get maximum unbalance in the two inductor currents as $i_{L2} = 2\, i_{L1}$.

From fig.4 and equation (6), we can write the equation for voltage across switch S1 as,

$$v_{S1} = v_C + V_i - v_o = 2V_i - v_o \quad (10)$$

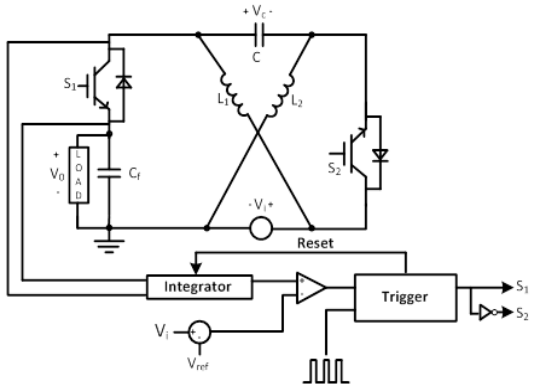


Fig.6: Z-Source inverter with one-cycle control strategy.

Thus, the voltage across the switches is more.

The elements of the impedance networks are designed based on the ripple contents. Fig. 5(b) shows that the capacitor C is charged by the current i_{L1} in the time interval (1-D)T. Thus, the voltage ripple across the capacitor is given by

$$\Delta V_C = \frac{i_{L1}(1-D)T}{C} \cong C = \frac{i_{L1}(1-D)T}{k_v * v_i} \quad (11)$$

Also, the inductor current ripple can be given as,

$$\Delta i_L = \frac{Vi*D*T}{L} \cong L = \frac{Vi*D*T}{k_i * i_L} \quad (12)$$

Where, k_v and k_i are capacitor voltage and inductor current ripple factors respectively.

4. ONE-CYCLE CONTROL THEORY

Using one-cycle control strategy, the power source perturbations can be minimised and highly efficient constant frequency control can be achieved. It corrects switching error on one switching cycle. Duty ratio of the switch depends on the states of the current switching cycle. Fig.6 shows Z-Source inverter with one-cycle control strategy.

The voltage across switch S1 is sensed and fed to the integrator. S1 is switched OFF and S2 is switched ON by the clock signal. Thus, the integrator voltage is given by,

$$v_{int} = k \int_0^t (V_{S1} dt)$$

$$= k \int_0^{(1-D)T} (v_C + V_i - v_o) dt \quad (13)$$

The integrator will reset when the integrator value reaches $V_i - V_{ref}$ and S1 will be switched ON.

$$v_{int} = V_i - V_{ref} \quad (14)$$

The average value across the switch S1 is given by

$$\overline{V_{S1}} = \frac{1}{T} \int_0^{(1-D)T} \left(v_C + V_i - v_o\right) dt = \mathrm{K}(V_i - V_{ref}) \quad (15)$$

Where, $K = \frac{1}{kT} = 1$

The average voltage across inductor L, in steady state, is zero.

$$\overline{V_{S1}} = V_i - v_o \quad (16)$$

Comparing equations (15) and (16)

$$V_i - V_{ref} = V_i - v_o$$

Thus, $$V_{ref} = v_o \quad (17)$$

5. SIMULATION RESULTS

Simulations have been performed to analyse the proposed topology. The z-network parameters used are: Inductors L_1 and L_2 = 2 mH, capacitor C = 220 µF. Other parameters are: Input DC voltage V_i = 350 V, output voltage v_o = 230 V, output voltage frequency is 50 Hz, switching frequency is 25 kHz and filter capacitance C_f = 25 µF. The load resistance is 60 Ω. Fig.8 shows the simulation results for load resistance R = 60 Ω. Also, to analyse the effect of mutual inductance, coupling of factor of 0.5 is used for the same parameters. Fig.9 shows the simulation results for load resistance R = 60 Ω with mutual inductance. From fig.8 and fig.9, it can be seen that the ripples are reduced to the great extent by the use of mutually coupled inductors. Fig.10 shows the simulation results for no load with mutual inductance.

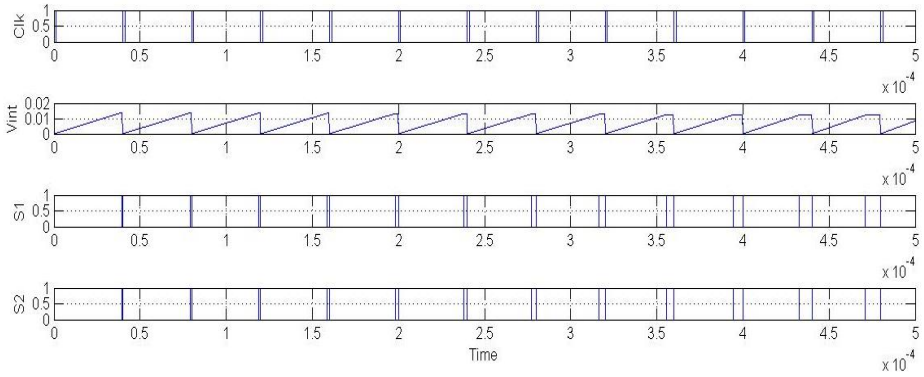


Fig.7: Principle Waveform for one-cycle control

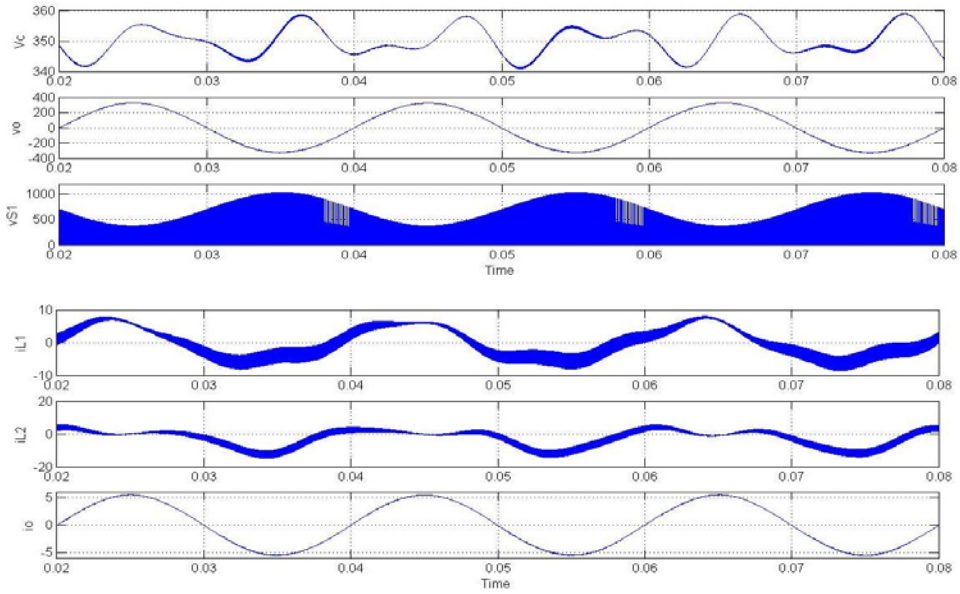


Fig 8: Simulation result for load resistance R = 60 Ω without mutual inductance.

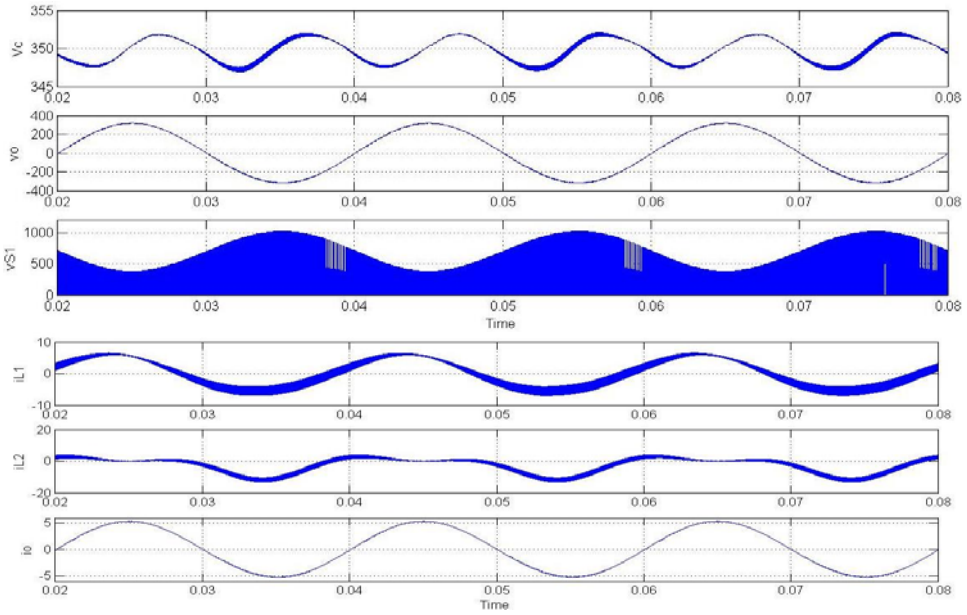


Fig 9: Simulation result for load resistance R = 60 Ω with mutual inductance.

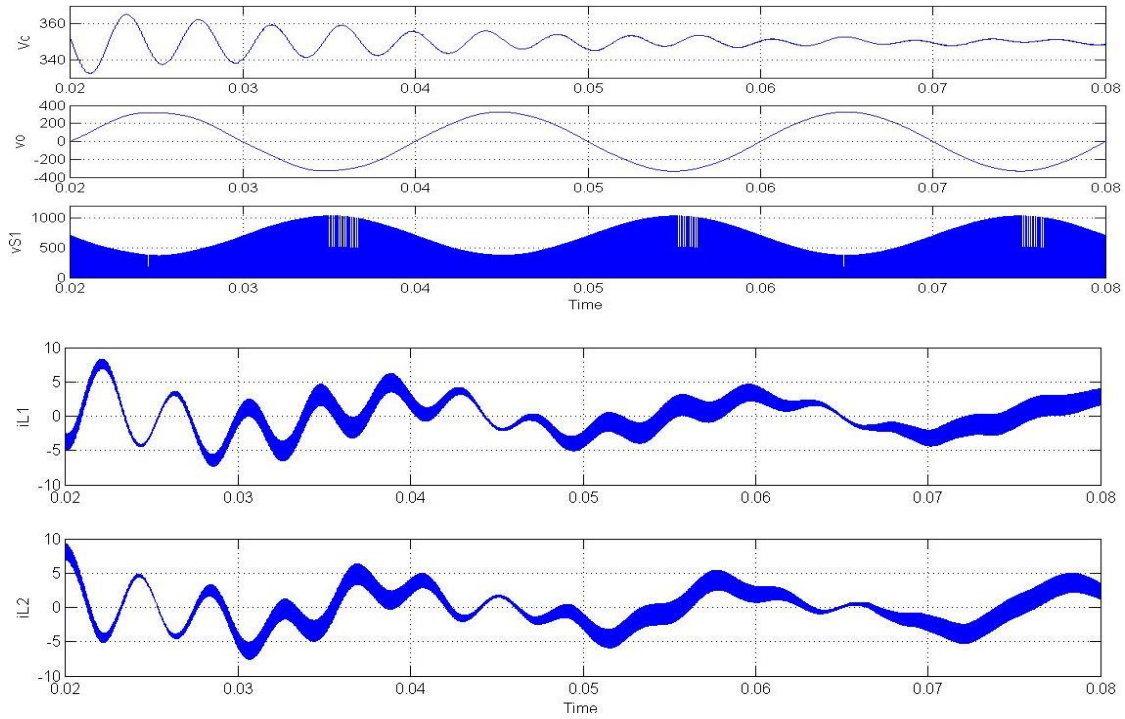


Fig. 10: Simulation results for no load with mutual inductance.

6. CONCLUSION

A single-phase Z-source inverter topology with common ground between the supply and load has been analysed. The topology is analysed by network analysis and simulation also performed to check the result. The effect of mutual inductance in Z-source network has also been analysed.

7. REFERENCES

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