VHDL DESIGN FOR VIDEO COMPRESSION

[1]Sonali M. Wararkar, [2]Prof. V.M.Joshi
[1]PG Student, [2]Assistant Professor,
Department of E&TC, PVPIT, Pune, India.
Email:[1]sonali.wararkar13@gmail.com [2]joshivaishali7@gmail.com

Abstract—Video compression is a very useful tool to eliminate the amount of excess data in video files. Compression creates a new file that stores data in a format that require less space. Video compression is reducing redundancy in video data. Compression techniques are used in video conferencing, video telephony, video on mobile phone, video on internet, HDTV broadcast. Common methods of video compression are the 1D DCT, DWT and dual tree DCT. These techniques have some drawbacks such as Discrete Wavelet Transform (DWT) performs compression of video in large amount and because of such huge amount of compression the quality of video/image reduced. The processing of 1D DCT is very slow. Dual tree DCT consume more time. The proposed system will be designed by using 2D DCT and the main advantage of the proposed system is that it will help to overcome the drawback of 1D DCT, DWT and dual tree complex wavelet transform. The proposed system will help to improve the speed of the compression, efficiency of the video also it consuming less time.

Index Terms— Video compression, DCT, Simulink, Xilinx System Generator (XSG), Hardware Co-Simulation

I. INTRODUCTION

Most video applications involve the transmission or storage of a large amount of data. To reduce the requirements in terms of bandwidth and storage, some form of data compression is often used to transmit or store video. A variety of data compression techniques have been developed over the last few years for various applications.[1] In this paper, video compression is studying for use in areas where a low-complexity is desired.

Everyone knows that video is the series of images or the meaning of video is the motion pictures. Video is a term used to describe any sequence of time varying images. Movies or films, digital cameras and television are some examples of video signals as are the signals that drive computer monitor, laptop, mobile and PDA displays. Video is made up of number of frames. The compression of an image or video file is of great concern in digital communication system because of the storing capacities and constraints in the transmission rate. And a video compression format or a video compression specification is a specification for digitally representation of video as a file or a bit stream. In this paper, focus is on video compression using very hardware description language.

II. PROPOSED 2D-DCT BASED VIDEO COMPRESSION

The basic block diagram of video compression using 2D DCT transform as shows fig.1

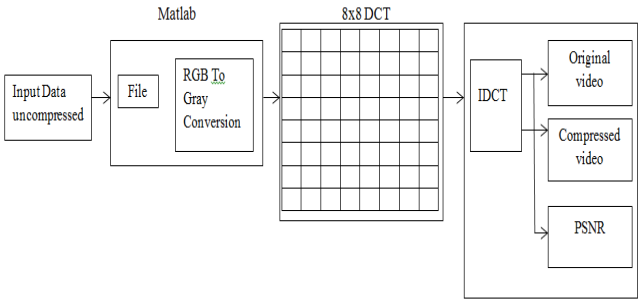


Fig.1 Block diagram of 2D-DCT based video compression

Step1: AVI file

AVI files can be created with no Compression, resulting in extremely large file sizes, but with no loss of quality from the input video to the saved file.

Step2: RGB to Gray Conversion

Fig. 2 shows RBG to gray conversion diagram. Transmitting images or video in RGB color space is not practical as their bandwidth requirement is very high. To overcome this problem and minimize the bandwidth requirement images in RGB color space are converted into other color space such as gray and then transmitted. For color space conversion, the RGB image is taken and converted into pixels. The generated pixels are given to the color converter module. The color conversion module generates new set of pixels, gray pixels which are given back to the software which recreates the image in gray color space. This design helps us to reduce the overall hardware requirement of the system. [4]**.** Image involving only intensity are called gray scale images. If only the brightness information is needed, color images can be transformed to gray scale images. The transformation can be made by equation.

$$Iy=0.333Fr+0.5Fg+0.1666Fb$$

Where Fr, Fg and Fb are the intensity of R, G and B component respectively and Iy is the intensity of equivalent gray level image of RGB image. In RGB pixel information image there are three component (R,G,B) and each component has a fix intensity 190, 183, 175. When RGB image converted into gray image then the intensity of pixel (1, 1) can be calculated by using the pixel values of RGB image in above transformation.

Iy=0.333*190+0.5*183+0.1666*175=183.925

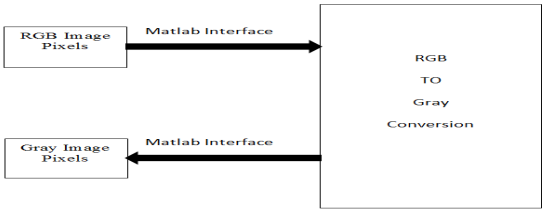


Fig. 2.RGB to gray color conversion

Step3: Discrete Cosine Transform

A DCT expresses a finite set of data in terms of cosine waves oscillating at different frequencies with different amplitude. DCT has several applications in science and engineering where frequency spectrum and compression of data is under consideration. This is usually the case for audio and video applications. The reason why DCT is that popular in image processing is the ability of energy compaction.[2]

The formal definition of DCT is given below:

$y(k) = w(k)\sum_{n-1}^{N} x(n)\cos(\frac{\prod(2n-1)(k-1)}{2N})$ k= 1,2…..N

Where

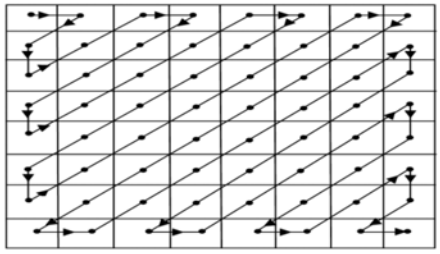
$$w(k) = \begin{cases} \frac{1}{\sqrt{N}} & k = 1 \\ \sqrt{\frac{2}{N}} & = 2 \le k \le N \end{cases}$$

N is the length of x, and x and y are the same size. If x is a matrix, dct transforms its columns. The series is indexed from n = 1 and k = 1 instead of the usual n = 0 and k = 0 because MATLAB vectors run from 1 to N instead of from 0 to N-1.

y = dct(x,n) pads or truncates x to length n before transforming.

Step4: Zigzag Pattern

DCT coefficients are rearranged in increasing frequency order (zig-zag order) as shown in Fig. 3. The first DCT coefficient is having zero frequency. It is called DC coefficient and the rest of the 63 coefficients are called AC coefficient. DC coefficient from the previous blocks are subtracted with the current block (differential coding). The DC coefficients represent the average image information of the block. The DC differential coding is performed to reduce the code size as nearest block possess the almost same average energy. [3]



0	1	5	6	14	15	27	28
2	4	7	13	16	26	29	42
3	8	12	17	25	30	41	43
9	11	18	24	31	40	44	53
10	19	23	32	39	45	52	54
20	22	33	38	46	51	55	60
21	34	37	47	50	56	59	61
35	36	48	49	52	58	62	63

Fig. 3. Zig-zag ordering for DCT coefficients [6]

Step4: Inverse Discrete Cosine Transform

The inverse discrete cosine transform reconstructs a sequence from its discrete cosine transform (DCT) coefficients. The IDCT function is the inverse of the DCT function. x = IDCT(y) returns the inverse discrete cosine transform of y

$$x(n) = \sum_{k=1}^{N} w(k)y(k)\cos\left(\frac{\pi(2n-1)(k-1)}{2N}\right)$$
$$n = 1,2,\ldots\ldots N$$

Where

$$w(k) = \begin{cases} \frac{1}{\sqrt{N}} & k = 1 \\ \sqrt{\frac{2}{N}} & 2 \le k \le N \end{cases}$$

and N = length(x), which is the same as length(y). The series is indexed from n = 1 and k = 1 instead of the usual n = 0 and k = 0 because MATLAB vectors run from 1 to N instead of from 0 to N-1.x =idct(y,n) appends zeros or truncates the vector y to length n before transforming. If y is a matrix, IDCT transforms its columns.

III. HARDWARE IMPLEMENTATION

Field Programmable Gate Array (FPGA) is a reconfigurable IC. Spartan6 SP601 is chosen for hardware implementation because of it has advantages like reconfigurability, contains 128mb of DDR2 component memory, low power, small size, & high speed of operations. The implementation process of image fusion algorithms on hardware has the most viable solution for improving the performance of the systems. A Field Programmable Gate Array (FPGA) is one such reconfigurable hardware, offering superior features than DSP & other hardware device due to their product reliability & maintainability advantages in digital image processing. The multiple processing data sets require in many algorithms have to be performed sequentially on a computer and fused one pass in FPGA.

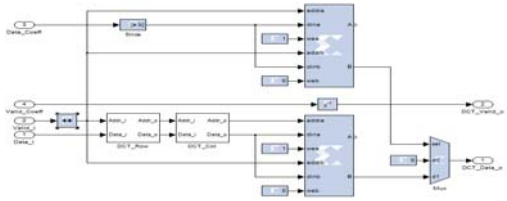


Fig. 4. modeling of FPGA implementation of video compression using 2D DCT

It is very difficult to write a code for FPGA design [5]. To create an FPGA design, using Hardware Description Language (HDL) such as VHDL or Verilog. Xilinx System Generator is a MATLAB-simulink based design tool which offers high performance & require very less learning and development time. XSG for FPGA is a tool which offers block libraries that plugs into Simulink model tool is integrated with MATLAB window. Simulink has become an important part of engineering programs and industries. To start with Simulink in matlab, double-click on Simulink icon. The Simulink window opens. Then with the help of Simulink Library Browser, we can access the different toolboxes available for processing. The Video and Image processing block set contains a number of elements such as sources, sinks, math operators, parameters etc. The Xilinx Block set contains various elements shown below such as Basic Elements, Math, Shared Memory, Control logic, tools etc. Fig.4 shows the complete Simulink design model of FPGA implementation of video compression using 2D-DCT algorithm.

IV RESULT AND DISCUSSION

Table 1 Device utilization summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	520	18224	2%
Number of Slice LUTs	449	9112	4%
Number of fully used LUT-FF pairs	119	850	14%
Number of bonded IOBs	44	232	18%
Number of Block RAM/FIFO	2	32	6%
Number of BUFG/BUFGCTRLs	1	16	6%
Number of DSP48A1s	10	32	31%

Minimum period: 16.400ns (Maximum Frequency: 60.976MHz)
Minimum input arrival time before clock: 3.305ns
Maximum output required time after clock: 7.233ns
Maximum combinational path delay: No path found

Original video

90% compression

50% compression

10% compression

By the study of compression it shows that Discrete Wavelet Transform (DWT) performs compression of video in large amount and because of such huge amount of compression the quality of video/image reduced. But in Discrete Cosine transform (DCT) compression, quality of video is maintain even after performing the compression and this is the advantage of DCT compression

V. CONCLUSION AND FUTURE SCOPE

Video-compression is reducing redundancy in video data Compression technique. Also allows more efficient storage & transmission of data. Xilinx software is used for both as synthesis and simulation for giving output result respectively. Verilog HDL is a hardware description language that can be used to model a digital system. By using DCT computation perform a large number of multiplication & addition but with well established and regular data access pattern DCT used which is simple to computation as compared to DWT, After reordering the reaming coefficients it is cheaper in cost than other compression algorithm also Require less storage & easy to computation. So by using require less blocks, minimum costing & simple algorithm video compression are done. Discrete Wavelet Transform (DWT) performs compression of video in large amount and because of such huge amount of compression the quality of video/image reduced. The processing of 1D DCT is very slow. Dual tree DCT consume more time. By using 2D DCT the drawback of 1D DCT, DWT, dual tree DCT has been eliminated. 2D DCT system had improved the speed of the compression, efficiency of the video also it consume less time. The future work will be that the compression can be done by using new format of compression i.e. H.264.

REFERENCES

[1]International conference on telecommunication and computing [ICTC-13] ECE, kits, Ramtek India on"VHDL design using concept of system on chip for video compression" by SHWETA ARUN SARODE M.TEC [Electronics Engineering] Student, and PROF.S.M.KHARAD Prof. and Head of Department Of E&C Engineering. Kavikulguru Institute of Technology Science, Ramtek, Maharashtra, india.

[2]International Journal of Computer Applications (0975 – 8887) Volume 65–No.10, March 2013 on "An Area Efficient Design of Fully Pipelined, 2D DCT, Quantizer and Zigzag JPEG Encoder using VHDL" by Durg Patidar, Jaikaran Singh, Mukesh Tiwari, Department of Electronics and Communication Engineering Sri Satya Sai Institute of Science and Technology, Sehore M.P. India

[3] Thesis on Efficient VLSI Architectures for Image Compression Algorithms by Vijay Kumar Sharma January 2012.

[4]International Journal of Computer Applications (0975 – 8887) Volume 7– No.2, September 2010 on "A Theory Based on Conversion of RGB image to Gray image" by Tarun Kumar Assistant Professor Computer Science and Engineering Department Vidya College of Engineering, Meerut (U.P)and Karun Verma.

[5] Thesis on Video compression by Kellie Frazier 2010

[6] Thesis on JPEG Image Compression Using an FPGA by James Rosenthal December 2006