HIGH GAIN DC-DC CONVERTER INCORPORATING SWITCHED CAPACITORS FOR HIGH VOLTAGE APPLICATIONS

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Abstract— Fuel cell stacks and photovoltaic panels generate low DC voltages. In order to make them use in various high voltage applications, the voltage is to be adjusted to required levels. Thus a high gain DC-DC converter is employed which in turn serve to become a key part of renewable energy system. This project presents a new family of Inductor Energy Storage Cell-Switched Capacitor(IESC-SC) based DC-DC converter which incorporates the excellent voltage regulation capability of simple boost circuit and high gain capability of SC cells. The converter topology is designed and simulated with MATLAB/Simulink to validate its theoretical result. Besides, the performances of conventional circuits are being compared with the present topology. The improved effectiveness due to the lower power loss, high voltage step up gain and a lower switch voltage stress when compared to other topologies become the attractive feature for its use with DG systems. A circuit based prototype has been built for 12 V input and 60V output voltage to obtain 35W output power and the theoretical result is being validated. Closed loop control for the converter has also been done.

Keywords—Boost converter, Non-isolated, Switched Capacitor, Voltage gain.

I. INTRODUCTION

The output voltage of the renewable energy system is too low to be able to connect to the load in standalone application or to the grid [1]. This urges the need for a high step up converter to boost the low voltage to very higher level. Fig. 1 shows the architecture of a solar micro-grid where there is a need of high voltage gain Considering the cost, size and efficiency non-isolated transformer less converters are preferred.

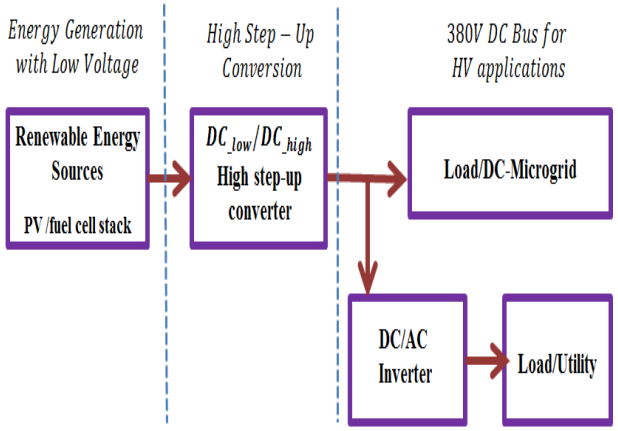

Fig.1.The architecture of a solar micro grid [1]

Simple boost converters are the conventional and simple topology among non-isolated systems with continuous input current. But to achieve high voltage gain duty cycle approaches unity causing poor dynamic responses to line and load variations. Consequently efficiency decreases drastically. Also the voltage stress across the switch is very high since the output voltage will come directly across the switch [2]. Later various boost converters have been cascaded and is found that high voltage gain is obtained but the efficiency becomes the product of each added boost converters. Also it becomes complex and difficult to regulate the output voltage due to multiple switches.

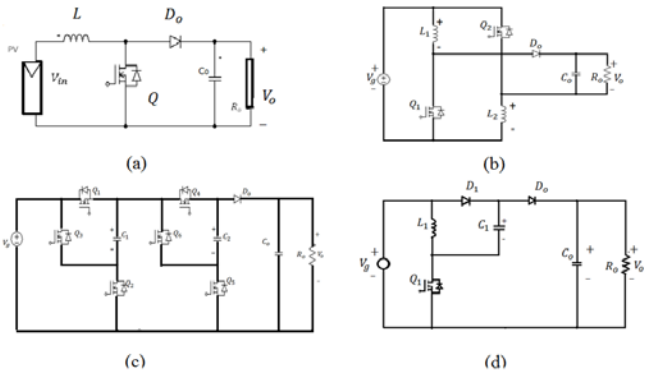

Fig.2. Step up converters (a). Simple boost converter [3] (b). Two Inductor Boost Converter [4] (c). Switched Capacitor Converter [5] (d). Luo Converter [6]

Various high gain converters have been discussed in the literature. The complexity of the cascaded boost converter has been rectified by the quadratic boost converter where the output voltage have quadratic dependence on the duty ratio but the efficiency is still the same as that of cascaded converters. Switched Capacitor (SC) converter circuits which consist of capacitors, switches and diode can obtain high voltage gains depending upon the number of capacitors used [6]. The exemption of inductors in the circuit makes the circuit more compact and light with high power density. But the high current spikes limit its usage. Also the circuit structure predetermines the voltage conversion ratio which makes it non flexible to be used in renewable energy applications.

Luo has incorporated the switched capacitor converter circuit into the simple boost converter to obtain a hybrid one for the use in high power application [7]. But it is found that the voltage gain is still low for efficient operation when high voltage gain is needed. When the SC cells were incorporated in Two Inductor Boost Converter (TIBC) converters [8], high voltage gain is obtained but with the limitations that this circuit cannot be further extended in need of very high voltages at the output. Complexity to regulate the output voltage due to the presence of two switches adds to its drawback.

Thus a task of integrating the advantages of the high voltage gain of SC converter and excellent output regulation of a switching-mode DC-DC converter is to be done. Further, the implementation of such devices needs to be an optimum configuration with the following constraints.

1. less size
2. simple control
3. minimum possible components for maximum possible voltage gain
4. less voltage stress across the switch
5. extendible

Thus an optimum inductor energy storage cells - switched capacitor based high gain converter circuit is to be built

II. PROPOSED TIESC-SC CONVERTER

A. *Derivation of TIESC-SC Converter*

To eliminate rigidity in the output voltage regulation with change in input voltage, an inductor is used along with SC. The inductor is used to store the charges needed for capacitors to contribute to the output voltage and it is named as an inductor energy storage cell. SCs can be integrated with an inductor cell either by connecting the SC cell across the inductor or by connecting it across the switch [9]. Basic configuration of an inductor storage cell with the switched capacitor is as shown in Fig 3.

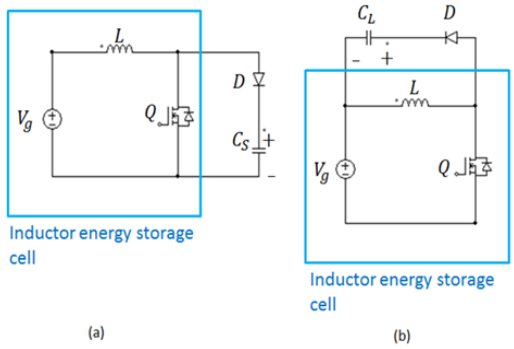

Fig.3. Circuit configuration of quadratic boost converter [9]

When connected across the switch, SC act as the load for boost converter and thus the voltage induced in the capacitor C_S is given by the Eqn 1.

$$V_{CS} = \frac{V_g}{(1-D)} \text{..... ....(1)}$$

When connected across the inductor, SC act as the load for buck-boost converter and the voltage induced in the capacitor is given by Eqn (2)

$$V_{LS} = \frac{V_g \times D}{(1-D)} \text{..... ....(2)}$$

The elementary circuit, which consist of single inductor energy storage cell incorporating switched

capacitor cells also called as Single Inductor Energy Storage Cell-Switched Capacitor (SIESC-SC) converter is as shown in the Fig 4.

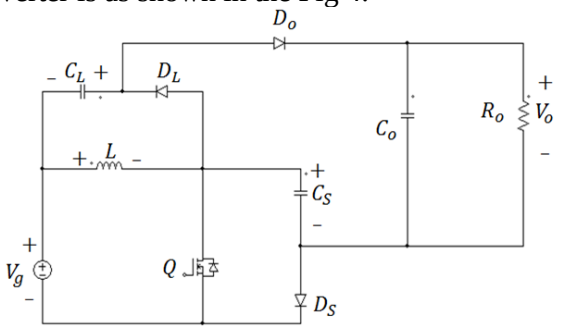

Fig.4. Elementary Circuit of TIESC-SC Converter

The elementary circuit has 2 modes of operation in continuous conduction mode and are shown in Fig 5 and Fig 6.

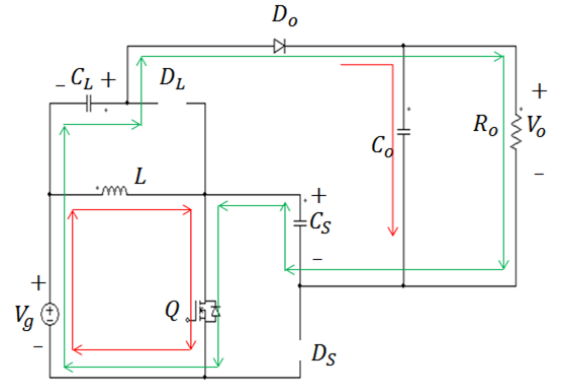

Fig.5. Mode I operation: When switch, Q=ON

When the switch Q is ON, diodes D_L and D_S gets reverse biased. During this period, the input voltage source V_g charges the inductor. Also, capacitors C_S and C_L are in series with the input voltage source to serve the load and the output capacitor C_o through Q.

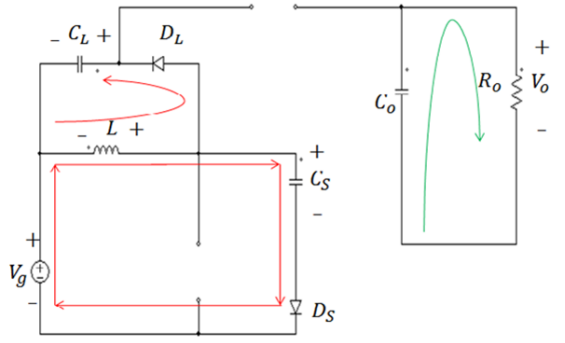

Fig.6. Mode II operation: When switch, Q=ON

When switch is OFF Diodes D_L and D_S gets forward biased. D_o is reverse biased and the load is isolated from the input voltage source. C_S gets charged by both the inductor and the input voltage source but the capacitor C_L is replenished only by the inductor. Output capacitor continues to serve the load. Model graph of the hybrid converter is shown in the Fig 7.

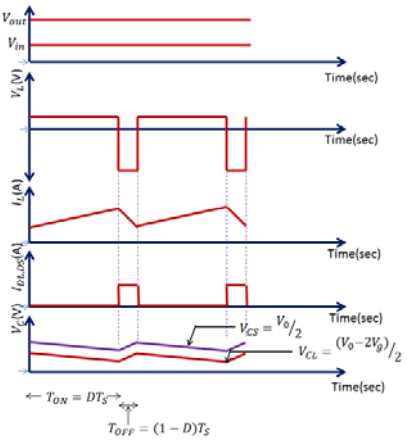

Fig.7. Model waveform of hybrid elementary SIESC-SC DC-DC converter

The output voltage of the circuit will be the sum of the voltages of C_S, C_L and V_g and thus the voltage gain M is given by:

$$M = M_{CS} + M_{CL} + M_{V_g} \quad \text{.....(3)}$$

$$M = \frac{1}{1-D} + \frac{D}{1-D} + 1 \quad \text{.....(4)}$$

$$M = \frac{2}{1-D} \quad \text{.....(5)}$$

Two inductor energy storage Cell- Switched Capacitor based high step up dc-dc converter is being derived from the elementary circuit. It has one switch, two inductors, five capacitors, and (n+2) diodes. The circuit diagram of TIESC-SC converter is as shown in the Fig 8.

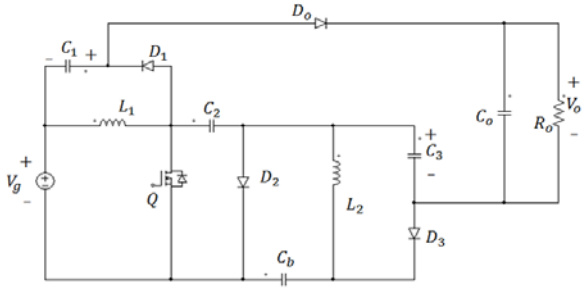

Fig.7. Model waveform of hybrid elementary DC-DC converter

Here the SCs are added in series to the existing SCs to increase the voltage gain. An inductor energy storage cell, which consist of L_2, D_2 and C_b is added to replenish the energy for the added SC which in this case is C_2. C_b acts as a voltage source and contribute to the charging of SCs in the circuit.

B. Modes of operations

The TIESC-SC converter has three distinct intervals in CCM and are being described in the following.

Mode I-[t_o, t_1]: In mode I operation of TIESC-SC converter, the switch Q is ON and is in conducting stage. The input voltage source charges L_1 and capacitor C_2 charges C_b and L_2. Meanwhile, C_2 and C_3 are in series with the voltage source and C_1, to supply the load through Q. Thus, V_{C3} decreases while V_{Cb} increases. As the voltages of C_b and C_3 are equal before the switch conducts, we have V_{Cb} greater than V_{C3}. In this mode, both the inductor current increases as the inductors are being charged.

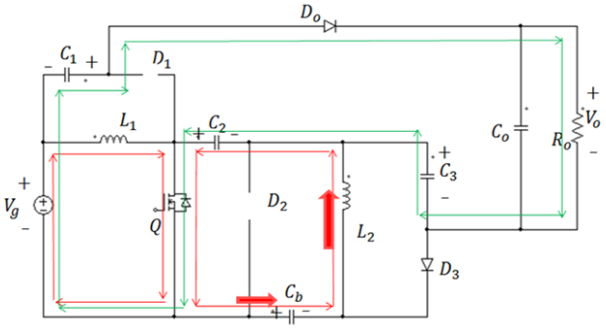

Fig.9. Mode I operation: When switch Q=ON

Mode II-[t_1, t_2]: The switch Q is turned OFF during the mode II of TIESC-SC circuit operation. Because of V_{Cb} is greater than V_{C3}, D_3 conducts and D_2 remains in OFF position. L_2 charges C_1 via D_1, and it charges C_2 and C_3 and discharges C_b. Meanwhile, L_2 charges C_3 via D_3.

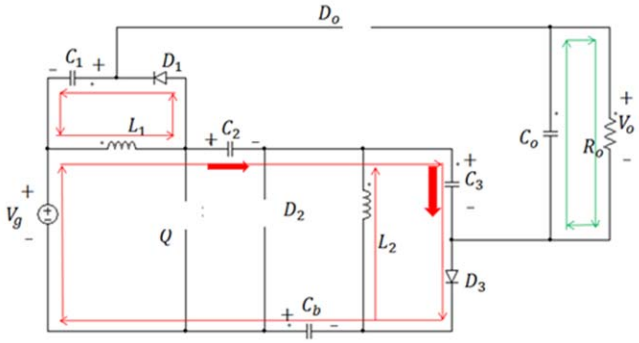

Fig.10. Mode II operation: When switch Q=OFF

Mode III-[t_2, t_3]: The switch, Q remains to be in OFF position. When V_{C3} increases to V_{Cb}, D_2 conducts and L_2 charges C_3 and C_b in parallel. Thus, $V_{C3} = V_{Cb}$. At the same time, L_1 charges C_1 through D_1 and charges C_2 via D_2. At the end of this mode both the inductor currents decrease to the maximum, since, the inductors are being discharged.

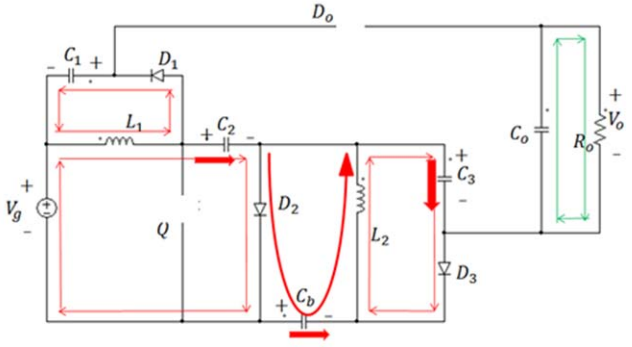

Fig.11. Mode III operation: When switch Q remains OFF

For the three modes of operation, the key waveform is as shown in the Fig12.

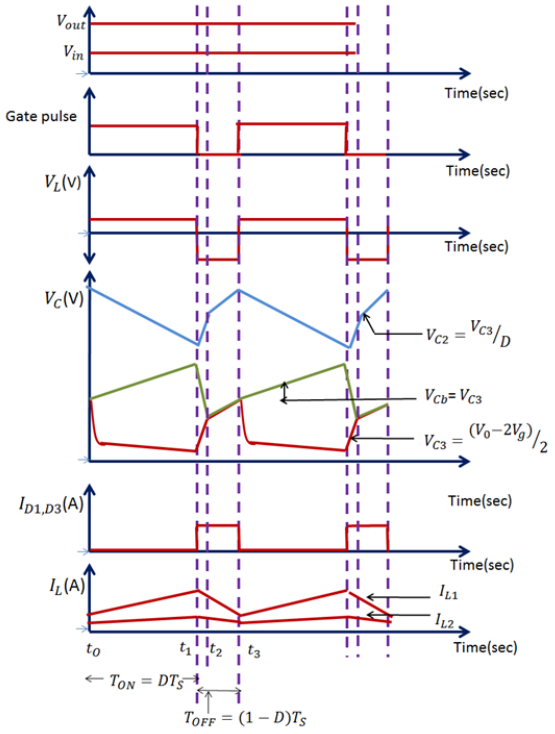

Fig.12. Model graph of TIESC-SC Converter

C. Gain Expression for TIESC-SC Converter

Similar to elementary dc-dc converter the output of TIESC-SC converter can be regulated using the duty cycle, and the output voltage is determined by the voltage induced in each SCs. The output voltage of the circuit will be the sum of the voltages of C_1, C_2, C_3 and source.

$$V_{C1} = V_{C3} = V_{Cb} = \frac{V_g \times D}{(1-D)} \quad \text{.....(6)}$$

$$V_{C2} = \frac{V_g}{(1-D)} \quad \text{..... ....(7)}$$

Hence the expression for voltage gain of the TIESC-SC converter is given by,

$$M = M_{C1} + M_{C2} + M_{C3} + M_{V_g} \quad \text{.....(8)}$$

$$M = \frac{D}{1-D} + \frac{1}{1-D} + \frac{D}{1-D} + 1 \quad \text{.....(9)}$$

$$M = \frac{2+D}{1-D} \quad \text{..... ....(10)}$$

The voltage gain of TIESC-SC based converter configuration can be further increased by extending the circuit. This can be obtained by adding more SCs into the circuit with multiple inductor energy storage cells to replenish the added SCs. Since SCs are added across an inductor, the voltage gain of D/(1-D) is obtained in addition; with the insertion of each SC. Thus we can infer that when number of inductors in the circuit are n, number of added SCs will be (n-1) with voltage gain of each SC equal to $V_g \times (D/(1-D))$.

D. Design of parameters

1. Switched Capacitors C_1, C_2 and C_3

At the switching frequency, small voltage ripples exist in the capacitors. When the switch is in ON position, sum of voltages of SCs and the voltage source becomes slightly more than the output voltage. Since the SCs C_1, C_2 and C_3 act as the voltage source, they along with the voltage source in series together contribute to the output voltage. Voltage difference which adds to the ESR of the capacitor contributes to a large pulsating current. Hence the voltage ripple should be minimized. The average current that C_1, C_2 and C_3 deliver to the load when switch is ON is I_o. Thus the ripples present in each SC is given by

$$\Delta V_{C1} = \frac{I_o \times T_S}{C_1} \quad \text{.....(11)}$$

$$V_{C1} = V_{C3} = V_{Cb} \quad \text{.....(12)}$$

$$\Delta V_{C2} = \frac{I_o \times T_S \times D}{C_2} \quad \text{.....(13)}$$

Here voltage ripple is selected as 0.1% of the output voltage.

2. Inductors L_1 and L_2

Current ripple is high when input voltage is low since input current increases. We take $\Delta I_L = 20\% \times I_{in}$. The average inductor current is largest when $V_g = 9V$ which equals 4A. Thus, $\Delta I_L = 0.8Amps$. The expression for ripple current is given by the equation

$$\Delta i_L = \frac{V_g D T_S}{L} = \frac{V_o (1-D) D T_S}{(2+D) L} \quad \text{.....(14)}$$

When D=0.5 the current ripple reaches its maximum value.

3. Output filter Capacitors C_f

Consider that the output of TIESC-SC converter is connected to the input of single phase inverter. The value of output capacitor should be very large such that ac component of the output voltage passes through it and the output voltage is maintained at the switch off period of the TIESC-SC converter. Voltage ripple is taken as 0.1% of the output voltage. The capacitance value is given by the formula

$$C_f = \frac{P_o}{(2\pi f_L)\Delta V_o \times V_o} \quad \text{.....(15)}$$

Where f_L=50Hz

III. SIMULATION STUDIES AND RESULTS

The validity of TIESC-SC converter is being verified using computer-aided simulations in MATLAB/Simulink platform. Based on the parameter design done in the previous section, TIESC-SC converter component values have been calculated to produce 35 W power by boosting a 9-15 V input voltage to a 60V output voltage at a switching frequency of 20 kHz. Table 1 tabulate the specification of components used.

Table 1: Design Values of TIESC-SC Converter

Parameter	Values
DC input voltage	10-15V
DC output voltage	60V
Power rating	35W
Switching frequency	20kHZ
Inductor L1, L2	517µH
Capacitors C2	10µF
Capacitors C1, C3,Cb	23µF
Output Capacitor C_f	3270µF
Resistor, R	100 ohms

Similarly other conventional topologies such as simple boost, TIBC, TIBC II and SIESC-SC converter topologies have been designed for same power and voltage ratings. Voltage stress, efficiency and output voltage of TIESC-SC converter is compared with that of conventional topologies. The voltage stress across the switch of each converter is being tabulated in Table 2. The graphical representation of efficiencies and output voltages are being plotted in Fig 13 and Fig 14 respectively.

Table 2: Voltage stress comparison

Converter topologies	Voltage gain (M)	Duty Ratio	Voltage stress values
Simple Boost	1/(1-D)	0.8	60
TIBC	(1+D)/(1-D)	0.667	36
TIBC II	(3-D)/(1-D)	0.5	24
SIESC-SC	2/(1-D)	0.6	30
TIESC-SC	(2+D)/(1-D)	0.5	22.5

It is being found that voltage stress drastically decreases for high voltage gain in TIESC-SC converter to less than 37% of the output voltage. Also since the duty ratio of TIESC-SC converter is lesser than others for same output voltage, current ripple and the turn off current of the switch is lower. This results in low conduction and switching losses thereby increasing the efficiency. The output voltage levels are high for different duty ratios in the proposed converter when compared to other conventional topologies.

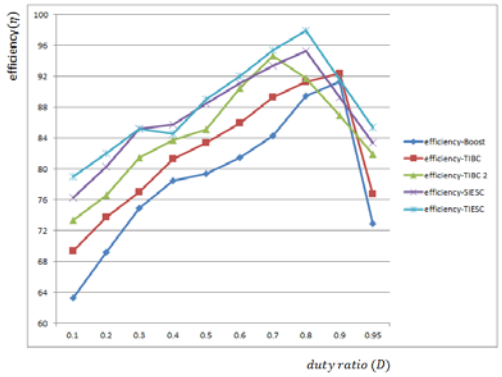

Fig.13. Efficiency Comparison

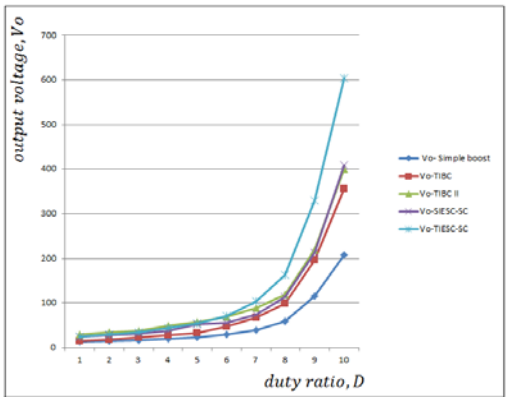

Fig.14. Output Voltage Comparison

Thus, TIESC-SC converter have been analysed further to study its transient behavior. The SIMULINK block diagram of the above designed TIESC-SC converter is shown in Fig.15.

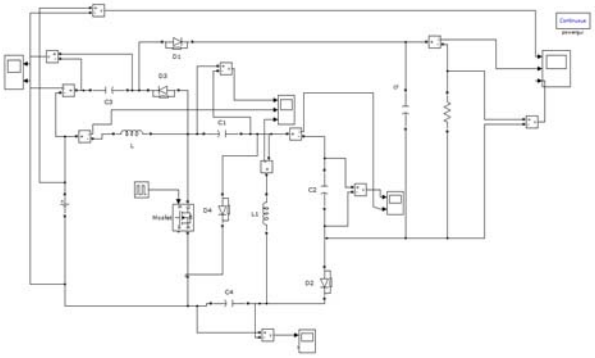

Fig.15. SIMULINK block diagram of the TIESC-SC converter

Fig 16 shows the output current and voltage waveforms of TIESC-SC converter. It has been found that when a 12 V input supply is given, then TIESC-SC converter produces a 60 V at the output.

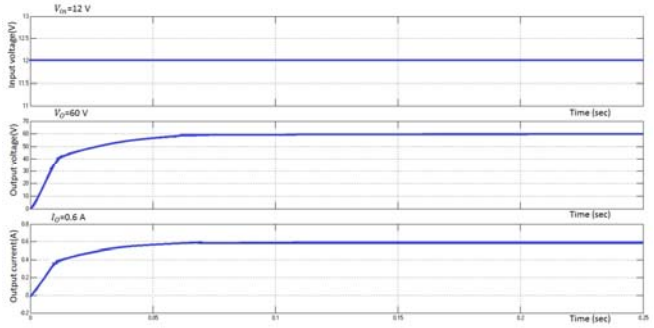

Fig.16. TIESC-SC converter output

Fig 17 shows the voltage across the switched capacitors and Fig 18 gives the current through output diode, D_1 and the switch. It is being found that the capacitor voltages are same as that of the theoretical values obtained.

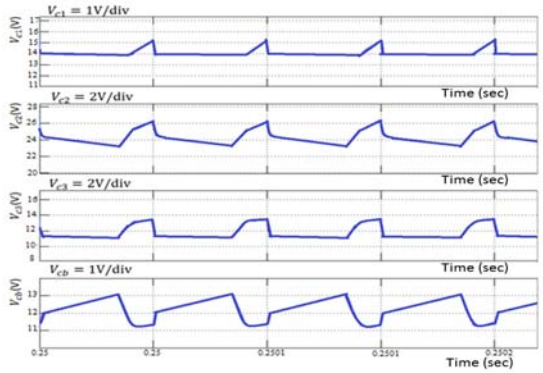

Fig.17. TIESC-SC ConverterVoltage waveforms-V_{C1}, V_{C2}, V_{C3} and V_{Cb}

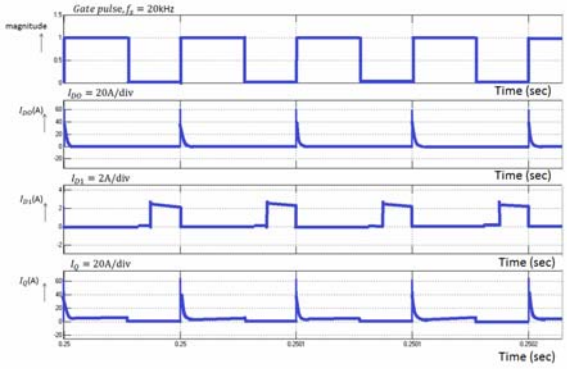

Fig.18. TIESC-SC ConverterCurrent waveforms-Gate pulse, I_{Do}, I_{D1} and I_Q

It can be seen from the figure that I_{Do} and I_Q currents have high spikes upto 60 Amps at each switching cycle and this increases the switching losses which eventually affects the converter efficiency. This can be alleviated by adding a snubber inductor in series with the switch on its drain side. By allowing a 3V voltage drop across the inductor, the rate of change of current can be reduced to 8 amps such that it is allowable by the switch. This can be achieved by taking inductor value as 1.05µH. This can be obtained as follows.

$$V_L = L\frac{dI}{dt} \quad \text{.....(16)}$$

$$L = \frac{3\times 3.5\times 10^{-6}}{10} = 1.05\mu H \quad \text{.....(17)}$$

After adding an inductor of 1.05µH, the current waveform of the circuit is as shown in the Fig 19. It is being found that the current spike through the output diode and so through the switch has been decreased to allowable value. The output voltage waveform without and with inductor is being compared and it is being found that for the same duty ratio, the output voltage is being increased from 60 V to 62.3V.

For every change in load or input voltage there arise variations in the output voltage. Thus a closed loop feedback control is being done in the MATLAB/simulimk platform and is as shown in the Fig 20.

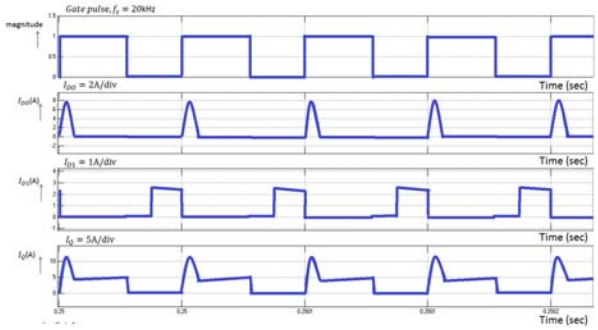

Fig.19. TIESC-SC Converter Current waveforms with Snubber Inductor- Gate pulse, I_{Do}, I_{D1} and I_Q

A negative feedback control is being done with proportional integral block. Here the output voltage is taken and is compared with the desired value to produce an error in case of change in output voltage. This error is then processed in the PI controller, where, the voltage error produced is used for the generation of PWM signal by comparing it with the oscillator ramp signal.

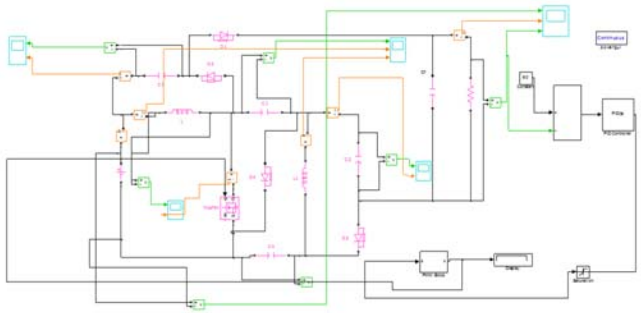

Fig.20. Closed Loop Control Strategy of TIESC-SC Converter

The value of P is taken as 1 and that of I is taken as 0.001.

IV. HARDWARE IMPLEMENTATION

Simulation studies have been experimentally verified by building a prototype model. The proposed converter is being tested in the laboratory and a desired output is obtained when tested with and without the snubber inductor. A square pulse of 20 KHz frequency is obtained using PIC 16F877A microcontroller.

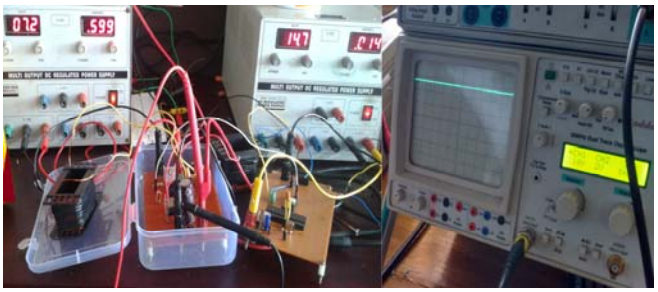

Fig.21. Closed Loop Control Strategy of TIESC-SC Converter

The circuit was implemented in PCB. With the result obtained, the prototype model has been found to be working as per the conditions needed with some losses which occured due to high frequency switching and due to the component parameters. When 7 V is given in the input, an output of 28 V is obtained. The losses can be reduced by decreasing the switching current spikes which can be achieved by incorporating an inductor in series with the drain side of the switch. TIESC-SC converter with snubber inductor has also been tested in the laboratory and the setup is as shown in the Fig 22. Here it can be seen that the voltage gain has been increased drastically upto the desired limit for same duty ratio when compared to the TIESC-SC converter without a snubber inductor. The rise of current has also been limitted to less than 10 amps as per the simulation studies. Thus, when considering simulation results along with the experimental results, it can be inferred that the voltage gain for TIESC-SC converter has been increased for same duty ratio when snubber inductor is being added due to the decrease in current spike through the switch. Efficiency has also being compared for TIESC-SC converter with and without the snubber inductor and it is being found that the switching stress due to current spike can be decreased without compromising the efficiency of the circuit.

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Fig.22. Complete Hardware Setup of TIESC-SC Converter (a). without snubber inductor (b). with snubber inductor

The output obtained is a dc voltage with desired level of accuracy for a given duty ratio and so the feasibility of the high gain dc-dc converter topology is confirmed for the use in high voltage applications. The voltages across each parameter is verified with that of theoretical and simulation results and are found to be similar. Further it has been found that, when an inductor is placed in series with the switch, the performance of the converter can be further increased in a better way. From the experimental results it can be inferred that the hardware setup is working and produces the desired output.

V. CONCLUSION

The merits of switched capacitors and the simple boost converter have been incorporated in a single circuit. High boost conversion ratio has been achieved with relatively less duty cycle and with small size when compared to conventional topologies. It also decreases the voltage stress across the switch. But the switching losses were high due to the current spikes through the switch. It has been rectified with the addition of a snubber inductor in series with the drain side of the switch. The inductor value is so small such that it does not affect the

circuit operation of the TIESC-SC converter. Thus an optimized converter topology has been designed. Further a voltage control mode feedback voltage regulation has been implemented in this circuit.

In this thesis work, TIESC-SC converter has been designed and has been done and a detailed analysis were carried out in MATLAB/simulink platform. A prototype model has been developed in the laboratory. The results obtained from the prototype model were satisfactory with the theoretical values.

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