DESIGN OF AREA EFFICIENT HIGH THROUGHPUT PIPELINED VITERBI DECODER FOR WIRELESS APPLICATION

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Abstract

In many wireless communication systems the used of pipelined VSLI architecture for virerbi decoder gives good error control performance viterbi decoder convolution and encoder .The viterbi algorithms used for decoding the convolution codes to propose the pipelined vietrbi decoder and convolution encoder is in field programmable gate array. This architecture is able of achieving high throughput in area efficient way. Hence it necessary for large constraint length and high throughput rate. By increasing the basic process elements the throughput can be linearly increases. The add compare select (ACS) units and its sub circuits of the viterbi decoder and trace back units have been operated in pipelined way to meet high throughput rate. By analysis the algorithm of viterbi decoder, it explores a practical method to design a pipelined processing of viterbi decoder.

Index Terms: convolutional encoder, viterbi encoder, viterbi algorithm, FPGA, pipelining.

I. INTRODUCTION

The convolutional coding in communication system has been used with the help of deep space and wireless communications. It is an alternative to block codes for the transmission over a noisy channel. In IS-95 and wireless digital cellular normal for CDMA (code division multiple access) also in employs convolution coding. In the Viterbi decoding algorithm, proposed Viterbi in 1967, is a decoding process for convolution codes in memory-less noise. This algorithm can be applied to a problems met in the design of communication systems.

This Viterbi decoding algorithm gives both a most likelihood and a most from effects to causes; reasoning based on past experience algorithm. A maximum from effects to causes; reasoning based on past experience algorithm identifies a code word that maximizes the conditional chance of the decoded code word against the received code word and most likelihood algorithms identifies and show a code word that maximize the conditional prospect of the received code word against the decoded code word. The same result by algorithms gives when the source information has a uniform distribution. Traditionally, In VLSI design there are the two most important concerns i.e., performance and silicon area. Recently, there is also important concern in battery power application power dissipation, such as laptop, computers, pagers and cellular phones. Power dissipation having two categories first dynamic power dissipation and second static power dissipation.

1.1 Viterbi decoder architecture

In the organization of convolution encoder and Viterbi decoder more than a few important design issues have also been discussed such as, branch metric unit addition method, the design

of add compare select, parallel unit of trace back and decoder. An ordinary Viterbi decoder is usually collected of five blocks, as shown in the Fig. 1.

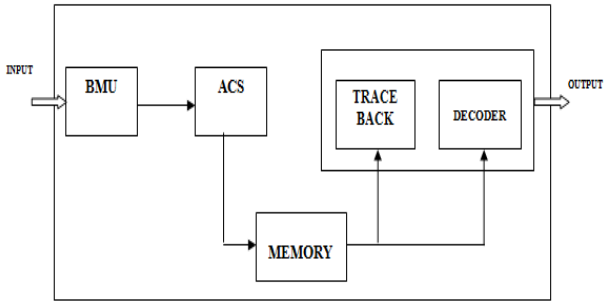

Fig . 1. Viterbi decoder architecture.

BMU (Branch Metric Unit) –It receive the input signals and balance the peculiarity between the expected values and input signals and lastly gives the results to the Add Compare Select. [1], [6]

ACS (Add Compare Select) – ACS completes the survivor paths and create the decision vector. In this unit there are two comparers, and these two comparers are precisely parallel. The one is used for comparing data bit and the other is used for comparing signal bits. The benefit of this design is to dropping the circuit timing delay. [1], [6]

MEMOEY- MEMORY is cycle used for discount the survivor paths. The core unit of this design is the TB (Trace Back) and DECODER, which include two role modules. The one is TB that read the information of the survivor paths in the MEMORY and other is DECODER that computes the output results. These two modules are working simultaneously in different MEMORY addresses. In this way, the Viterbi decoder is more competent than a normal one because the DECODER do not need to wait TB. [1], [6]

II. LITERATURE REVIEW

In this paper a modified Viterbi algorithm has been accessible for a Wi-Fi receiver. It shows that plan goes ahead associated with the modified Viterbi decoder implementation by implementing Xilinx tool in verilog design. An implementation on Field Programmable Gate Arrays (FPGA) gives user litheness to a lowering the rate and programmable solutions. [1]

In this paper proposes an execution on the CSA which optimizes Viterbi decoder circuits. CSA gives first relationship method for path metric calculation and compact at circuit Hamming space calculation. The power utilization up to 10% is improves by using CSA module with respect to the total area of the circuit. The counter output is compared with number of input bits for error minimization in CSA module. With the help of this CSA module experimental results explain that the planned CSA module decreases nearly 10% refers to the power consumption. [2]

For Viterbi decoders employ T-algorithm the author proposed a pre-computation plan with associated hardware architecture. Compared with existing schemes that target at capable implementation of T algorithm, the proposed approach is more dependable in general. The analysis of the critical path reveals that the pre-computation scheme can achieve the iteration bound for Viterbi decoders employing T-algorithm with insignificant hardware overhead. [3]

In this paper shows three objectives. Firstly, to design and simulated an orthodox Viterbi decoder is used. For quicker process application the Gate Diffused Input Logic (GDIL) based Viterbi decoder is designed using simulated, Xilinx ISE and synthesize effectively. The new projected GDIL Viterbi gives short power simulation results with very fewer path delays. Secondly, the GDIL Viterbi decoder is ones again compared with our planned technique, which comprises a Survivor Path Unit (SPU) implements a trace back method with DRAM. This intended approach of incorporating DRAM provisions the path information in a way which allows fast read access without requiring physical partition of the DRAM. This leads to a comprehensive gain in pace with low power things. Thirdly, all the viterbi decoders are compared, simulated, synthesized and the proposed approach shows the most excellent simulation and synthesizes outcome for high speed application and low power in VLSI design. [4]

III. CONVOLUTION ENCODER

Convolution encoder is takes input data bits and gives out of two bits. It also combines the fixed number of input bits. The input bits are

stored in fixed length of shift register and they merge with mod – 2 adders which are implemented with a XOR gate. Convolution encoding is also process of adding redundancy to signal bit of stream and it is equivalent to binary convolution.

The theory is illustrated with help of above example. When the message bit is shifted to place "S" as shown in Figure. 2, the new values of V1 and V2 are generated depending upon S0, S1, and S2. S1 and S2 store the earlier two message bits. The current bit is present in S0. so, equation becomes, V1= S0 XOR S2, and V2= (S0 XOR S1) XOR S2

The output switch first samples V1 and then V2. The shift register then shifts contents of S1 to S2 and contents of S0 to S1. Next response bit is then taken and stored in S0. Again V1 and V2 are generated according to this new arrangement of S0, S1, and S2. The output switch samples V1 and V2. For every input message bit two encoded output bits are transmitted with V1 and V2. Number of message bits k=1, for n=2 Number of encoded output bits for one message bit.

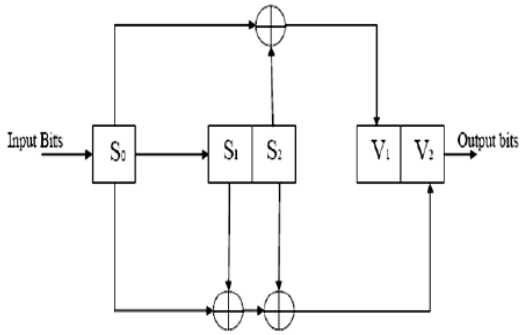

Fig . 2. The Rate 1/2 convolution encoder.

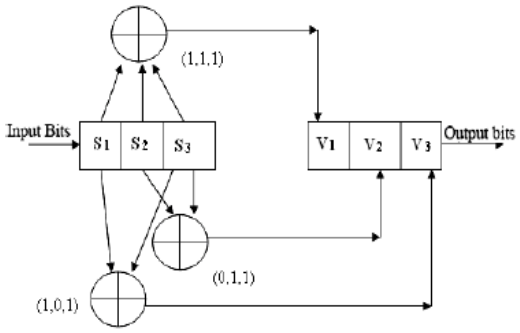

Fig . 3. The Rate 1/3 convolution encoder.

3.1 Branch metric unit (BMU)

Branch metric unit used for receive the input signals and compute the difference between the input signals and excepted values and output is goes to add compare select unit. According to the principle of convolution encoder, input is 1 bit to convolution encoder and output is 2 bit from convolution encoder and BMU unit is also used for count the number of differing bits. If both the applied input signals are different either (High / Low) or (Low / High) then the output signals of EXOR gate is High and both the applied input signals is same then the output signals of EXOR gate shows Low. In pipeline scheme can be easily applied for branch metric calculation to achieve enough high speed because in branch metric module no feedback loop exist. BMU implementation can be simplified by

bm (x , y, z) = -bm ($\bar{x}$, $\bar{y}$, $\bar{z}$)

Therefore only half unit of BMU to be generated then ACS unit is used in that block for add and subtract the branch metric.

Bm (0, 0, 0) = (-A -B -C)
Bm (0, 0, 1) = (-A –B +C)
Bm (0, 1, 0) = (-A +B -C)
Bm (0, 1, 1) = (-A +B +C)

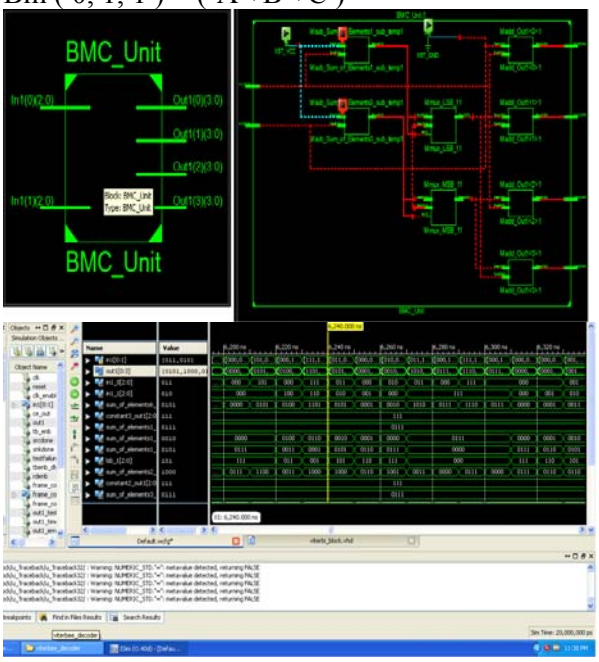

Fig . 4. BMU RTL schematic and wave form.

3.2 Add compare unit (ACS)

ACS unit is used for complete the survivor path and generate the decision vector. It consists of two compares and these are parallel with each other. One is used for comparing the signal bit and other is used for comparing the data bits. The merit of this design the ACS unit is reducing the circuit timing delay and this block is same part of memory. This is used for saving the survivor

path. This unit also consists of two full adders and one half adders. Output of branch metric unit is added with the previous path metric and to give output is the new path metric for the next branch metric. For ACS unit assuming a VD with 64 states (constraint length of 7).

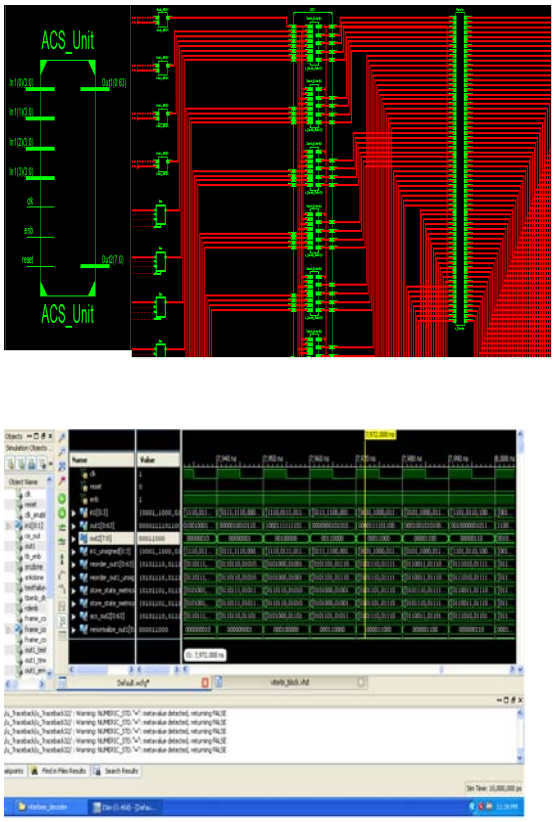

Fig . 5. ACS RTL schematic and wave form.

3.3 Trace back unit (TBU)

The trace back unit is a bank of registers, which record the survivor path of each state by ACS unit to design the system it has core unit of trace back (TB) and decoder it has two functions modules. Trace back unit is used for read the information of the survivor path in the memory and decoder is used for computes the output results. This modules work simultaneously but different memory address. Survivor path lengths 64 in memory space are divided into four blocks and the capacity of each block is 60. A register is assigned to each state and the length of register equal to the frame lengths. The corrected output sequence is produce by the decision vector. The trace back unit is used for them to decide final output.

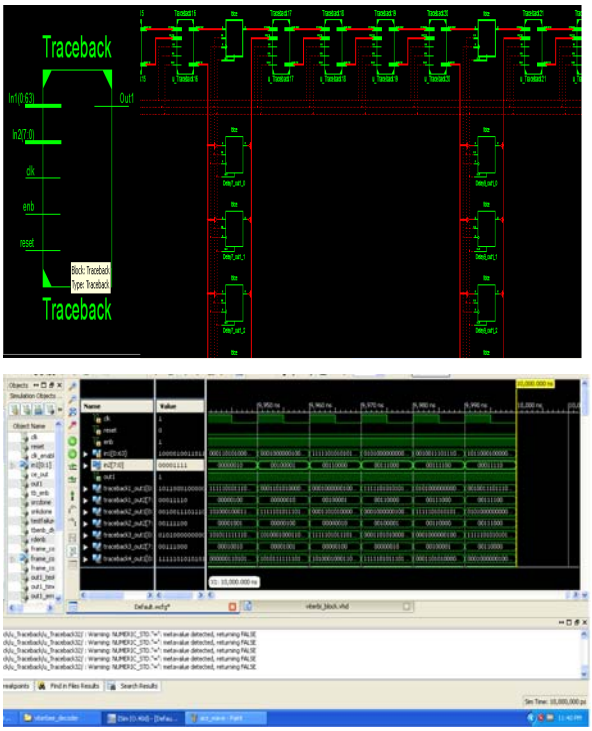

Fig . 6. TBU RTL schematic and wave form.

IV. CONCLUSION

Viterbi decoder is very important block in CDMA or wireless system. This paper has design and implemented convolution encoder and Viterbi decoder targeting FPGA implementation. The aim of this paper was to expand a pipeline processing in trace back and decoder memory unit and in this way we can show area efficient and to reduce power.

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