QUADRATIC BOOST DERIVED HYBRID CONVERTER WITH SIMULTANEOUS AC AND DC OUTPUTS

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Abstract— The Quadratic boost derived hybrid converter (QBDHC) is a new hybrid converter topology which can supply simultaneously both AC as well as DC from a single DC source. The new hybrid Converter is derived from the single switch controlled quadratic boost converter by replacing the controlled switch with voltage source inverter (VSI). This new hybrid converter has the advantages like reduced number of switches as compared with conventional design having separate converter for supplying AC and DC loads and provide DC and AC outputs with an increased reliability resulting from the inherent shoot through protection in the inverter stage. Such multioutput converters with better power processing density and reliability can be well suited for systems with simultaneous dc and ac loads, e.g, nanogrids in residential applications. For controlling the switches, PWM control based upon unipolar sinusoidal PWM is used.

Keywords—Boost converter, Quadratic boost converter, Nanogrid, Pulse width modulated inverters.

I. INTRODUCTION

Micro grid [1] is a small autonomous system formed by integrating various distributed energy sources like solar, wind, fuel cells, biomass etc. The architectures are being increasingly incorporated in modern smart residential electrical power systems. These systems involve different load types - dc as well as ac which are efficiently interfaced with different kinds of energy sources (conventional or non conventional) using power electronic converters. Fig. 1 shows the schematic of a system, where a single dc source V_{dcin} (e.g., solar panel, battery, fuel cell, etc.) supplies both dc V_{dcout} and ac V_{acout} loads.

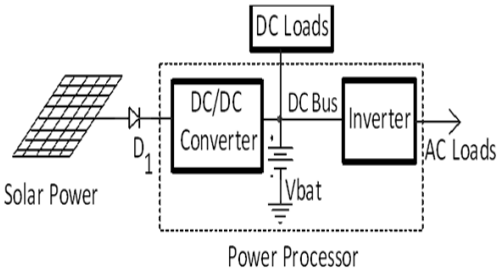


Fig.1.The architecture of a solar micro grid [1]

There are several DC-DC converter configurations [2] were already proposed such as Buck, Boost, Buck-Boost, SEPIC, CUK, etc. Boost and Buck converter configurations can increase and decrease the output voltages respectively, while the other converters can perform both functions. A DC-DC converter with a high voltage gain is desirable in many modern residential applications. Generally,

when there is a need to step up a DC voltage, a boost converter is usually chosen. To achieve a high voltage gain, the duty cycle of the power switch of the boost converter must be large, resulting in high conduction losses and degrading the converters efficiency. Inverter section may be either voltage sourced or current sourced. Voltage source inverters are commonly preferred in micro grid applications.

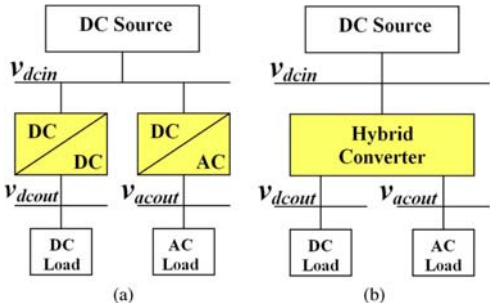


Fig.2.The architectures used for getting simultaneous outputs from single input

The architectures of Fig. 2 show the converter schemes with simultaneous ac and dc output from a single dc input [3]. Fig. 2(a) uses separate power converters for each conversion type (dc to dc and dc to ac) while Fig 2(b) utilizes a single power converter stage to perform both the conversions. The latter converter, referred to as a hybrid converter which has higher power processing density and improved reliability (resulting from the inherent shoot-through protection capability). These qualities make them suitable for use in compact systems with both dc and ac loads.

Smart residential systems are often connected to non conventional energy sources to provide cleaner energy. Due to space constraints, these dedicated energy sources are highly localized and have low terminal voltage and power ratings (typically, on the order of a hundred watts). Conventional designs involves two separate converters to power residential loads ,a dc-dc converter and a voltage source inverter (VSI) [4]connected either in parallel or cascaded manner and supplying dc and ac loads separately. Depending on the requirements, topologies requiring higher gains may be required to achieve step up operation. In PWM (square-wave) dc-to-dc converter topologies, dc conversion ratio M is a function of duty ratio D of the active (transistor) switch. Both minimum and maximum attainable conversion ratios are limited in practical converters. M_{max} is limited by the degradation in efficiency as duty ratio D approaches 1. On the lower end, minimum ON-time of the transistor switch results in a minimum attainable duty ratio and consequently in a minimum conversion ratio.

Conversion range can be extended significantly if conversion ratio M has a quadratic dependence on duty-cycle. In this work, a quadratic converter with simultaneous ac and dc output (QBDHC) is introduced. The converter possesses less number of switches and better conversion range than the conventional converters. A unipolar PWM technique is used for control pulse generation, so that it reduces the THD in output voltage. To verify the validity of the proposed approach, computer-aided simulations are performed using MATLAB/SIMULINK. Also an experimental prototype is made to confirm the feasibility of the circuit.

II. PROPOSED QBDHC CONVERTER

A. *Quadratic Boost Converter*

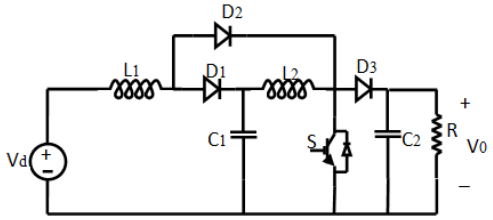


Fig.3. Circuit configuration of quadratic boost converter

The circuit diagram of a quadratic boost converter [5] is shown in Fig 3. The circuit comprises of a single power MOSFET switch, S, two diodes, D1 and D2, two capacitors, C1 and C2, two inductors L1 and L2 and a load resistor. Compared to conventional boost converter the conversion ratio M has the quadratic dependence with the duty ratio. Hence the expression for duty ratio can be derived as relation (1).

$$\frac{V_{dcout}}{V_{dcin}} = \frac{1}{(1-D)^2} \qquad (1)$$

B. *Derivation of QBDHC topology*

The QBDHC topology is derived by replacing control switch 'S' of quadratic boost converter by a voltage source inverter and a LCL filter. The resulting circuit diagram is shown in Fig.4. The proposed converter provides simultaneous AC and DC output from

a single DC input with better conversion range. The four control switch (Q_1-Q_4) controls both AC and DC outputs. The boost operation of the proposed converter can be realized by turning on both switches of any particular leg (either Q_1-Q_4) or (Q_3-Q_2) simultaneously. This is equivalent to shoot-through switching condition as far as VSI operation is concerned, and it is strictly forbidden in the case of a conventional VSI. The QBDHC, during inverter operation has the same circuit states as a conventional VSI. For conventional VSIs the input dc voltage is required only during the power intervals, i.e., when there is a power transfer with the source.

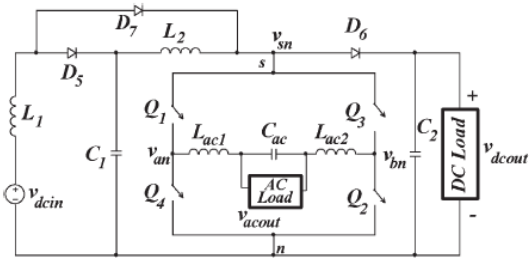


Fig.4. Circuit configuration of quadratic boost derived hybrid

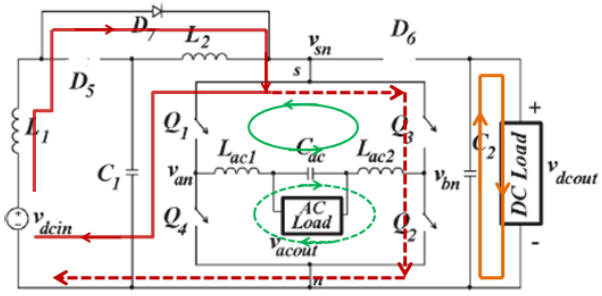
Converter

In the other intervals, the current freewheels among the inverter switches and these states do not require the input to be at a fixed dc value and hence can be zero. In the QBDHC, the switch node voltage (V_{sn}) acts as the input to the inverter; it switches between the voltage levels V_{dcout} and zero. The switching scheme should ensure that the interval for power transfer with the source occurs only when V_{sn} is positive, i.e., when V_{sn} clamped to the dc output voltage V_{dcout}.

C. *Modes of operations*

The QBDHC has three distinct switching intervals as described in the following.

Interval I-Shoot-through interval: The equivalent circuit schematic of the QBDHC during the shoot-through interval is shown in Fig.5 The shoot-through interval occurs when either Q1-Q4 or Q3-Q2 of any particular leg are turned ON at the same time. The duration of the shoot-through interval decides the boost converter duty cycle (D). In addition to turning on of the switches in the same leg, a switch from the opposite leg is also made in ON state. So inverter output current circulates within the bridge network switches.



, Fig.5. Equivalent circuits and current directions of the QBDHC during

shoot-through interval

Interval II-Power interval: During this interval, the ac output receives power from the source. The power interval, shown in Fig.6 occurs when the inverter current enters or leaves the bridge network at the switch node S. The diode D_5 and D_6 were conducts during this period, and the voltage at the switch node (V_{sn}) is equal to the V_{dcout}. In this interval, either Q_1-Q_2 or Q_3-Q_4 is turned ON. The inverter output V_{ab} will be equal to V_{dcout}, when Q_1 and Q2 are in on state and -V_{ab} when Q_3 and Q_4 is ON.

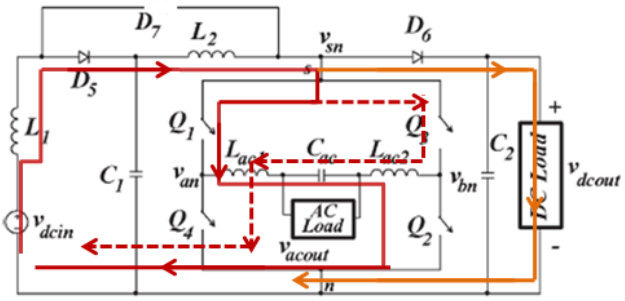


Fig.6. Equivalent circuits and current directions of the QBDHC during power interval

Interval III-Zero interval: The zero interval occurs when the inverter current circulates among the bridge network switches and is not sourced or sunk. During this interval, either all top or the bottom switches are ON. The current in the inductors is discharged through the load during the interval. The diode D_5 and D_6 were conducts during this period. Fig.7 shows the equivalent circuit for this interval.

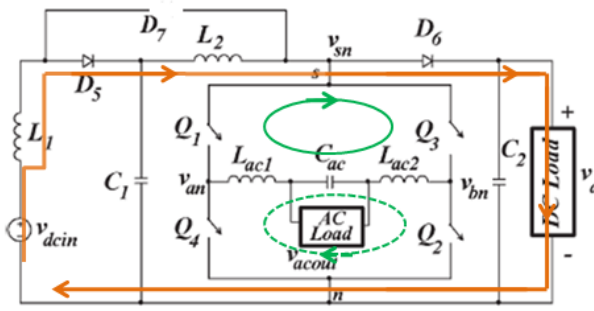


Fig.6. Equivalent circuits and current directions of the QBDHC during zero interval

D. *Gain Expression for AC and DC outputs*

Similar to conventional boost converters dc output of QBDHC can be regulated using the duty cycle, and it is determined by the shoot through state in a switching cycle. Hence the expression for voltage gain of dc output is given by,

$$\frac{V_{dcout}}{V_{dcin}} = \frac{1}{(1-D)^2} \quad \text{.....(1)}$$

The modulation index, denoted by M_a ($0 \le M_a \le 1$), regulates the ac output voltage of the QBDHC, and its definition is similar to that associated with conventional VSIs. The peak output ac voltage is related to the input as,

$$\frac{V_{acout}}{V_{dcin}} = \frac{M_a}{(1-D)^2} \quad \text{.....(2)}$$

As the same set of switches controls both the dc and ac outputs, there is limitation to the maximum duty cycle or modulation index that can be achieved for this topology. The switching strategy must satisfy the following constraint:

$$M_a + D \le 1 \quad \text{.....(3)}$$

Hence, the maximum value of ac gain is achieved at the equality condition of Eqn 3. At this condition, the peak value of the ac voltage is equal to the input voltage, and this is independent of the values of the duty cycle and modulation index. The expression for output dc (P_{dc}) as well as ac power (P_{ac}) can be derived as follows:

$$P_{dc} = \frac{V_{dcin}^{\ 2}}{R_{dc}(1-D)^4} \quad \text{.....(4)}$$

$$P_{ac} = 0.5 \times \frac{V_{dcin}^{\ 2} \times M_a^{\ 2}}{R_{ac}(1-D)^4} \quad \text{.....(5)}$$

E. *Control Scheme for QBDHC*

The PWM control scheme for the QBDHC is shown in Fig 7. In this scheme, the shoot-through is realized by gating-ON both the switches of a single leg at the same time. The switching strategy involves turning on only one leg at a time in order to achieve shoot-through. The reference signals to the PWM generation circuit are $V_m(t)$ and V_{ST} (t). The signals S_1-S_4 are provided to the gates of the controlled switches.V_{ST} (t) is a dc signal, controls the shoot-through period, and hence, the duty ratio (D_{st}) for the dc output of the boost converter and $V_m(t)$ controls the modulation index (Ma) for the inverter. The nature of the gate signals for a positive value of reference signal $V_m(t)$ has been shown in Fig.7.

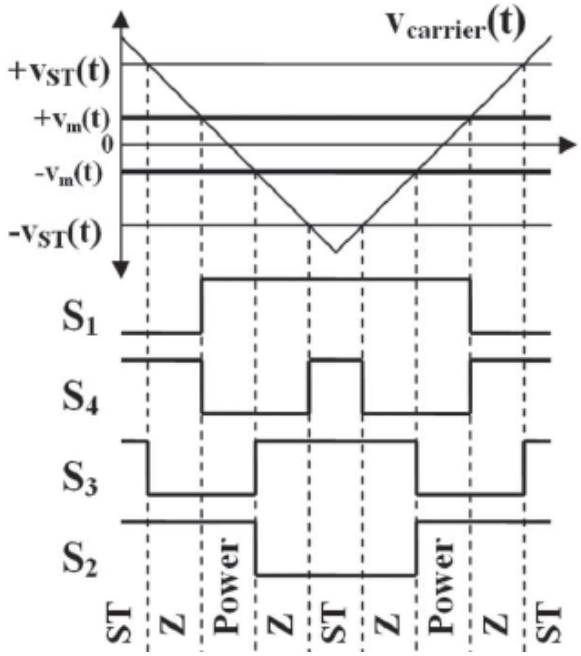


Fig.7. Proposed modified bipolar PWM control scheme for QBDHC

The maximum value of ac gain is achieved at the equality condition of Eqn.3. At this condition, the peak value of the ac voltage is equal to the input voltage, and this is independent of the values of the duty cycle and modulation index. The control parameters $V_m(t)$ and $V_{ST}(t)$ are generated by the control system and must satisfy Eqn.3. This switching strategy constraint is taken care of by the controller by satisfying the constraint given by the Eqn.6.

$$V_m \le |V_{ST}| \quad \text{.....(6)}$$

The digital implementation of the modified PWM scheme for the quadratic boost derived hybrid converter is shown in Fig.8.

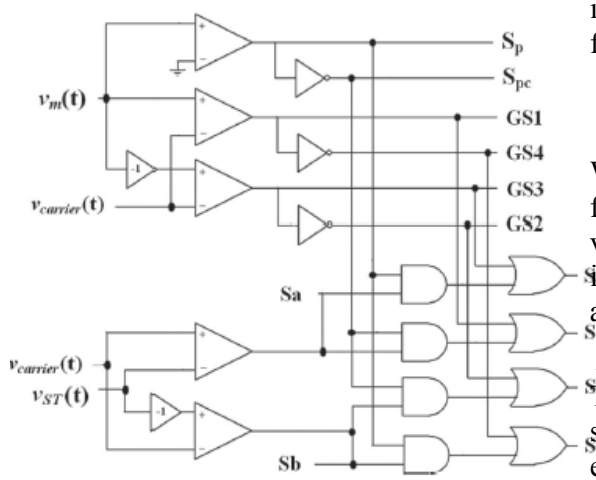


Fig.8. Digital implementation of the proposed modified PWM control scheme

F. Design of Passive Parameters

The ac output waveforms of the QBDHC are similar to those of a conventional VSI. Therefore, the filter design principles associated with the design of conventional VSIs can be used for Lac (= Lac1 + Lac2) and Cac.

$$C_{base} = \frac{1}{Z_{base} \times \omega_n} \text{.....(7)}$$

Where Z_{base} is the base impedance vale and ω_n is the natural frequency.

$$L_{ac} = \frac{V_{dcin}}{16 f_s \Delta I_{L\max}} \text{.....(8)}$$

Lowest ripple current in the output for a given inductance L and resonant frequency occurs at Lac1 = Lac2 . where ΔI_{Lmax} is the 25% current ripple The design of the filter capacity for a VSI proceeds from the fact that the maximal power factor variation acceptable by the grid is 3%. The filter capacity can therefore be calculated as a multiplication of system base capacitance.

$$C_{ac} = 0.03 \times C_{base} \text{.....(7)}$$

One of the major differences between the QBDHC and a conventional quadratic boost converter is that, in case of QBDHC, since both dc and ac outputs are achieved, the inductor currents and the capacitor voltages have both a high and a low-frequency components (at twice the output ac power frequency), in addition to their dc values. For the proposed converter, this instantaneous power balance is maintained by both the reactive elements (capacitors and inductors). Neglecting switching frequency components, the equations related to the instantaneous power balance can be written as follows.

$$v_{ab} = v_{an} - v_{bn} \text{.....(8)}$$

$$i_{ab} = \hat{i}_{ab} . \sin(\omega t - \Phi) \text{.....(9)}$$

Where □ is the phase difference between the fundamental components of inverter output voltage (v_{ab}) and current (i_{ab}). Therefore, the instantaneous inverter input power is expressed as Eqn.10

$$p_{ab} = 0.5\hat{v}_{ab}\hat{i}_{ab} . \cos\Phi - 0.5\hat{v}_{ab}\hat{i}_{ab} \cos(2\omega t - \Phi) \text{.....(10)}$$

The above expression has a dc as well as a sinusoidal component. The dc component is equal to the real power demanded by the ac output (Pac). Thus, the average input current of the inductor (L_1) can be calculated as,

$$I_{L1} = \frac{P_{dc} + P_{ac}}{V_{dcin}} \text{.....(11)}$$

The sinusoidal component of instantaneous power P_{ab} is balanced by the variation of the inductor current and the capacitor voltage. This results in a low-frequency ripple (at twice the power frequency) in the inductor current as well as the capacitor voltage. This power balance equation is written as

$$p_{ab} = \frac{d(0.5L_1 i_{L1}^{\ 2} + 0.5L_2 i_{L2}^{\ 2} + 0.5C_1 V_{C1}^{\ 2} + 0.5C_2 V_{dcout}^{\ 2})}{dt} \text{.....(12)}$$

The switches Q_1-Q_4 and Q_2-Q_3 are complementary in operation except during the shoot-through interval. The input to the inverter bridge equals to V_{dcout} during both power and zero intervals. Thus, the maximum stress on each switch is equal to V_{dcout} , the dc output voltage, neglecting the voltage drop across the conducting diodes. Thus, the selection of switch ratings is dependent upon the dc output voltage rather than the input voltage, contrary to the case for a conventional VSI. The expressions for the currents and voltages in different intervals are shown in Table 1, and the maximum current through the switches can be expressed as follows:

$$\hat{i}_{sw} = i_{L\max} + \left|\hat{i}_{ab}\right| \text{.....(13)}$$

Table 1: Steady state expressions of QBDHC

Interval	Shoot through State	Power Interval	Zero Interval
i_{D5}	0	i_{L1}	i_{L1}
i_{D7}	i_{L1}	0	0
i_{D6}	0	i_{L2}-$\|i_{ab}\|$	i_{L2}-$\|i_{ab}\|$
i_{C2}	-I_{dcout}	i_{D6}-I_{dcout}	i_{D6}-I_{dcout}
v_{ab}	0	$\pm V_{dcout}$	0
v_{sn}	0	V_{dcout}	V_{dcout}

III. SIMULATION STUDIES AND RESULTS

To verify the validity of the QBDHC, computer-aided simulations are carried out using MATLAB/SIMULINK. For the purpose of designing the passive components, the ripple contents (both high- and low-frequency components) in the inductor current and the capacitor voltage have been taken to be 20% and 3%, respectively at the rated power. Based on the equations derived on the previous section the components of QBDHC have been designed for D=0.4 and M_a=0.5. The parameter specifications of the designed QBDHC are given in Table 2. The SIMULINK block diagram of the above designed converter is shown in Fig.9.

Table 2: Design example specification of QBDHC (Open loop)

Parameter	Values
DC input voltage	10V
DC output voltage	27V
AC output voltage	13V_{rms}
Power rating	80W
Switching frequency	10kHZ
Inductor 1	64.8µH
Inductor 2	300µH
Capacitor 1	10µF
Capacitor 2	2.5mF
Filter Capacitor C_{ac}	20µF
Filter Inductor L_{ac}	150µH

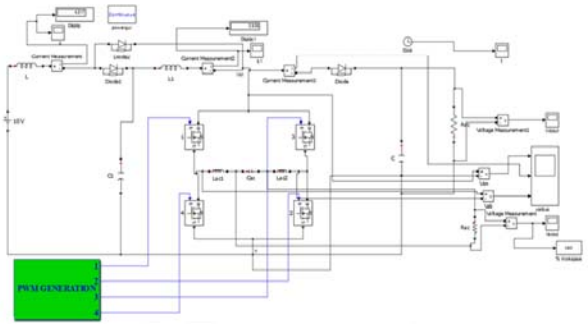


Fig.9. SIMULINK block diagram of the quadratic boost derived hybrid converter

The MATLAB implementation of the PWM unipolar control strategy is shown in Fig.10. In figure logical gates were used for getting the proposed unipolar PWM scheme.

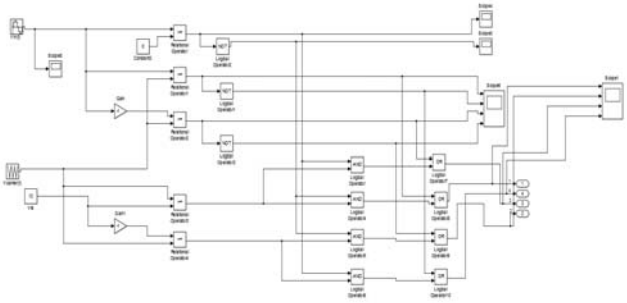


Fig.10. SIMULINK block diagram of the proposed unipolar PWM scheme

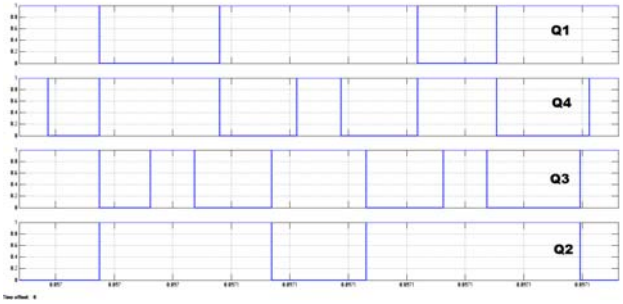


Fig.11. Control pulses for the switches

The control pulses for the switches Q_1, Q_4, Q_3 and Q_2 are shown in Fig.11. The control schematic described in previous section has been used for the generation of the gate signals. The waveforms validate that, whenever the switches Q_1 and Q_4 or Q_3 and Q_2 are on at the same time shoot through interval occurs and it controls the dc output.

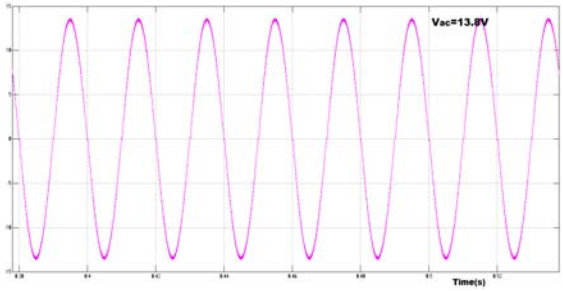


Fig.12. AC output waveform for D=0.4 and M_a=0.5

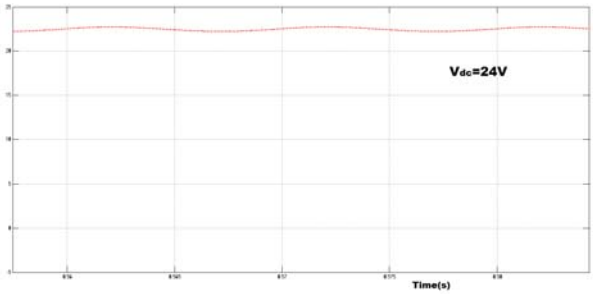


Fig.13. DC output waveform for D=0.4 and M_a=0.5

The ac output voltage and dc output voltages obtained for the QBDHC topology illustrated in Fig.12 and Fig.13 respectively. From the figures, for an input voltage of 10V, the dc output obtained is 24V and ac output as 13V, which is satisfactory with the theoretical values. The THD analysis of QBDHC for the designed values is shown in Fig.14. The THD results show that the circuit posses less harmonic components and designed filter components are accurate.

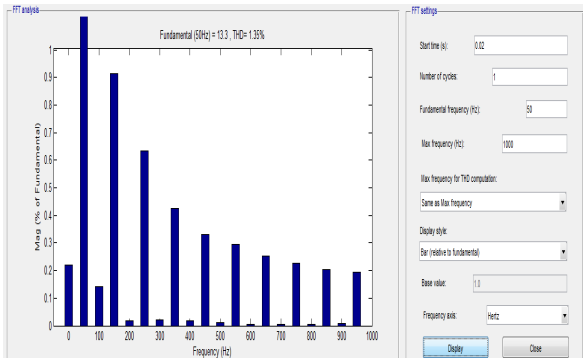


Fig.14. THD analysis of QBDHC for D=0.4 and M_a=0.5

The inverter output voltage waveform is shown in Fig.15. The V_{ab} takes values V_{dcout} when Q_1 and Q_2 is ON, and $-V_{dcout}$ when Q_3 and Q_4 is ON.

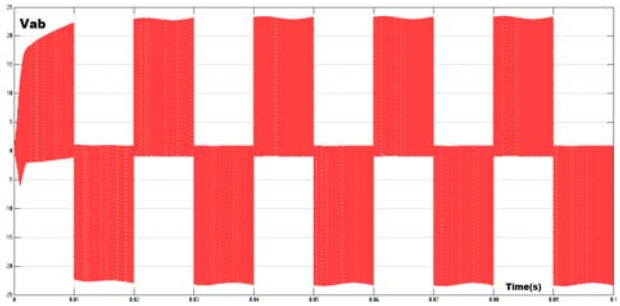


Fig.16. Simulation results for inverter output voltage of QBDHC

The input inductor current waveform i_{L1} is shown in Fig.17 as below; the waveform indicates that the obtained value is near to the designed value. For the QBDHC, the inductor current is drawn from a dc source, and hence, the ripple content in the input current should be as low as possible.

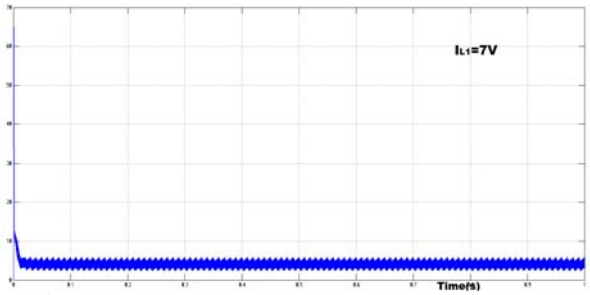


Fig.17. Simulation results for input inductor current of QBDHC

The power transfer takes place only if the switch node voltage V_{sn} is positive and equals to dc output voltage. The switch node voltage waveform of designed QBDHC is shown in Fig.18. The peak value equals to the dc output value. Here it is 24V.

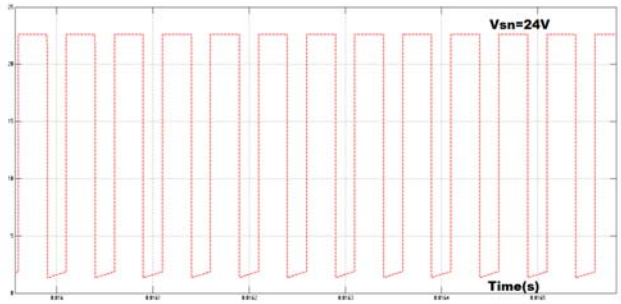


Fig.18. Simulation results for switched node voltage of QBDHC

IV. HARDWARE IMPLEMENTATION

The simulation results are verified experimentally by the hardware implementation.

The proposed converter is tested and an output is obtained. The PWM signals generated in MATLAB/SIMULINK is recreated by using a PIC 16F877A microcontroller. The prototype of QBDHC converter is modeled at 10 kHz.

Main parts of the system are as follows:

1. Power supply unit
2. PIC 16F877A microcontroller board
3. Gate Driver Circuit
4. Quadratic boost derived hybrid converter board

The power supply unit is used to generate regulated power supply. 7805 regulator IC is used to obtain +5 V output. A capacitor is used to eliminate ripples. An LED is connected to the circuit to check whether it is properly working.

PIC16F877A development board includes a microcontroller and a voltage regulator IC. PIC16F877A microcontroller is selected for providing PWM signal to the designed converter. PIC16F877A is general purpose microprocessor which has additional parts that allow them to control external devices. Basically, a microcontroller executes a user program which is loaded in its program memory. The gate pulses generated using the Microcontroller is having only a 5V magnitude. So in order to convert it into the required voltage level a gate driver circuit is required. Gate driver circuit used here uses a gate drive optocoupler TLP250 and resistors.

Complete hardware setup of the QBDHC circuit is shown below. In the figure. The gate signal from the PIC development board is fed to the power circuit via driver circuit.

Fig.25. Complete Hardware Setup of the QBDHC

The output voltage contains dc voltage with required level of accuracy and so the feasibility of the topology is confirmed. The hardware setup for the entire system is developed. From the experimental results it is clear that the hardware setup is working and produces the desired output.

V. CONCLUSION

The QBDHC is a modified boost derived hybrid converter topology which can produce ac and dc output simultaneously from a single DC input with better conversion ratio than previous topologies. The QBDHC topology posses some distinct advantages like inherent shoot through protection, no dead time compensation circuits were required, reduced number of switches, DC and AC outputs can be independently controlled, improved dynamics than cascaded designs and it can also be adapted to generate AC outputs at frequencies other than line frequencies by a suitable choice of the reference carrier waveform. In this thesis work detailed analysis of QBDHC was done and the designed circuits were simulated in MATLAB platform and a prototype model of 80W load is constructed. The results obtained from the prototype model were satisfactory with the theoretical values.

References

[1]. R. Adda, S. Mishra, and A. Joshi, "A PWM control strategy for switched boost inverter," Proceedings of Energy Conversion Congress and Exposition (ECCE), pp.991-996, November 2011

[2]. Ned Mohan, Tore M. Undeland, William P. Robbins., "Power electronics converter applications and design," Wiley press, page(s) 811, 2003.

[3]. Olive Ray,Santanu Mishra, "Boost-derived hybrid converter with simultaneous ac and dc outputs" IEEE transaction on industry applications,Vol.50,No.2, March 2014

[4]. P. S. Bimbhra."Power electronics," Khanna Publishers 4th edition, page(s) 755.

[5]. K.Tattiwong, C. Bunlaksananusorn, "Analysis Design and Experimental Verification of a Quadratic Boost Converter," Proceedings of TENCON IEEE Region 10 Conference 2014, Page(s): 1-6.