DESIGN AND ANALYSIS OF ZERO VOLTAGE TRANSITION FOR INTERLEAVED BOOST CONVERTER USING MATLAB/SIMULINK

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Abstract

This paper proposes a novel soft- switching Boost converter consists of two shunted an auxiliary inductor and boost conversion units . At zero voltage this converter is used to turn on both the active power switches to limit the switching losses and distinctly increase the conversion efficiency. Since the two shunted - operated elementary boost units are similar. The analysis and design for the Boost converter module becomes quite easy. A test circuit is analysed and simulated, and the circuit operation shows satisfactory result with the theoretical analysis. The experimental results of the simulated output of this converter module is effective and very well with the output efficiency as high as 95%.In high power application interleaved operation of two or more boost converter has been proposed to increase the output power. A detailed mode analysis of interleaved topology is presented. The interleaved topology used to decreases switching device current ratting since current in each phase is distributed
Keywords: Interleaved boost converter, Soft switching, Quasi resonant converter,Zero current Switching(ZCS), Zero voltage Switching(ZVS),

I . INTRODUCTION

Boost converters are popularly employed in equipments for different applications. For high-power-factor requirements, The main problem with these kinds of converters is that the voltage stresses on the power switches are too high in the resonant converters, especially for the high-input dc-voltage applications. An interleaved converter with a coupled winding is proposed to a provide a lossless clamp. Additional active switches are also appended to provide soft-switching characteristics. High level output power and low level output ripple obtained by these converter. This paper explains a soft-switching boost converter consists of interleaved shunted elementary boost conversion and auxiliary inductor. This converter is able to switch on both the active power switches at zero voltage to decrease their switching losses and rapidly increases the convertion efficiency therefore the two paralleloperated boost units are similar,analysis of operation and design for the converter module becomes simple.

II. .CIRCUIT CONFIGURATION

Fig. 1 Shows the proposed soft-switching converter module. Inductor L1 , MOSFET active switch S1, and diode D1 comprise one step-up conversion unit, while the components with subscript "2" form the other conversion unit .LS is shunted with the two active MOSFET switches to release the electric charge stored within the output capacitor Cs prior to the turn-ON to fulfil zero-voltage turn- ON (ZVS), and therefore, raises the converter efficiency. To calculate the parameters L1,L2, and C0 are replaced by voltage and current sources..

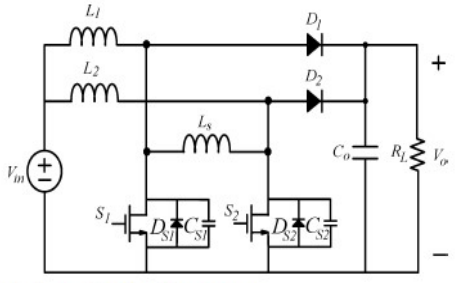


Fig. 1. Proposed interleaved boost converter.

III .CIRCUT OPERATION ANALYSIS

Before analysis on the circuit, the following assumptions are presumed.

1. The value capacitor output C0 is more ,so it is necessary to neglect the output voltage ripple.
2. The MOSFET voltage drop on switches S1,S2, and diodes D1, and D2, are neglected.
3. InductorsL1, and L2 have large inductance, and their currents are identical constants, i.e.,IL1=IL2=IL
4 The value of Output of the capacitances of switches CS1, and CS2 , i.e.,CS1=CS2=CS

The two active switches S1 and S2 are operated with pulse width-modulation (PWM) control signals. They are gated with identical frequencies and duty ratios.. The rising edges of the two gating signals are separated apart for half a switching cycle.

A.MODE-1.

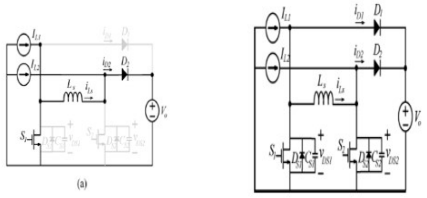


Fig. 2. Simplified circuit diagram.

When the two gating signals are separated for half a switching cycle.At this mode, the gating signal for switch S2 has transmitted to low state and the voltage VDS2 increases toV0 at t0 . At the beginning of this mode, current flowing through S2 completely commutates to D2 to supply the load. Current IS1 returns from negative value toward zero;IL1 flows through LS. Due to the zero voltage on VDS1 , the voltage across inductor LS is V0, i.e. iLS, will decrease linearly at the rate of V0/LS. Meanwhile, the current flowing through S1 ramps up linearly. As iLS drops to zero, current is1 contains only IL1, while iD2 equals IL2. Current iLS will reverse its direction and flow through S1 together with IL1. As iLS increases in negative direction,iD2 consistently reduces to zero. At this instant, iLS equals –IL2, diode D2 turns OFF , and thus this mode comes to an end.

Despite the minor deviation of iS1 from zero and ILS from IL1, currents iLS ,is1,iD2 and the duration of this mode t01 can be approximated as

$$i_{Ls}(t) = I_L - \frac{V_o}{L_S}t \quad (1)$$

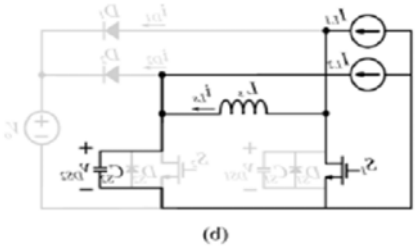
$$i_{S1}(t) = \frac{V_o}{L_S}t \quad (2)$$

$$i_{D2}(t) = 2I_L - \frac{V_o}{L_S}t \quad (3)$$

$$t_{01} = \left(\frac{3}{4} - D_{\text{eff}}\right)T_S - \frac{\sin^{-1}(V_o/(V_o + 2I_L/\omega C_S))}{\omega} \quad (4)$$

where D_{eff} is the effective duty ratio to be explained later and $\omega = 1/\sqrt{L_S C_S}$.

B. MODE-2.



(d)

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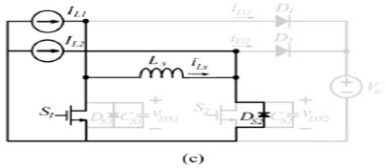
$$v_{DS2}(t) = V_o \cos(\omega t) \quad (5)$$

$$i_{Ls}(t) = -V_o \omega C_S \sin(\omega t) - I_L \quad (6)$$

$$t_{12} = \frac{\pi}{2\omega}. \quad (7)$$

C. MODE-3.



(c)

At t=t2, voltage VDS2 decreases to zero. After this stage , DS2, the antiparallel diode of S2, starts to conduct current. The negative directional inductor current iLS freewheels through S1 and DS2 , and holds at a magnitude that equals iLS2(t2) , a little higher than IL.

During this mode, the voltage on switch S2 is clamped to zero, and it is adequate to gate S2 at zero-voltage turn- ON

$$t_{23} = \left(D_{\text{eff}} - \frac{1}{2}\right) T_S. \qquad (8)$$

D. MODE-4.

MODE-4. The switch S1 turns OFF at t=t3. Current iLS begins to. Charge the capacitor CS1. The charging current includes IL1 and iLS . Since the capacitor CS1 retrieves a little electric charge, iLS decreases a little and resonates toward –IL2.at t4 In iLS, will not equal–IL2 and with a higher value, The mode will get end the voltage on switch S1 and current through LS can be approximated as While the capacitor voltage VCS1 ramps to V0,D1 will be forward-biased.

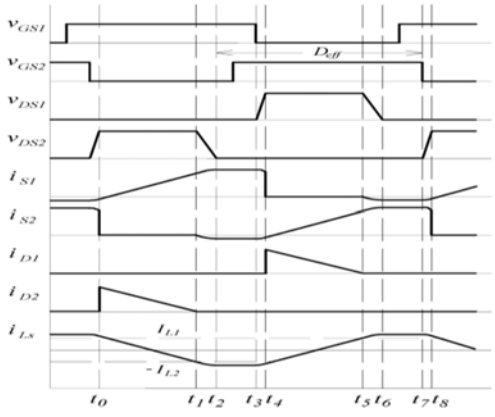
$$v_{DS1}(t) = \left(V_o + \frac{2I_L}{\omega C_S}\right) \sin(\omega t) \qquad (9)$$

$$i_{Ls}(t) = I_L - (V_o \omega C_S + 2I_L) \cos(\omega t) \qquad (10)$$

$$t_{34} = \frac{\sin^{-1}\left(V_o/(V_o + 2I_L/\omega C_S)\right)}{\omega}. \qquad (11)$$

While the capacitor voltage vCS1 ramps to V0,D1 will be forward-biased, and thus this mode will come to an end.

V. WAVEFORM



Modes I–IV describe the scenario of switch S2 between off-state proceeding to ZVS turn-ON . Operations from modes V–VIII are the counterparts for switch S1.

VI.CIRCUIT DESIGN

Operations from modes V–VIII are the counterparts for switch S1. VI.CIRCUIT DESIGN The proposed circuit is focused on higher power demand applications. Under continuous conduction mode (CCM) The inductors L1 and L2 are likely to operate , the peak inductor current can be reduced along with less conduction losses .Under CCM operation, the current ripple specification related to the inductances of L1 and L2. What dominates the output power range
and ZVS operation is the inductance of LS

A.Considerations on Inductor LS

A.Considerations on Inductor LS As the description in mode II, prior to the turn-ON of switch S2, iLwill discharge CS2, the output capacitor of switch S2, and therefore, surpass IL2 . In order to turn ON S2 at ZVS condition, switch S1 has to keep ss conducting currentso as to iLS allow to flow through antiparallel diode DS2.
The gating signal VGS2 can comfortably impose on S2. WhenDS2 clamps the switch voltage at zero, This means that vGS2 should shift to high state before vGS1 goes low. Symmetrical operations of both switches and ZVS, the duty ratios of both switches should be more than 0.5.

Whereas VDS1 or VDS2 is zero, it looks like the switch S1 or S2 is turned ON. Taking S2, for example, modes III–VII constitute the effective switch turn-ON time. Defining the effective duty ratio Deff, the voltage across L2 and VL2 holds at Vin for duration of Deff TS ; while ignoring the tiny period of modes II and VIII, VL2 is (Vin - VO) for (1 - Deff)TS. Applying the voltage–second balance principle on inductor L2, we can obtain

$$V_o = \frac{1}{1 - D_{\text{eff}}} V_{\text{in}}. \qquad (12)$$

As for the design LS of , it can be noted that current iLS will drop from IL1 down to –IL2 approximately during modes I and II. The current swing span should be a little more than 2IL to discharge CS2, and therefore, reduces vDS2 to zero before turning ON .
Consequently, (13) can be formulated to estimate the current variation ratio.

$$\frac{V_o}{L_S} = \frac{2I_L}{(1 - D_{\text{eff}})T_s} = \frac{I_{\text{in}}}{(1 - D_{\text{eff}})T_s} \qquad (13)$$

Where TS is the switching period and Iin is the input current. Assuming that the converter efficiency is, the input and load current are related as follows.

$$I_o = \eta(1 - D_{\text{eff}})I_{\text{in}}. \quad (14)$$

Therefore

$$L_S = \frac{\eta V_o T_s (1 - D_{\text{eff}})^2}{I_o}. \quad (15)$$

B. Considerations on Output Regulation

Combining (13) and (15), we can rewrite the relationship between input voltage Vin and output voltage V0 as

$$V_o = \frac{\eta T_s}{I_o L_s} V_{\text{in}}^2 = \sqrt{\frac{\eta R T_s}{L_s}} V_{\text{in}}. \quad (16)$$

For normal operations of a converter, the output voltage V0 is expected to be constant. Therefore, for a fixed LS value, switching period TS should be modulated to cope with the variations of load current I0 or input voltage Vin.

This indicates that this converter will be operated under adaptable

Parameter	Value
Inductors L1 and	600µ H
Inductors Ls	200µ H
Capacitor Co	3000 µF
Switching frequency fs	60 kHz
Input voltage vin	85v
Output voltage	3o8v
Out power po	3.9kw
MOSFETs	IXFH16F84
Diodes D1,D2	IN4007

TABLE 1 CIRCUIT PARAMERTER

Frequency to provide constant output voltage Similarly, the input current Iin with respect to output current I0 can be depicted

$$I_{\text{in}} = \frac{1}{\eta}\sqrt{\frac{V_o I_o T_s}{L_s}}. \quad (17)$$

And the output power P0 is

$$P_o = \frac{T_s}{L_s} V_{\text{in}}^2 = \eta^2 \frac{L_s}{T_S} I_{\text{in}}^2. \quad (18)$$

C. Considerations on Input Current Ripple.

The current ripples on each of the boost inductor ILcan be denoted as

$$\Delta I_L = \frac{D_{\text{eff}} T_S}{L} V_{\text{in}}. \quad (19)$$

Due to the interleaved operation, the input current is the summation of two boost inductor currents. Observing Fig. 5, the input current ripple can be illustrated as (20)

$$\Delta I_{\text{in}} = \frac{(2D_{\text{eff}} - 1)T_S}{L} V_{\text{in}}. \quad (20)$$

Under certain input current ripple requirement, inductance inductor L1and L2 can be obtained

D. Considerations Output Voltage Ripple

Since the load and output capacitor receivethe current summation from diodes D1 and D2, the frequency of the output ripple current becomes twice as high as the switch frequency. Therefore, the output ripple voltage can be reduced. The output ripple voltage can be estimated by evaluating the joint contributions from the capacitance and the equivalent series resistance (ESR)

$$\Delta V_C = \frac{I_o D_{\text{eff}}^2 T_S}{2C_o} = \frac{V_o D_{\text{eff}}^2 T_S}{2RC_o} \quad (21)$$

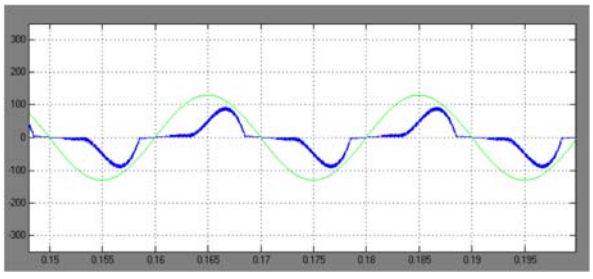
$$\Delta V_{\text{ESR}} = I_{\text{in}} \times \text{ESR} \quad (22)$$

$$\Delta V_o \cong \sqrt{\Delta V_C^2 + \Delta V_{\text{ESR}}^2}. \quad (23)$$

VII. SIMULATION RESULTS:

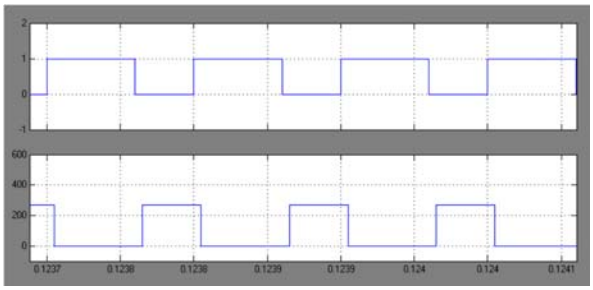
Conventional Circuit diagram wave forms

Fig:1. Input voltage and current.



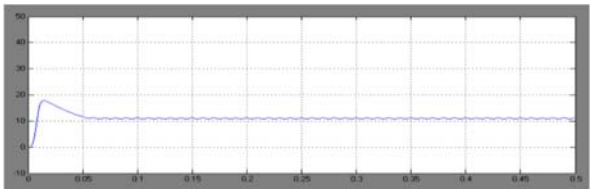
(vin:120v current:30A time:150msec)

Fig:2.Voltage vgs and vds triggering pulse waveform.



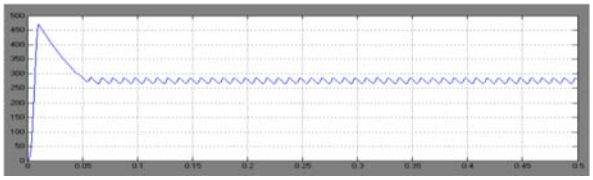
(vgs:1v vds:280v time:123msec)

Fig 3; Output current



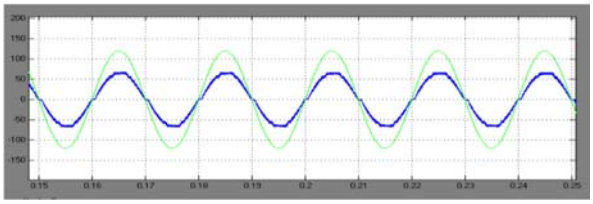
(Cureent:19A time:0.5msec) Fig 3:Output current

Fig4: Output voltage



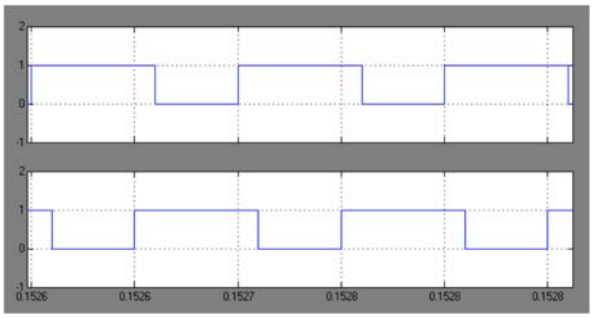
(voltage 470 and time 0.5msec)

Fig 5 : (Input voltage and current)
(vin:

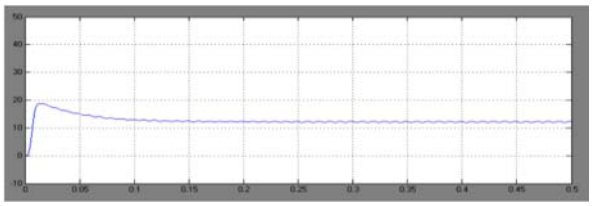


(vin:120v current:30A time:15sec)

Fig6: (Vg1andvg2Triggering pulses wave form)



(voltage vg1:1v vg2:1v time:152msec)

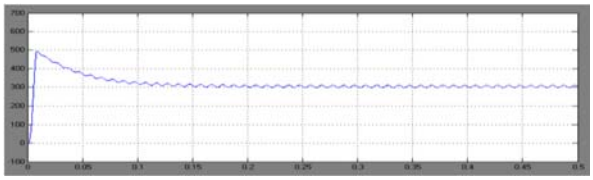


VIII. EXPERIMENTAL RESULT.

An experimental circuit is built MATLAB/SIMULINK to verify the feasibility of the is circuit topology..The parameters are listed Table1. Figs.9 and 10 illustrate the expermental waveforms. Fig.9 shows vgs and vds of each switch. Fig.6The gatingSingal is imposed on the switch after its voltage falls down to zero

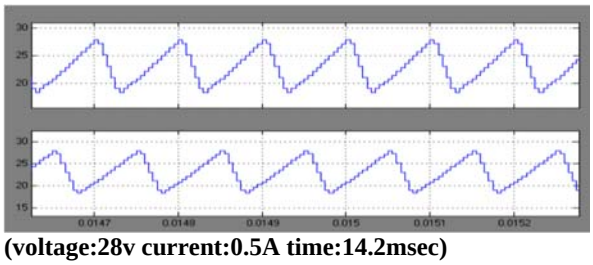
fig.10depicts relationships between current iL1,IL2 where this ripple current of iL1 is significant.IL1 flows though swtich s1 during its turn on period fig:11 shows the current ripples clearly input current ripple Iin is smaller than IL1 and IL2. The ration of Iin/Iin is less than 10% t Table 2 lists some comparison between measured results from experimental and calculated results from theoretical equcations. the measured results d not inculed the parasitics resonant peaks .the control unit of this is a peripheral interfance control micro controller. the swtiching frequency is modulated as depicted in provide output voltage regulation under output power shift.the cricuit is operated at different power output and input voltage fig15:The result is presented the best conventional voltage is320v and proposed output voltage370v the circuit efficiency achives 95%at 3.94kw.

Fig9:(vlotage vgs and vds of each switch)



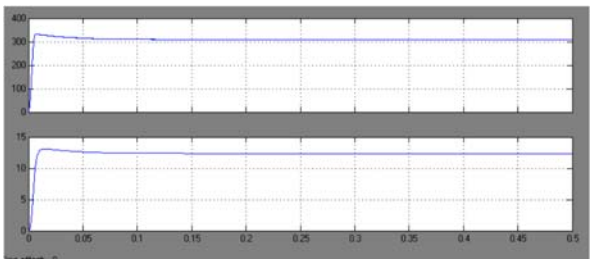
(vg1,vg2:20v vds1,vs2:350v time;162msec)

Fig10:current relationship betweeniL1,iL2



(voltage:28v current:0.5A time:14.2msec)

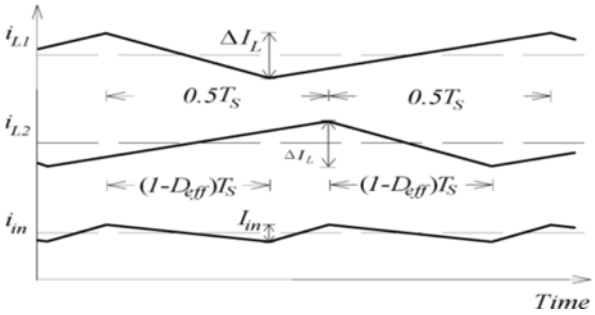
Fig11: Current ripple Iin, IL1 and IL2



IX.CONCLUSION

This paper has proposed a dual boost converter with zero voltage turn-on. It inherits the merits of interleaved converters, i.e., low output voltage ripple. The detail analysis design and control equations are presented .Inductor determines the performance of the converter. The converter can be controlled by varying switching frequency to deal with the fluctuation of input voltage and outputload. In a laboratory testing circuit, the results is presented in conventional output voltage is 320v and proposed output voltage 370v the circuit efficiency achieves 95% at 3.94k W output due to its ZVS characteristics.

X. FUTURE SCOPE THE PROJECT.



This paper concludes that c3-stage interleaved boost converter with120 degree shift can be done in future ripple can be reduced.

Closed loop can be done with ANN controlling.

XI. REFRENCES.

1. Q. Ting and B. Lehman, " Dual interleaved active-clamp forward with automatic charge balance regulation for high input voltage application ," *IEEE Trans. Power Electron., vol. 23, no. 1, pp. 38–44, Jan.2008.*
2. H. Mao, O. A. Rahman, and I. Batarseh, "Zero-voltage-switching DC-DC converters withsynchronous rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no.1, pp. 369–378, Jan. 2008.
3. J.-H. Kim, D.-Y. Jung, S.-H. Park, C.-Y.Won, Y.-C. Jung, and S.-W. Lee, "High efficiency soft- switching boost converter using a single switch," *J. Power Electron., vol. 9, no. 6, pp. 929–939, Nov. 2009.*
4. .MuhammadRashid,"Power electronics circuits ,devices and application.
5. .C. M.Wang, "A new single-phase ZCS-PWM boost rectifier with high power factor and low conduction losses," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp.500–510, Apr. 2006.