IMAGE SCALING ALGORITHM IMPLEMENTATION OF FPGA USING VHDL PROGRAMMING

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Abstract - In this Review paper, a low complexity adaptive edge enhanced algorithm is proposed for the implementation of two dimensional (2-D) image scaling applications. The proposed novel algorithm consists of a linear space-variant edge detector, a low complexity sharpening spatial filter and a simplified bilinear interpolation. The edge detector is designed to discover the image edges by a low-cost edge-catching technique. The sharpening spatial filter is added as a pre-filter to reduce the blurring effect produced by the bilinear interpolation. Furthermore, an adaptive technology is used to enhance the effect of the edge detector by adaptively selecting the input pixels of the bilinear interpolation. In addition, an algebraic manipulation and a hardware sharing techniques are used to simplify bilinear interpolation, which efficiently reduces the computing resources and silicon area in VLSI circuits. By adding eight 8-bit registers as a register bank, this design can process streaming data directly and requires only a one-line-buffer memory. The VLSI architecture of this work contains 6.67-K gate counts and achieves about 280-MHz processing rate by using TSMC 0.13-um CMOS process. Compared with the previous low-complexity techniques, this work performs better quality, higher performance, less memory requirements,
and lower hardware cost than other image scaling methods.

Index Terms - Edge detector, Image zooming, sharpening spatial filter, Two dimensional (2-D) Image scalar, and VLSI.

I. INTRODUCTION

Image scaling is the process of resizing a digital image. It has been widely applied in the fields of digital imaging devices such as digital cameras, digital video recorders, digital photo frame, high-definition television, mobile phone, tablet PC, etc. An obvious application of image scaling is to scale down the high-quality pictures or video frames to fit the minimize liquid crystal display panel of the mobile phone or tablet PC. As the graphic and video applications of mobile handset devices grow up, the demand and significance of image scaling are more and
More outstanding. The image scaling algorithms can be separated into polynomial-based and non-polynomial-based
Methods. The simplest polynomial-based method is a nearest neighbor algorithm. It has the benefit of low complexity, but the scaled images are full of blocking and aliasing artifacts. The most widely used scaling method is the bilinear interpolation algorithm by which the target pixel can be obtained by using the linear interpolation model in both of the horizontal and vertical directions..

II. RELATED WORK

A novel scaling algorithm is proposed for the implementation of 2-D image scalar. The clamp and sharpening spatial filters are added as pre-filters to solve the blurring and aliasing effects produced by bilinear interpolation. Furthermore, an adaptive technology is used to enhance the effects of clamp and sharpening spatial filters. To reduce memory buffers and computing resources for the very large scale integration (VLSI) implementation, the clamp filter and sharpening spatial filters both convoluted by a 3×3 matrix coefficient kernel are combined into

a 5×5 combined convolution filter. An edge-oriented area-pixel scaling processor is to achieve the goal of low cost, the area-pixel scaling technique is implemented with low-complexity VLSI architecture. A simple edge catching technique is adopted to preserve the image edge features effectively so as to achieve better image quality Compared with the previous low-complexity techniques; it performs better in terms of both quantitative evaluation and visual quality. An efficient VLSI design of bi cubic convolution interpolation for digital image processing. The architecture of reducing the computational complexity of generating coefficients as well as decreasing number of memory access times. Numerous digital image scaling techniques have been presented. The most popular methods are nearest neighbor, bilinear, Win scale, bi-cubic, and cubic. In which the simplest approaches are nearest neighbor and bi-linear interpolation. A better quality of interpolation is achieved by using higher order models. The high-speed VLSI architecture has been successfully designed with high performance architecture of bi-cubic convolution interpolation. In this paper bilinear interpolation technique is used for designing image scaling processor which has got the advantage of reducing the computing resources, memory requirement and it can be easily Implemented VLSI.

III. PROPOSED WORK

Adaptive edge- enhanced technique is used to develop real-time, low-cost, and high-performance image scalar using four line buffers. This also improves the image quality by adding sharpening spatial and clamp filters as pre-filters, by an adaptive technique based on the bilinear interpolation algorithm. Although the memory requirement and hardware cost had been efficiently reduced in the technique, it still requires four line buffers. Hence, a low cost, low-area, low-memory-requirement and efficient image scalar design is proposed in this work. An efficient image scaling algorithm design with low cost, low-area, low-memory- requirement is proposed in this work.

A. Theoretical Analysis

Image scaling is widely used in many fields, ranging from consumer electronics to medical imaging. It is indispensable when the resolution of an image generated by a source device is different from the screen resolution of a target display. For example, we have to enlarge images to fit HDTV or to scale them down to fit the mini- size portable LCD panel. The most simple and widely used scaling methods are the nearest neighbour and bilinear techniques. In recent years, many efficient scaling methods have been proposed in the literature. According to the required computations and memory space, we can divide the existing scaling methods into two classes: lower complexity and higher complexity scaling techniques. The complexity of the former is very low and comparable to conventional bilinear method. The latter yields visually pleasing images by utilizing more advanced scaling methods. In many practical real-time applications, the scaling process is included in end-user equipment, so a good lower complexity scaling technique, which is simple and suitable for low-cost VLSI implementation, is needed.

B. Scaling Methods

Image size is most commonly decreased (subsampled or down sampled) in order to produce thumbnails. Enlarging an image (up sampling or interpolating) is generally common for making smaller imaginary fit in a bigger screen in full screen mode, for example. “In Zooming” an image. By zooming it is not possible to discover any more information in the image than already exists, and image quality inevitably suffers. However, there are several methods of increasing the number of pixels, to improve the quality of image in zoom mode. Some Scaling Methods are given below:-

1. Nearest-Neighbor
2. Bilinear Interpolation
3. Bicubic Interpolation
4. Area-Pixel scaling

B. Block Diagram- Methodology of Implementation

In the proposed work (Figure1), the scaling process will be done on 2D Image. where the input image will be converted into pixel values using Matlab, and Bilinear Scaling (Interpolation) process will be applied over that image and again that pixel value will be retrieved into image using Matlab. The aim is to implement the image scaling processor at a very low cost. The image scaling process is done for 2D image and results are analysed by their PSNR. To obtain the qualities of the scaled

images by Bilinear scaling algorithm. The actual implementation of Bilinear Scaling Algorithm on FPGA is shown in Figure 2.

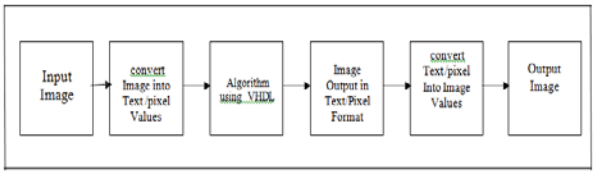

Figure 1: Block diagram for the proposed work

In the following block diagram (Figure2), the input gray scale image is converted in to text using matlab. The text image is given to register bank on FPGA. The pixels are feed to the sharp filter and edge detector. The edge detector identifies the horizontal and vertical gradient. The gradient gets added to form the edges in the image. The sharp filter which is actually a mask of weights arranged in a rectangular pattern, It is mainly used for smoothing and sharpening. The multiplexer combines the pixels coming from register bank directly and pixels passing through sharp filter.

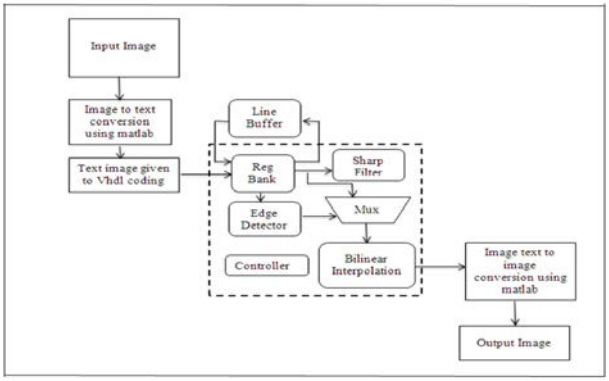

Figure 2: Implementation of proposed adaptive edge enhanced algorithm

The output of edge detector controls the multiplexer input according to the asymmetric parameter (A) of the image.

$$A = |P_{(m+1)} - P_{(m-1)}| - |P_{(m+2)} - P_{(m)}|$$

Where P(m+1) , P(m-1) , P(m+2) , P(m) four nearest neighboring Pixels. The multiplexed output is given to the bilinear interpolation block. The bilinear interpolation is used to up scaling or image zooming. Finally the image is zoomed by bilinear interpolation. The image text is converter to image using matlab. Finally output image is obtained.

D. Performance parameter:

The results obtained will be compared with the other algorithms which were noted in the literature review.

-- Peak signal-to-noise ratio(PSNR)

--Mean Square Error(MSE)

E. Steps for Proposed methodology

The steps followed in the proposed methodology are as below:

1. Read Gray Scale Image.
2. The Image is converted to Text Using Matlab.
3. The image pixels are passed through edge detector and sharp filter, implementation on FPGA .
4. Bilinear scaling method implementation on FPGA is applied to the pixels for up scaling.
5. The output pixels are converted to image using matlab.
6. Display the output Image.

IV. RESULTS

To be able to analyse the qualities of the scaled images by various scaling algorithms, a peak signal-to noise ratio (PSNR) is used to quantify a noisy approximation of the defined and the original images. Since the maximum value of each pixel is 255, the PSNR expressed in dB can be calculated as The results obtained will be compaired with the other algorithms which were Noted in the literature review.

1. Mean Square Error(MSE)

$$MSE = \frac{1}{MN}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}[P(i,j) - P'(i,j)]$$

Where

M & N are the size of the images.

2. Peak signal-to-noise ratio(PSNR)

$$PSNR(DB) = 10\log_{10}\frac{MAX^2}{MSE}$$

Where

Max= Maximum value of each pixel.

TABLE:-1 RESULTS FOR DIFFERENT IMAGES AND ITS PSNR

Parameter	Lina	peppers	Mandrial	Airoplan	xilinx logo	Cameraman
orignal size	64x64	64x64	64x64	64x64	64x64	64x64
scalling size	96x96	96x96	96x96	96x96	96x96	96x96
scaling factor	1.5	1.5	1.5	1.5	1.5	1.5
PSNR	36.01	37.8	39.46	36.3	37.25	36.48
MSE	16.29	10.8	7.375	15.2	12.22	14.61

V. CONCLUSION

This method is proposed to improve the quality of Image with PSNR ratio. Here we apply the binary value which is calculated from MATLAB software to the FPGA and we comprise image quality and PSNR ratio.

Based on the Bilinear Algorithm for Image Scaling. Finally we are concluding comparing the parameters which are get from FPGA kit and pass to the MATLAB GUI where we are Processing our algorithm.

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