DESIGN OF SUB VOLT AND ENHANCED BAND WIDTH IMPROVED IMPEDANCECURRENT MIRROR

P. Anil Kumar[1] Dr. Bharti Chourasia[2], Dr. N. Raj[3], Dr. Komal Kanojia[4]
[1]Ph.D Scholar, Dept of Electronics and Communication Enginering,
Sarvepalle Radhakrishnan University, India
[2]Professor,Department of Electronics and Communication Enginering,
SRK University, Bhopal, India
[3]Assistant Professor, Department of Electronics and Communication Enginering,
LMNIIT Jaipur, India
[4]Associate Professor, Department of Electronics and Communication Enginering, SRK

Abstract—In this paper, an efficient current mirror is proposed using a quasi-floating gate based MOSFET. SC (self-cascode) structure greatly improves increase in resistance an almost floating gate approach helps improve the drain-source voltage of the line MOSFET itself cascode and consequently both cascode transistors themselves get bored because both MOSFETs saturate this results in increased effective transconductance. The proposed current mirror also uses feedback at the input -part to reduce the input resistance. The current mirror works well up to 785 gigahertz bandwidths. The input and output impedances achieved are 390 X and 136 G X respectively. A complete analysis is done with the MOSFET Models with 180 nm CMOS technology sub threshold (± 0.5 V) voltage. Index Terms— Self cascode, Quasi-floating gate Current mirror, Transconductance, Output resistance

I. INTRODUCTION

The Nano meter device dimensions and under voltage characteristics preferred high-performance digital logic design functions. But these devices do not provide satisfactory performance in designing analog circuits which is largely due to the effect of channel length modulation (CLM).Among various approaches, the self cascode (SC) MOSFET is widely adopted to reduce such the CLM effect [1, 2]. However, the SC structure has a disadvantage of having requirement of large device dimensions. Many solutions have been introduced to compensate such requirements [3–5].The threshold voltage was always a great obstacle in circuit design, especially for low voltage analog circuits. The main cause is due to fact that the scaling technique cannot be applied to the threshold voltage In this regard, the minimum supply voltage cannot be obtained is scaled below the MOSFET threshold voltage. There are little widely accepted low voltage (LV) low power (LP) technologies who have shown their potential are under the threshold (weak inversion) range [7], level shifting technique [8], Mass-electric technology [9], floating gate (FG) structure [10], Quasi-Floating Gate (QFG) structure [11] and Bulk controllable floating/quasi-floating gate (BULK DRIVENFG/BULK DRIVENQFG) structure [12]. These LVLP techniques are classified unusual techniques. However, related the downside of using these techniques is minimal comparison of the transconductance and thus low bandgap circuits for gate-driven (GD) MOSFET-based designs between above mentioned techniques, FG and its modified structure QFG has proven its potential in LV analog design provides multi-input capacitive coupling that promotes threshold voltage scaling. Apart from this, when the result of QFG combined with BULK DRIVEN technique a new structure popularly known as BULK DRIVENQFG MOSFET showed improved frequency parameters over of simple BULK DRIVEN based different designs. Commonly BULK DRIVEN based circuit designs provide a very low voltage operation but do suffers from poor linearity and extremely low

transconductance. So, based upon the desired performance parameter enhancement of designs, the choices of technique is developed.

There are few non-conventional techniques can be found as: based on BULK DRIVEN [13], based on FG [14, 15], based on QFG [16–20] and based on BULK DRIVENQFG [21–23]. Few recent works on low power current mirror design can be found in [24–27]. In this paper, a modified structure of gate driven Self Cascode (SC) is proposed which uses the Quasi floating gate (QFG) MOSFET. The proposed QFG-SC structure results in operation of both the MOSFETs in saturation mode resulting in improved performance over conventional gate driven SC structure. Further to evaluate the performance of proposed QFG-SC, current mirror designs is presented and compared with its conventional architecture.

The paper explains the different sections. In Section II detailsabout the proposed QFG-SC structure followed to design ofbasic current mirror circuit based on proposed QFG-SC andas well based on conventional SC structure in Sect. III. Alsothis section includes a high performance current mirror
design to exploit the features of proposed QFG-SC structure.The current mirror designs is supported by their smallsignal model analysis. The simulation results are discussed and inconclusion and future work in sec IV and Sect. V respectively.

II. Quasi Floating Gate Self Cascode Strcture

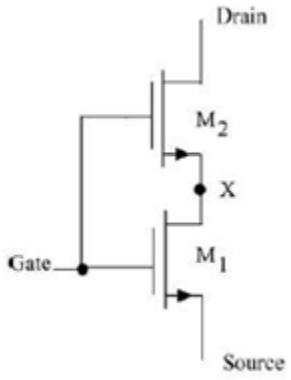

Fig: 1 Self cascode structure: a Conventional SC

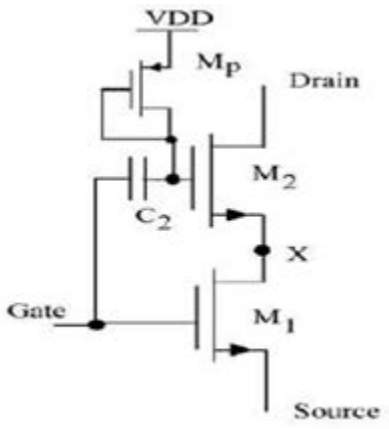

Fig:2Self cascode structure:Modified QFGSC

Analysis of Fig. 1, showed operation of M1 in linearmode whereas M2 in saturation mode. However, if M1 ischanged from linear mode to saturation mode then effectivetransconductance can
be increased which can used inhigh gain analog circuits. The possibility of this conditionexist if VDS of M1 is increased, i.e. Vth,M2\Vth,M1. The
Required condition need to be satisfied for operatingboth the MOSFETs of SC in saturation region is [5]:

$$V_{DS,sat,M_2} \geq V_{th,M_1} - V_{th,M_2}. \quad (1)$$

$$V_{th2,eff} = \frac{C_{T,qfg}}{C_2} V_{th2} - \frac{C'_{GD,MP}}{C_2} V_{DD}, \quad (2)$$

To achieve this condition, the QFG technique is used inthe proposed design. In Fig. 1b, the transistor M2 ischanged to QFG with the help of input capacitor C2 and theMOSFET MP working in cut-off region so as to realizelarge value resistance. Under such the effective thresholdvoltage of M2 changes to equation 2. where CT;qfg is the total capacitance seen at the QFGnode of M2 and C0GD;MP is the parasitic capacitance of MP.

The advantage of using QFG can be seen in (2) where theeffective threshold of M2 gets scaled down due to whichthe possibility of satisfying the condition for saturationregion shown in (1) increases. The QFG MOSFET leads toincreased value of VDS of M1 which changes its

operatingregion from linear to saturation. As both the MOSFETs ofSC turns in saturation, the effective transconductance getsincreased. The effective transconductance of proposedQFG-SC is calculated as:

$$G_{m,QFG-SC} = \frac{g_{m1}r_{01} + g_{m2,qfg}r_{02,qfg} + g_{m1}g_{m2,qfg}r_{01}r_{02,qfg}}{r_{01} + r_{02,qfg} + g_{m2,qfg}r_{01}r_{02,qfg}}. \quad (3)$$

III Proposed Quasi Floating Gate SC current mirror

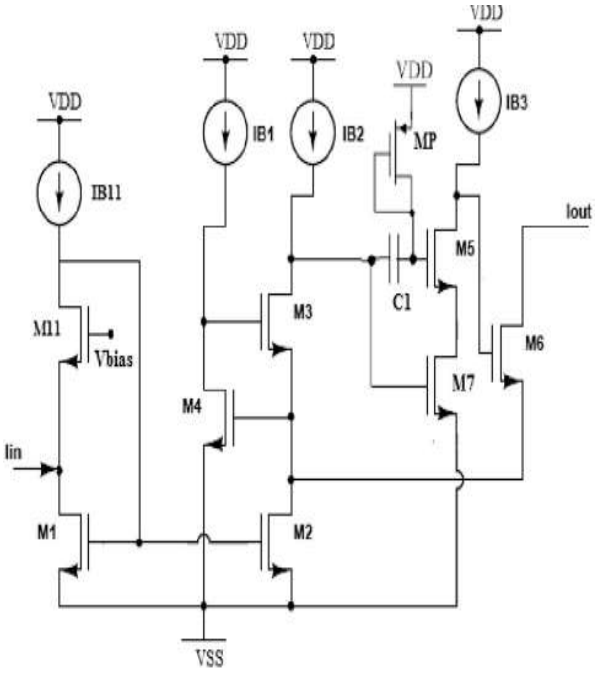

Fig 3:Proposed high performance current mirror

The working principle remains the same like that of itsconventional design. In order to reduce the input resistancea scaling factor is introduced in the input resistance. Thisfactor is introduced by applying a negative feedback viaMOSFET M11 and current source IB11. As the draincurrent of M11 is constant due to current source IB11, anychange in the input current is sensed by M1 and accordingly
produces suitable change in its gate-to-source voltage(Vgs,M1). The input node experience a scaling factor of($gm_{11}r_{011}$) which helps in reducing the resistance further.Similarly, to boost the output resistance the output sectionis modified by using proposed QFG-SC structure. TheMOSFET M5 andM6 together forms the self cascade structure and to convert it in QFG, a capacitor C1 and cutoffmode MOSFET Mp is used at the gate node of M5. TheQFG-SC structure introduces a multiplying factor of(gm7r07) in the output resistance which significantly boostthe output resistance. Though these modification does notaffect the bandwidth but it can be also improved byapplying the compensation techniques like resistive,inductive etc. [30].

(i) Input resistance:

Small signal model for calculating the input resistance($R_{in.prop}$) of proposed current mirror is shown in Fig. 4.

At node 1

$$i_{in} - \frac{V_{11}}{R_1} - g_{m1}V_1 - \frac{V_1}{r_{01}} = 0 \quad (4)$$

At node 1

$$g_{m11}V_1 + \frac{V_1 - V_{11}}{r_{011}} - \frac{V_{11}}{R_{11}} = 0 \quad (5)$$

Since $g_m r_0 >> 1$

$$V_{11} \approx g_{m11}(r_{011}//R_{11})V_1 \quad (6)$$

From (4) and (6)

$$i_{in} = \left(\left(\frac{1}{R_{11}} + g_{m1}\right)g_{m11}(r_{011}//R_{11}) + \frac{1}{r_{01}}\right)V_1 \quad (7)$$

By Solving the eq (7)

$$R_{in} = \frac{V_1}{i_{in}} \approx \frac{1}{g_{m1}g_{m11}(r_{011}//R_{11})} \quad (8)$$

For an ideal current source, $R_{11} = \infty$

$$R_{in,prop.} \approx \frac{1}{(g_{m11}r_{011})g_{m1}} \quad (9)$$

From (9), it can be observed that compared to conventionalcurrent mirror there is a scaling factor of (gm11r011)in the input resistance. However, it remains similar to thatof conventional FVF current mirrorit can be observed that compared to conventionalcurrent mirror there is a scaling factor of (gm11r011)in the input resistance. However, it remains similar to thatof conventional FVF current mirror.

(ii) Output resistance:

The small signal model for calculating the output resistanceof proposed current mirror $R_{out;prop.}$is shown in Fig. 5.The symbols used throughout analysis are the standardspice model

parameters of MOSFET and have their usual meaning.

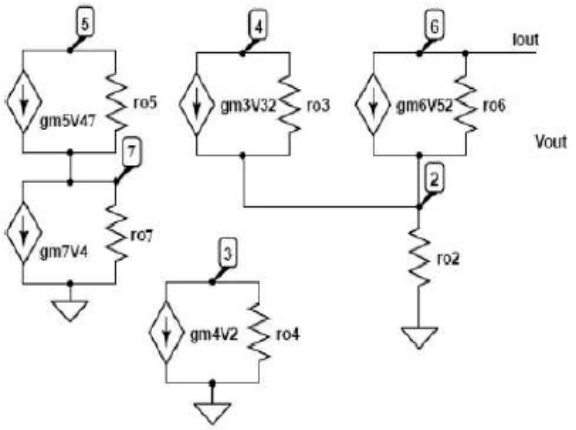

Fig. 4 Small signal model for calculating output resistance

$$\text{Here} \quad i_{out} = g_{m6}V_{52} + \frac{V_{out} - V_2}{r_{o6}}$$

$$V_2 = i_{out} r_{o2}$$

and

$$V_5 = -(g_{m5}r_{05})(g_{m3}r_{o3})(1 + g_{m4}r_{o4})(g_{m7}r_{07})V_2$$

From above (10), (11), (12)

$$R_{out} = \frac{V_{out}}{i_{out}} = (r_{o6} + r_{o2}((g_{m6}r_{o6})(g_{m5}r_{o5}) (g_{m7}r_{07})(g_{m3}r_{o3})(1 + g_{m4}r_{o4}) + (1 + g_{m6}r_{o6}))) \quad (13)$$

Since $g_m r_o >> 1$

$$R_{out,prop.} \approx r_{o2}(g_{m3}r_{o3})(g_{m4}r_{o4})(g_{m5,qfg}r_{o5,qfg})(g_{m6}r_{o6})(g_{m7}r_{07}) \quad (14)$$

whereas for conventional architecture it is [18]

$$R_{out,conv.} \approx r_{o2}(g_{m3}r_{o3})(g_{m4}r_{o4})(g_{m5}r_{o5})(g_{m6}r_{o6}) \quad (15)$$

From (14) and (15), the improvement in output resistancecan be seen by factor ($g_{m7}r_{07}$) compared to its conventionalarchitecture.

IV Simulation results

The conventional and proposed current mirrors is simulatedon 180 nm CMOS process at ± 0.5 V power supply.The enhancement type of MOSFETs is used in this paper todesign current mirror circuit. The device dimensions takenfor simulation purpose in CM designs presented are shownin Table 1. The other assumed parameters for circuit simulationsare also listed in respective tables. The simulation results well support the mathematical analysis of proposed designs. The current transfer characteristic of proposed current mirror ranging from 0 to 700 µA is shown in Fig. 6. The input characteristics are shown in Fig. 7.

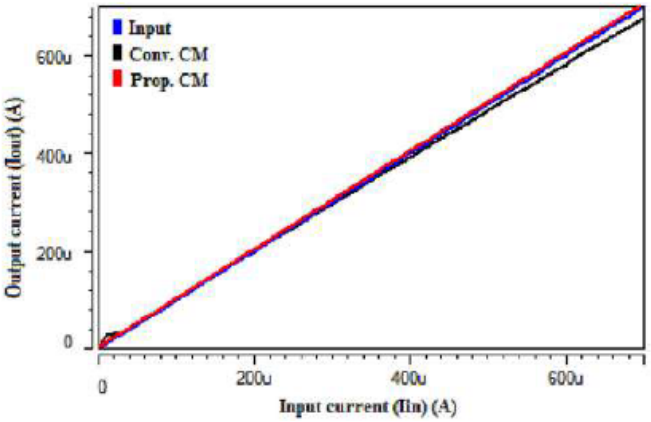

Fig5: current Tansfer characteristics ranging (0-700uA)

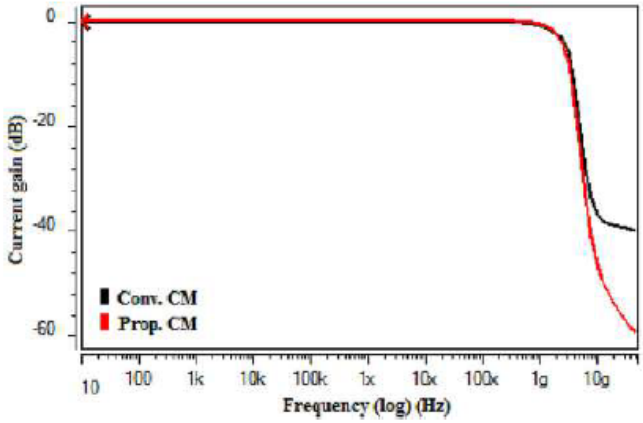

Fig6:frequency Response

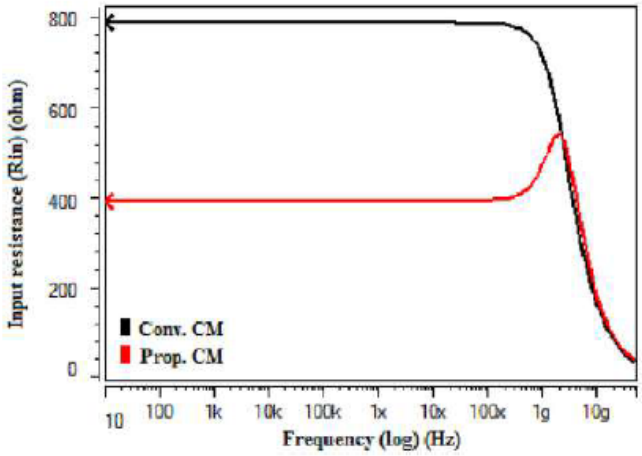

Fig7: Input Resistances

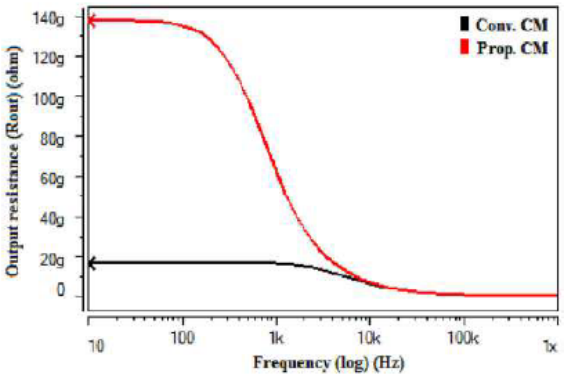

Fig8:Output Resistances

Table 1 (W and L of MOSFET)

Transistors	W (μm)	L (μm)	Transistors	W (μm)	L (μm)
M11	25	0.24	M5	2.24	0.24
M1	25	0.24	M6	5.25	0.24
M2	25	0.24	M7	2.24	0.24
M3	10	0.24	MP	0.24	0.24
M4	10				

C1 = 1pf, supply = ± 0.5 V, IB11 = IB1 = 30 µA,
IB2 = IB3 = 100 µA

Table 2(Comparision of performance parametersof proposed CM)

Parameters	[25]	[30]	[18]	Proposed CM (Fig. 3)
Input current (uA)	0–500	–	0–700	0–700
Input resistance (ohm)	17	8	780	378
Output resistance (ohm)	750 K	–	13G	137G
-3db frequency (HZ)	4.5G	11.1G	2.4G	2.2G
Supply (V)	± 0.5	1.5	± 0.5	± 0.5
Technology (um)	0.18	0.18	0.18	0.18

V Conclusion and future scope

With the increased transconductance ofQFG self cascode, the proposed current mirror exhibitsgiga ohm range output resistance fig 8. The reduced inputresistance is achieved by using a feedaback at the inputnode.

the proposed current mirror has good input andoutput resistance. However, the input resistance can befurther reduced by using the additional feedback loop in theinput section. Apart from resistance it has been observedthat the bandwidth of proposed current mirror is limited to2.2 GHz range and by thecompensation techniques can be applied to proposed circuit to wide bandwidth.

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