A HYBRID CASCADED NINE LEVEL INVERTER

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Abstract—The problem of harmonic distortion in the case of conventional two level inverters can be reduced using multilevel inverters. With increase in number of levels, the output voltage waveform approaches nearly a sinusoidal waveform that has reduced harmonic distortion. For a given level a CHB has got minimum number of switches compared to other topologies. This paper proposes a Nine Level Cascaded H Bridge Inverter with reduced number of switches and has a lower total harmonic distortion. The control strategy used is a dual reference multicarrier phase shifting modulation. The proposed inverter can be used for photovoltaic systems.

Index Terms—Multilevel Inverter, Multicarrier Pulse Width Modulation

I. INTRODUCTION

The problem of harmonic distortion in the case of conventional two level inverters can be reduced using multilevel inverters. Multilevel inverters has the advantages such as they have nearly sinusoidal output voltage waveforms, output current with better harmonic profile, less stress of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size and lower EMI, all of which make them cheaper, lighter and more compact. The different types of multilevel inverter are Neutral Point Clamped (NPC) or Diode clamped, Flying (FC) and Cascaded H bridge (CHB) multilevel inverter. Among these the H-bridge multilevel topologies are the most attractive as they got a higher level of output voltage for the same number of power devices [1]-[2]. The aim is to increase the level number of level number for the H-bridge multilevel topologies, such that the harmonic contents can be reduced as much as possible while keeping low switching frequency and switching losses. Owing to its modular structure it can be stacked easily for high voltage and high power applications.

Several identical H-bridge cells are cascaded in series as per the requirement constitute a cascaded H bridge. Cascaded H bridge (CHB) multilevel inverter is suitable for photovoltaic systems[3]-[5] .Cascaded H bridge can be further classified as symmetrical and asymmetrical bridge inverters. For a symmetric inverter the input DC voltage is equal in all the cascaded power cells and is unequal for asymmetrical CHB. In terms of modularity, maintenance and cost the symmetrical CHB is more advantageous. In case of the asymmetrical CHB input DC voltage is varied in each power as per the requirement to increase the voltage levels. In this paper a new configuration of the transistor clamped H-Bridge based 9-level multilevel inverter is proposed which produces a nine-level output voltage.

II. CONFIGURATION OF PROPOSED NINE LEVEL INVERTER

The proposed nine level inverter consist of cascading of two single-phase, 5-level PWM inverter. Cascading y number of 5-level inverter gives a maximum number of (4y + 1) levels[10]. The overall harmonic profile of the output waveforms is improved by the addition of an auxiliary/clamping switch to each of the bridge The component-count of the proposed inverter configuration is highly reduced when compared with the conventional CHB inverter, for the same output voltage level. The circuit for nine level cascaded H-bridges is shown in Fig.1.

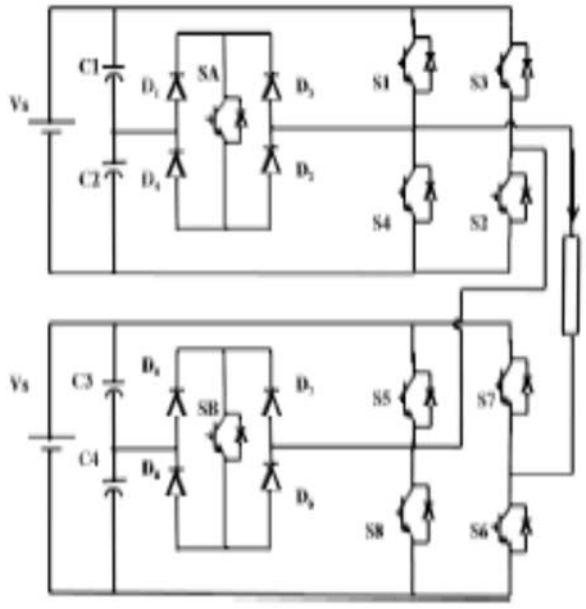

Fig.1.Proposed Nine Level Inverter

To synthesize nine output voltage levels, it employs two independent dc voltage sources of V_s which are divided into two input sources 1/2 V_s in order to secure an additional dc voltage source of V_s [12]. The inverter module having a bidirectional switch produces 5-levels of output voltage (- V_s, -.5V_s, 0, V_s, .5V_s) by controlling of the switches. Since every output terminal of the inverter module is connected in series, the output voltage becomes the sum of the terminal voltages of each inverter.

III.WORKING

Proper switching of the inverter can produce nine output-voltage levels: 0,1/2V_s, V_s,3/2 V_s,2V_s,-1/2V_s,-V_s,-3/2V_s,-2V_s. The switching states are given in Table 1.

TABLE.1.SWITCHING PATTERN FOR THE PROPOSED NINE LEVEL INVERTER

Sl	S2	S3	S4	S5	S6	S7	S8	SA	SB	V_o
0	1	0	1	0	1	0	1	0	0	0
0	1	0	0	0	1	0	1	1	0	$0.5V_s$
1	1	0	0	0	1	0	1	0	0	V_s
1	1	0	0	0	1	0	1	0	0	$1.5V_s$
1	1	0	0	1	1	0	0	0	0	$2V_s$
0	1	0	1	0	1	0	1	0	0	0
0	0	1	0	1	0	1	0	1	0	$-0.5V_s$
0	0	1	1	0	0	1	0	0	0	$-V_s$
0	0	1	1	0	0	1	0	0	1	$-1.5V_s$
0	0	1	1	0	0	1	1	0	0	$-2V_s$

The nine switching states are obtained by proper switching.For the output voltage Vo=0.5Vs,the switches S2,S6,S8and SA are on.The switches S1,S2,S6 and S8 are made on to obtain Vo=Vs.With S1,S2,S6 and SB on,the output voltage can be obtained as 1.5Vs.To get Vo=2Vs, S1,S2, S5 and S6 are made on.The switching on of S2,S4,S6 and S8 gives Vo=0.To obtain Vo=-0.5 Vs,S3,S5,S6 and S7 are made on.Switches S3,S4,S5,S7 are made on to make Vo=-Vs.With S3,S4,S7 and SB on , Vo=-1.5 Vs.The nineth level Vo=-2Vs is obtained by switching on S3,S4,S7 and S8.

IV. PWM MODULATION

The gating signals for the inverter are generated by using dual reference Multi carrier phase shifted pulse width modulation. In the Sinusoidal pulse width modulation scheme, the output voltage can be changed by varying the width of pulses as the switch is on and off several times during each half-cycle By properly selecting the type of modulation for the pulse widths and the number of pulses per half-cycle ,the lower order harmonics can be eliminated or

reduced. Higher order harmonics may increase, but these can be eliminated easily by filters of lower size. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics which is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter. The dual reference multicarrier phase shifting modulation is given in Fig.2.

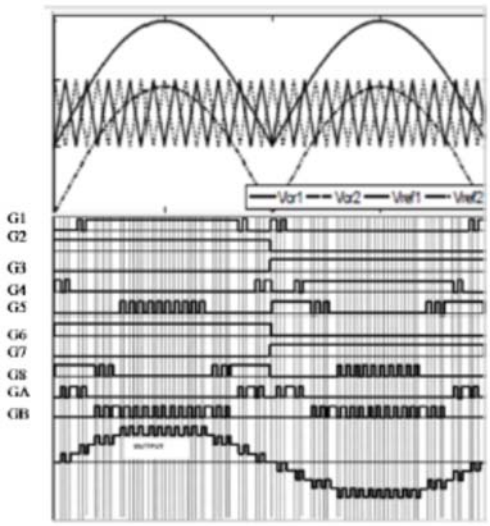

Fig.2.Dual Reference Multicarrier Pulse Width Modulation

In this pulse width modulation two reference signals and the two carrier signals are used. The references are identical but are displaced by an offset which is equal to the carriers amplitude which is equal to 0.5.

$$Vref = VmSin\omega t \qquad eqn \quad (1)$$

$$Vref1 = |Vref| \qquad eqn.(2)$$

$$Vref2 = \frac{1}{2}|Vref1| \qquad eqn.(3)$$

The carriers have same amplitude and frequency but are phase shifted by an angle given by

$$\theta cr, n = \frac{2(n-1) * 180}{Nc}$$

V. EXPERIMENTAL RESULTS

The Simulink model for the proposed Nine level inverter is given in Fig.3.The simulation is carried out in MATLAB/SIMULINK. The control strategy is also given.

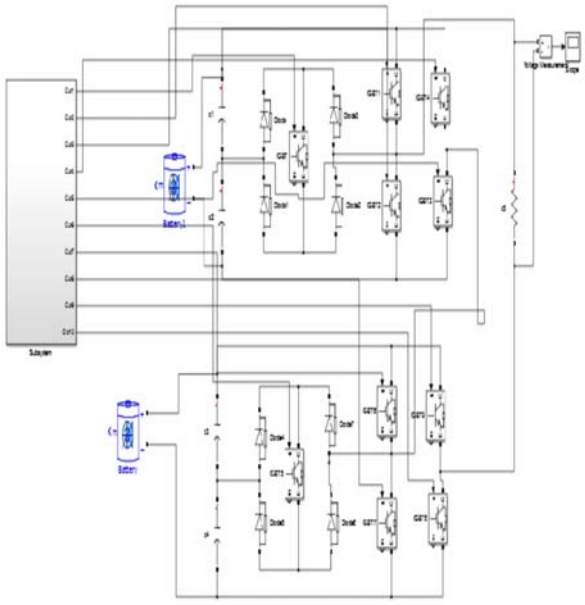

Fig.4. Simulink Model of .Proposed Nine Level Inverter

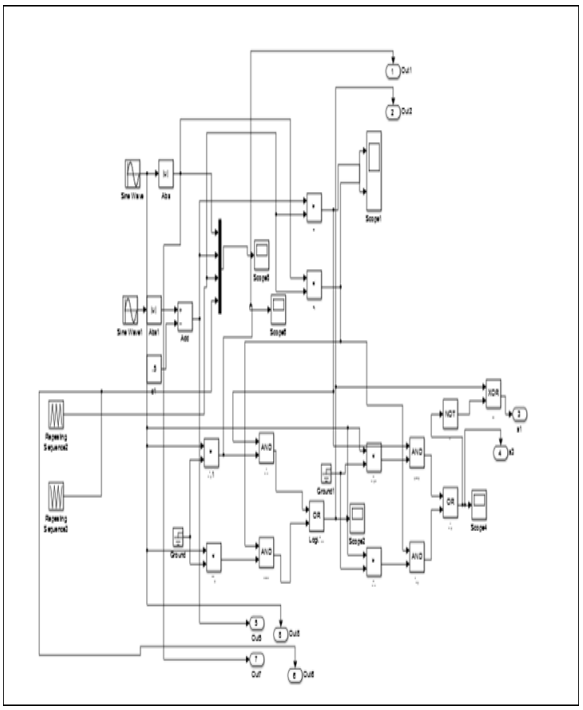

Fig.5. Simulink Model of .PWM

The dual reference multicarrier phase shifting pulse width modulation scheme is shown in Fig.5.The advantage of this scheme is that it offers the charge balance control in the input DC sources and voltage across the capacitor are also balanced .

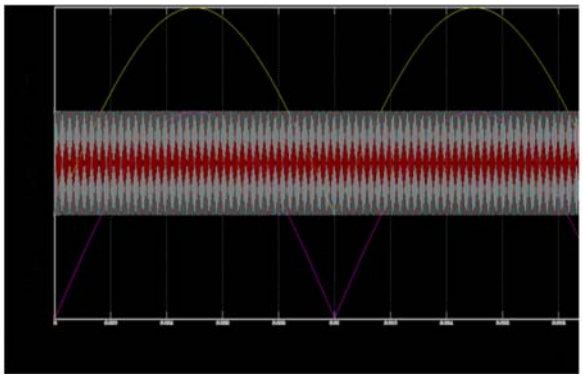

Fig.6. Pulse Width Modulation

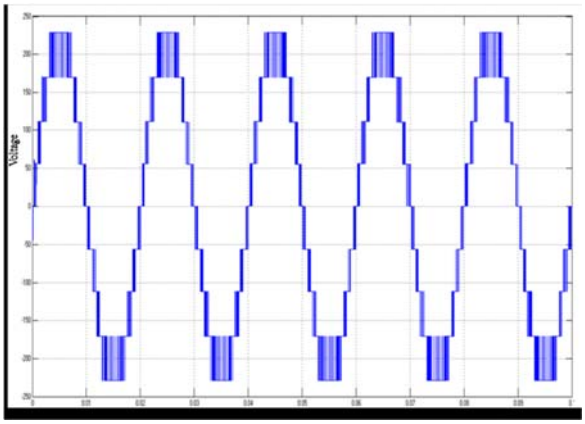

Fig.7. Output Voltage of .Proposed Nine Level Inverter

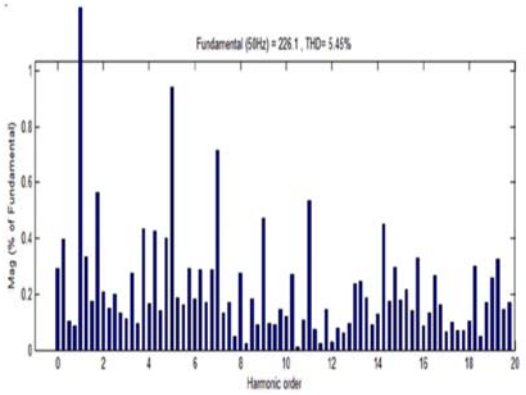

Fig.8. THD Analysis of Output Voltage

The THD obtained is about 5.45%.This improves the efficiency of the proposed inverter.

The hardware is implemented using MOSFET IRF 540 and optocoupler MCT2E.The gating pulses are generated using Microcontroller. The hardware setup is shown in Fig.9. The protype uses two 12 V dc sources as input and the nine level output of 24 V is obtained as in Fig.10.

Fig.9. Hardware Set up

Fig.10. Observed Output Voltage Waveform

The desired nine level output voltage is obtained as above.

V.CONCLUSION

The proposed Nine level inverter has reduced number of switches and has a lower THD. This proposed multilevel inverter reduces the harmonic content and thereby the size of filter is reduced. The proposed cascaded inverter is suitable for grid connected photovoltaic systems.

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