VLSI DESIGN OF FULL SUBTRACTOR USING MULTI-THRESHOLD CMOS TO REDUCE THE LEAKAGE POWER AND GROUND BOUNCE NOISE

[1]Pawar Chander, [2]Pokala Santhosh, [3]Prasad Kurhe
[1,3]Assistant Professor,SRES, College of Engineering,Kopargaon,Maharashtra
[2]Assistant Professor,SRCEW,Nizamabad, Telangana
Email: [1]pawarchander@gmail.com, 2Santu_523@yahoo.co.in, [3]prasad.kurhe576@gmail.com

ABSTRACT

The performance degradation with technology scaling is one of the major issues in today's life. Leakage power dissipation in the IC increases exponentially with technology continuously scaling down. MTCMOS Power Gating is a very well known way to reduce leakage current, but when circuit transition goes from sleep to active mode, due to abrupt transitions introduces Ground Bounce Noise in the circuit, it disturbs the normal working of any circuit and tends to wrong output and also reduces the reliability of circuit.

In this paper a full subtractor using MTCMOS technique design is proposed to reduce leakage power and ground bounce noise. Combinational logic has extensive applications in quantum computing, low power VLSI design and optical computing. Low-power design techniques proposed to minimize the active leakage power in nanoscale CMOS very large scale integration (VLSI) systems and an additional wait mode and extra header transistor is added in the circuit to reduce the ground bounce noise.

Keywords

MTCMOS, Full Subtractor, Leakage Power, Ground Bounce Noise.

1.INTRODUCTION

The rapid increase in the number of transistors on chips has enabled a dramatic increase in the performance of computing systems. However, the performance improvement has been accompanied by an increase in power dissipation; thus, requiring more expensive packaging and cooling technology. Power dissipation in CMOS circuits has been the charging and discharging of load capacitances, often referred to as the dynamic power dissipation. Dynamic power is consume when transistors are switching As the technology continue to scale down a significance portion of the total power consumption in high performance digital circuits is due to leakage current because of reduced threshold voltage .MOSFETs are fabricated with high overall doping concentration, lowered source/drain junction depths, halo doping, high-mobility channel materials, etc. Furthermore, the reduction of the gate oxide thickness (tox) causes a drastic increase in the gate tunnelling leakage current due to carriers tunnelling through the gate oxide, which is strong exponential function of the voltage magnitude across the gate oxide [1], [6] to minimize the leakage power in active mode. In current CMOS technologies, the sub threshold leakage current is much larger than the other leakage current components. Even in current-generation technology, sub threshold leakage

power dissipation is comparable to the dynamic power dissipation, and the fraction of the leakage power will increase significantly in the near future. Today's microprocessor designs devote a large fraction of the chip area [8] to the memory structures. High- performance onchip cache memories are a crucial component in the memory hierarchy of modern computing systems. In this technique each NMOS andPMOS transistors in the logic gates is split into two transistors. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the topNMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor. This reduces the power dissipation in logic circuits. This technique is implemented to BASIC gates such as AND,OR,XOR etc,COMBINATIONAL circuits such as FULLADDER,SEQUENTIAL circuits such as D-Flip-flop and also for memory cells such as 6TSRAM CELL.

2.IMPLEMENTATION OF EXISTING DESIGN

2.1 Full Subtractor

A full subtractor is a combinational circuit that performs a subtraction between two bits taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. The three inputs A, B and C denote the minuend, subtrahend and previous borrow respectively

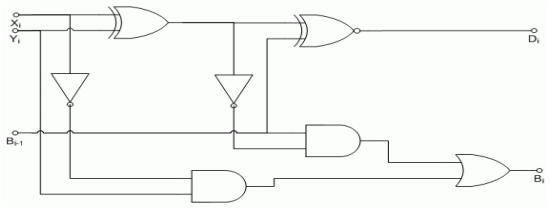


Figure 1. Gate Level Diagram of a Full Subtractor

The two outputs D and B represent the difference and borrow, respectively. The logic circuit for full subtractor is shown in Figure 1. The waveforms for the full subtractor shown in Figure 2 reflect the logic outlined in truth table.

TABLE I. Truth Table of Full Subtractor.

A	B	C	DIFFERENCE	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The simplified boolean functions for the outputs can be obtained directly from the truth table. The simplified logic equations are:

DIFFERENCE=A'B 'C + A'B C' + AB 'C' + AB C

BORROW = C(A'B' + AB) + A'B

Where A, B, C, are the inputs. D is output or difference and B is the borrow. The waveform of full subtractor is shown in figure.

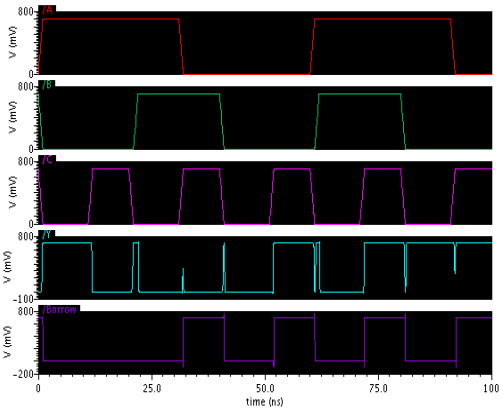


Figure 2.Waveform of Full Subtractor

3. PROPOSED DESIGN IMPLEMENTATION

3.1 Full subtractor using pass transistor logic

A sleep transistor is referred to either a PMOS or NMOS high Vth transistor that connects permanent power supply to circuit power supply which is commonly called "virtual power supply". The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit. The PMOS sleep transistor is used to switch VDD supply and hence is named "header switch". The NMOS

sleep transistor controls VSS supply and hence is called “footer switch”. In sub-90nm designs, either header or footer switch is only used due to the constraint of sub-1V power supply voltage.

3.2 Leakage power suppression

Significant amount of subthreshold leakage currents are produced when a nano scale integrated circuit is idle. Furthermore, transistors with no switching activity produce subthreshold leakage currents even in an ACTIVE integrated circuit. Leakage power has been increasing exponentially with the technology scaling. In 90nm node, leakage power can be as much as 35% of chip power. Consequently, leakage power reduction becomes critical in low-power applications such as cell phone and handheld terminals. Power-gating is the most effective standbyleakage reduction method recently developed . In the power gating, sleep transistors are used as switches to shut off power supplies to parts of a design in standby mode. Although the concept of the sleep transistor is simple, design of a correct and optimal sleep transistor is challenge because of many effects introduced by the sleep transistor on design performance, area, routability, overall power dissipation, and signal/power integrity. Currently, many of the effects have not been fully aware by designers. This could result in improper sleeper transistor design that would either fail to meet power reduction target when silicon is back or cause chip malfunction due to serious power integrity problems introduced. We have carried out comprehensive investigations on various effects of sleep transistor design and implementations on chip performance, power, area and reliability. In this paper, we shall describe a number of critical considerations in the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency. A sleep transistor is referred to either a PMOS or NMOS high Vth transistor that connects permanent power supply to circuit power supply which is commonly called “virtual power supply”. The sleep transistor is controlled by a power management unit to switch on andoff power supply to the circuit. The PMOS sleep transistor is used to switch VDD supply and hence is named “header switch”. The NMOS sleep transistor controls VSS supply and hence is called “footer switch”. In sub-90nm designs, either header or footer switch is only used due to the constraint of sub-1V power supply voltage

3.3 Ground bounce noise

During the active mode of the circuit an instant current pass from sleep transistor, which is saturation region and causes a sudden rush of the current. Elsewhere, because of self inductance of the off- chip bonding wires and parasitic Inductance on chip power rails, result voltage function in the circuit depends on input / output buffers and internal circuitry. The noise depends on the voltage.

4. LEAKAGE REDUCTION USING MTCMOS TECHNIQUE

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. This technique uses low, normal and high threshold voltage transistors in designing a CMOS circuit. Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current [5]. The low-threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path [2], [3]. The multi threshold CMOS technology has two main parts. First, “active” and “sleep” operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip [4]. These apply on between the low threshold voltage (low-Vt) gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as “power gating”.

The schematic of power gating technique using MTCMOS on full subtractor is shown in figure 3.

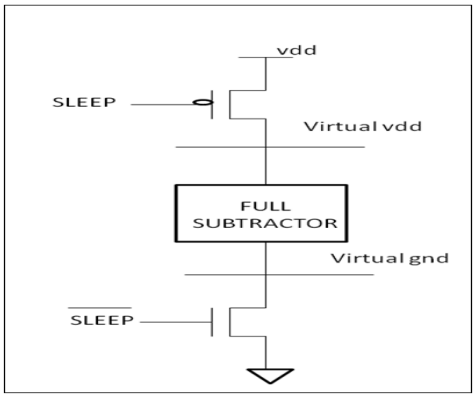


Figure 3. MTCMOS technique on full subtractor

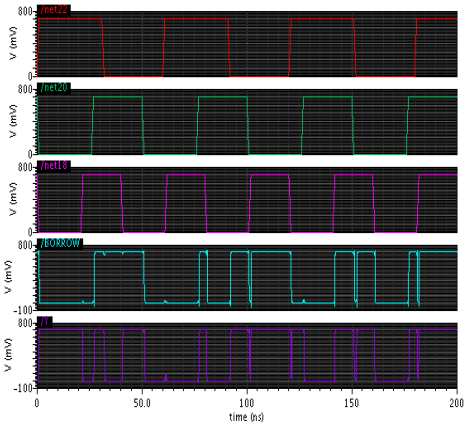
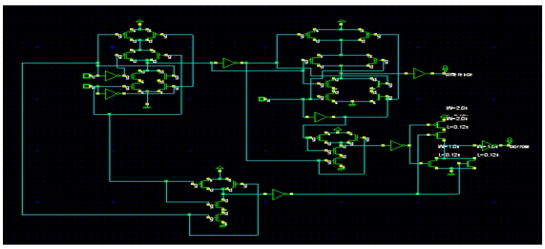


Figure 4. waveform of proposed full subtractor

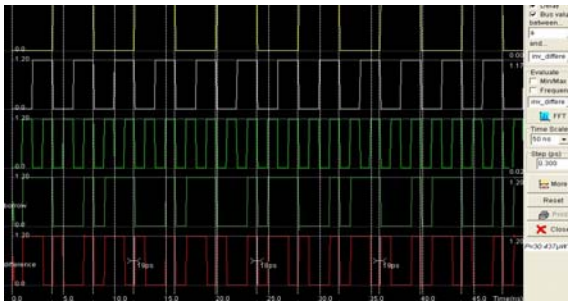
5. SIMULATION RESULT

A full subtractor subtracts 3input bits and gives the output in the form of difference and borrows. The simulation parameters have been analyzed with the help of the Microwind tool and DSCH for the schematic verification. By applying the MTCMOS technique in 60nm technology reduction in current and power is shown.

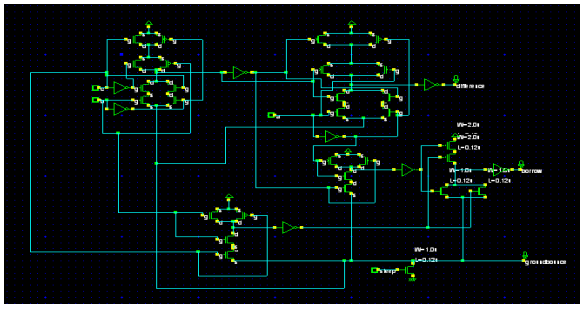
5.1 Full Subtractor Using CMOS Transistor



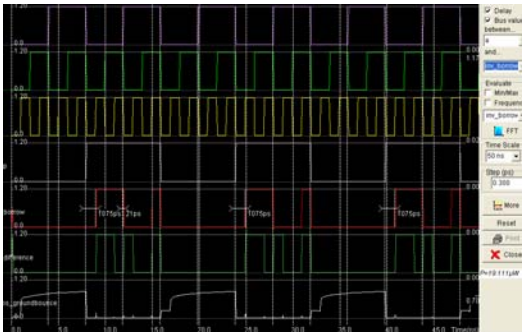
5.2 Power and Ground Bounce Noise Analysis



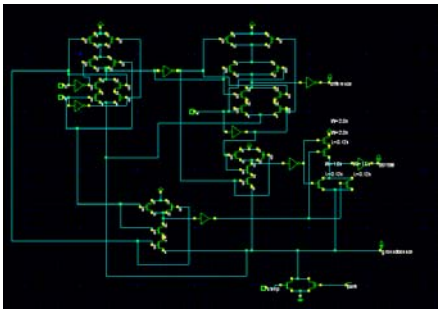
5.3 Full Subtractor Using CMOS in Sleep Mode



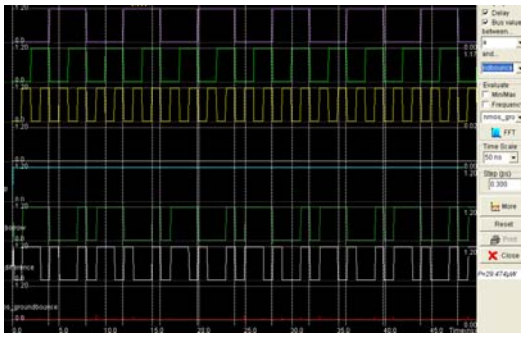
5.4 Power and Ground Bounce Noise Analysis in sleep mode



5.5 Full Subtractor Using CMOS Trimode



5.6 Power and Ground Bounce Noise Analysis in Trimode



6. CONCLUSION AND FUTURE SCOPE

In this paper, low leakage full subtractor cell is proposed for mobile applications with low ground bounce noise. Noise immunity has been carefully considered since significant threshold current of the low threshold voltage transition becomes more susceptible to noise. By using the proposed technique leakage power is reduced by comparison to the conventional cell (Base case). Ground bounce noise is reduced compared to Base case. Further, using the proposed technique the ground bounce noise is reduced in three designs (Base Case) compared to without applying the technique. Active power reduction is reduced in comparison to Base case. Noise immunity of proposed full sbtractor cell is reduced compared to the conventional subtractor cell (Base case). The proposed technique has been introduced with tri-mode technique for further reduction in the peak of ground bounce noise and overall power mode transition noise. The proposed full subtractor is designed with 120nm technology and operated with supply voltage.

In this we are concentrated on the leakage power analysis and ground bounce noise reduction,but the ground bounce noise is not removed completely. To remove ground bounce noise completely we should use triple phase sleep modulator ,so that the impact of ground bounce is completely removed ,but there is always a trade off between area ,speed and power.

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