DESIGN OF DATA TRANSMISSION SYSTEM BASED ON ETHERNET AND FIBER OPTIC LINK USING FPGA

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Abstract— Today's copper-based high-speed serial interfaces can deliver data at, multi-gigabit rates. Data transfer rates exceeding 100 Gbps are possible by using multiple lanes in parallel, but are limited in the distance they can travel. One approach that improves the distance is to use optical interconnect. This paper presents the design of FPGA based developmental board for real time data transmission using Ethernet and fiber optic link. With respect to the requirements, a hardware system with FPGA as the main control unit for logical interface, the Ethernet module and the fiber optic link as the data transmission channel communicating with the host computer is designed.

Index Terms— Ethernet, 100 Mbps fiber optic link, data transmission system, FPGA

I. INTRODUCTION

The ever-increasing quantity of data moving around the datacenter and over the Internet is straining the infrastructure as it struggles to keep up. Core functions such as the storage subsystems, the data switches and routers, and even the computing systems are now I/O limited. External data movement is limited by how fast and how far data can move through the cables and other interconnects that tie all the switches, routers, and storage arrays together. Hence in order to monitor the real time data of certain measurement control system, it is necessary to establish a data transmission system between host computer and measurement control system. Compared with the copper interconnects, the optical fiber has huge transmission capacity and excellent characteristics such as interference resistance, low attenuation, low maintenance cost etc. With the increasing demand for data transmission, a data transmission system with FPGA as the main control unit for logical interface, Ethernet module (wiznet) and the 100 Mbps fiber optic link as the data transmission channels communicating with the host computer is designed.

II. THE PROPOSED METHOD

The measurement control system transmits some random data to the host computer through the data transmission system. The flow of data is as follows:

- The data of measurement control system is sent over the fiber optic cable.
- This is received by optical transceiver of data transmission system. Then the data is sent to FPGA through external PHY chip DP83640 and wiznet W5300 chip.
- From FPGA the data is transmitted to host computer through wiznet module.

The proposed data transmission system is having the provision of transmission of data either through the fiber optic cable or through RJ45 via copper cable.

A. System Performance Requirements

For Optical fiber transmission, the transmission rate is around 100 Mbps of selected optical transceiver. In order to communicate with Optical fiber, the optical fiber interface is achieved using external physical layer (PHY) chip DP83640. The DP83640 supports both Twister Pair (100BASE-TX and 10BASE-T) and Fiber (100BASE-FX) media. The port may be configured for Twisted Pair (TP) or Fiber (FX) operation by strap option or by register access. At power-up/reset, the state of the RX_ER pin will select the media for the port. The default selection is twisted pair mode, while an external pull-down will select FX mode of operation.

The data transmission system operates at the maximum speed of 100 Mbps and hence accordingly it is designed.

B. System Architecture

The data transmission system is the bridge between the measurement control system and the host computer. The data coming from the measurement control system can be the random pre trigger signals of some detectors. The data is sent to the data transmission system via fiber optic and then it is sent to the host computer via the Ethernet after the data transmission system receives it. The host computer then processes the data according to the some specific requirement or logic and starts the transmission operation; the data transmission system sends the respective data to the measurement control system through the fiber optic after it receives the transmission instruction.

The data transmission is divided into four major functional modules, namely an optical interface module i.e; optical transceiver, Ethernet module (Wiznet module), media interface (MII) module, and the control unit i.e; FPGA.

The high-speed optical interface module is divided into the optical transmitter module and the optical receiver module. In accordance with the transmission characteristics of the optical fiber the optical transmitter module will encode the transmission data and serialize it, and modulate from the electrical signal to the light signal transmitted through the optical fiber; the optical receiver module detects the received optical signal, and convert it into an electric signal, and then extract the clock and recover the data.

Fig -1: Optical Transceiver module (AFBR-5803TZ)

C. System Hardware Architecture

The hardware structure of data transmission system includes optical fiber data transceiver part, Ethernet module for interfacing with host computer, the control unit FPGA and the power supply system. The optical transceiver is divided into the photoelectric conversion part and data encoding/decoding part. The special media interface chip is required for interfacing optical transceiver. This is achieved through media interface chip DP83640 Precision Phyter (External Physical Layer). The FPGA as the main control fulfils timing conversion and timing control. The design of the power supply system need to analyze the power type and the power consumption of the entire system, in order to determine the types of power supply and to choose the power chips.

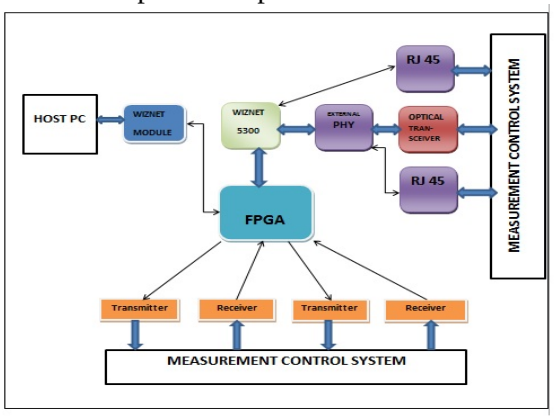

Fig -2: Architecture of Data Transmission system

The Host computer supply the +5V supply. The other power supplies such as 3.3V, 1.5V need to be conversed by various power functional chips. (1)

III. COMPONENT SELECTION

The various major components used for the design are listed below:

- Ethernet Module:- 100 Mbps WIZ-830MJ
- FPGA: Altera's Cyclone family, EP1C12
- W5300 Wiznet chip
- DP83640 Precision Phyter chip
- AFBR-5803Z Optical Transceiver
- HFBR-1119TZ Optical Transmitter
- HFBR-2119TZ Optical Receiver
- RJ-45 Integrated Magnetics

A. WIZ-830MJ

WIZ-830MJ is a network Module that includes W5300 (TCP/IP Hardwired chip, include PHY), MAG-JACK (RJ-45 with transformer). It has high network performance. It operates at 3.3V with 5V I/O signal tolerance. It includes hardware internet protocols such as TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP. It also includes hardware Ethernet protocols such as DLC, MAC.

B. EP1C12 FPGA

The flexibility and reconfigurability of FPGAs makes them an ideal solution for systems that demand a diverse set of high-speed I/O requirements. Along with the high-speed I/O capabilities, the FPGAs provide millions of configurable gates, lots of on-chip static memory, and additional dedicated system resources such as processor cores, phase-locked loops (PLLs), digital signal processing (DSP) blocks, PCI Express® (PCIe®) channels, and memory controllers. All the resources available on the FPGA allow designers to configure many system functions into the device's logic, thus reducing the number of circuits required on the system board. Additionally, the configurable nature of the FPGA allows designers to update the logic functions to add or remove features, patch logic bugs, or improve performance [4].

The Cyclone device family offers the following features:

- 2,910 to 20,060 LEs
- Up to 294,912 RAM bits (36,864 bytes)
- Supports configuration through low-cost serial configuration device
- Support for LVTTL, LVCMOS, SSTL-2, and SSTL-3 I/O standards
- Support for 66-MHz, 32-bit PCI standard
- Low speed (311 Mbps) LVDS I/O support
- Up to two PLLs per device provide clock multiplication and phase shifting
- Up to eight global clock lines with six clock resources available per logic array block (LAB) row
- Support for external memory, including DDR SDRAM (133 MHz),
- FCRAM, and single data rate (SDR) SDRAM

C. WIZNET W5300 CHIP

WIZnet chip W5300 contains the technology of full hardware logic of communication protocols such as TCP, UDP, IPv4, ICMP, IGMP, ARP and PPPoE. In order to provide high-performing data communication, the data communication memory is extended to 128kbyte and a 16bit bus interface is supported in W5300. Users can utilize 8 independent hardware SOCKETs for high-speed data communication.

W5300 supports BUS interface as the host interface. By using direct and indirect access methods, W5300 can be easily interfaced to the host like an SRAM memory. The data communication memory of W5300 can be accessed through TX/RX FIFO registers that exist in each SOCKET [5].

W5300 can provide Internet connectivity simply by setting some registers. When the initialization is successful, W5300 is available for data communication through Ethernet. After initialization, W5300 can transmit or receive data by opening the SOCKET's in TCP, UDP, IPRAW, or MACRAW mode. W5300 supports 8 SOCKETs to be used independently and simultaneously.

Fig -3: W5300 chip

The W5300 can be configured either in Internal PHY mode or External PHY mode using TEST MODE [3:0] select bits.

For internal PHY mode all the 4 bits are grounded or floated. The termination circuitry for internal PHY mode is shown below:

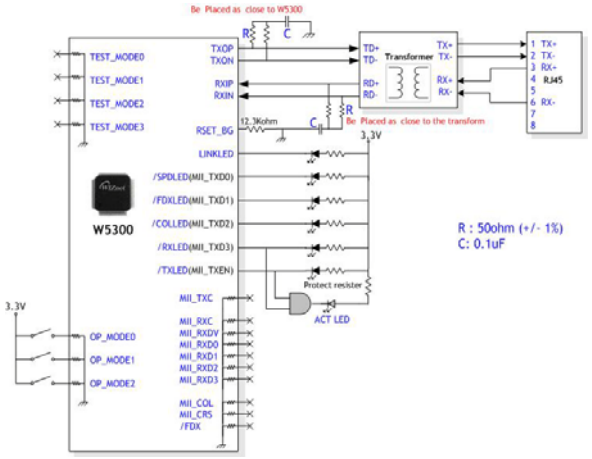

Fig -4: internal PHY & LED signals

If the internal PHY does not satisfy the user's requirements, an external PHY made by 3 rd party can be interfaced. In case of using external PHY mode, W5300 clock source should be selected. When TEST_MODE0 is logically high, a crystal is used, and when TEST_MODE1 is logically high, an oscillator is used.

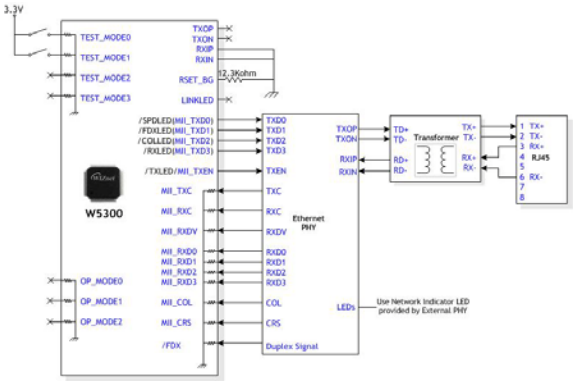

Fig -5: External PHY interface with MII

D. DP83640 Precision PHYTER

The DP83640 is a highly reliable, feature rich device suited for industrial applications. The DP83640 offers low power consumption, including several intelligent power down states. In addition to low power, the DP83640 is optimized for cable length performance far exceeding IEEE specifications. The DP83640 includes a 25MHz clock out. This allows the application to be designed with a minimum of external parts, which in turn results in the lowest possible total cost of the solution.

The DP83640 incorporates the Media Independent Interface (MII) as specified in Clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems. This section describes the nibble wide MII data interface. The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC).

This interface includes a dedicated receive bus and a dedicated transmit bus. These two data buses, along with various control and status signals, allow for the simultaneous exchange of data between the DP83640 and the upper layer agent (MAC) [6]. The receive interface consists of a nibble wide data bus RXD [3:0], a receive error signal RX_ER, a receive data valid flag RX_DV, and a receive clock RX_CLK for synchronous transfer of the data. The receive clock operates at either 2.5 MHz to support 10 Mb/s operation modes or at 25 MHz to support 100 Mb/s operational modes. The transmit interface consists of a nibble wide data bus TXD [3:0], a transmit enable control signal TX_EN, and a transmit clock TX_CLK which runs at either 2.5 MHz or 25 MHz. Additionally, the MII includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half Duplex mode. The COL signal asserts as an indication of a collision which can occur during half duplex operation when both a transmit and receive operation occur simultaneously [6].

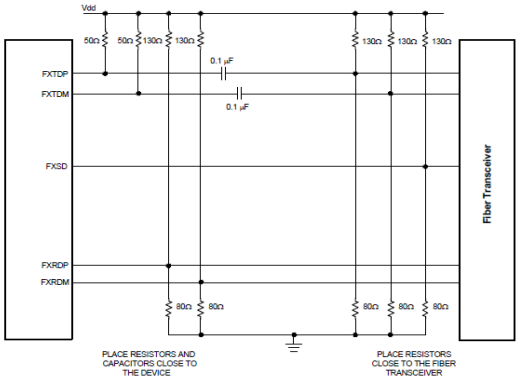

Fig -6: Circuitry for fiber interface with external PHY

E. AFBR-5803 Optical Transceiver

The AFBR-5803Z/5803TZ are 1300 nm products. The transmitter section of the AFBR-5803Z and AFBR-5805Z s-eries- utilize 1300 nm Surface Emitting InGaAsP LEDs. These LEDs are packaged in the optical subassembly portion of the transmitter section. They are driven by a custom silicon IC which converts differential PECL logic s-ignals-, ECL

referenced (shifted) to a +3.3V or +5V supply, into an analog LED drive current [7].

The receiver sections of the AFBR-5803Z and AFBR-5803Z series utilize InGaAs PIN photodiodes coupled to a custom silicon transimpedance preamplifier IC. The data output is differential. The signal detect output is single ended. Both data and signal detect outputs are PECL compatible, ECL referenced (shifted) to a +3.3 V or +5 V power supply.

F. HFBR-1119TZ Optical Transmitter and HFBR-2119TZ Optical Receiver

The HFBR-1119TZ/-2119TZ series of data links are high-

performance, cost-efficient, transmitter and receiver modules for serial optical data communication applications specified at 266 MBd for Fibre Channel applications. These modules are designed for 50 or 62.5 µm core multimode optical fiber and operate at a nominal wavelength of 1300 nm [8].

The transmitter utilizes a 1300 nm surface-emitting

InGaAsP LED, packaged in an optical subassembly. The LED is DC-coupled to a custom IC which converts differential- input, PECL logic signals, ECL-referenced (shifted) to a +5 V power supply, into an analog LED drive current.

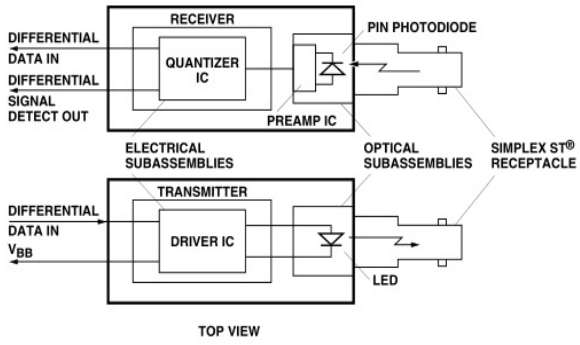

Fig -7: Transmitter and Receiver Block diagram

The receiver utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. The PIN-preamplifier combination is AC-coupled to a custom quantizer IC which provides the fi nal pulse shaping for the logic output and the Signal Detect function. Both the Data and Signal Detect Outputs are differential. Also, both Data and Signal Detect Outputs are PECL compatible, ECL-refer- enced (shifted) to a +5 V power supply.

IV. DESIGN

The design of the Data Transmission System using Ethernet and Fiber Optic link involves proper data flow between components whose control logic is designed in FPGA. The signals coming out from the measurement control system are sent to data transmission system via fiber optic cable which is received by optical transceiver. The optical transceiver consists of in built transmitter and receiver module. Hence the receiver receives the optical signal and convert it into an electric signal, and then extract the clock and recover the data. The output signal from receiver is fed to the external PHY chip DP83640 which is interfaced with optical Transceiver AFBR-5803Z. This chip then converts the received signal into equivalent 4 bits i.e; nibble wide data signal by using 100 Base-FX Receive logic employed in the chip. The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC). The receive interface consists of a nibble wide data bus RXD [3:0], a receive error signal RX_ER, a receive data valid flag RX_DV, and a receive clock RX_CLK for synchronous transfer of the data. The receive clock operates at 25 MHz to support 100 Mb/s operational modes. Similarly the transmit interface consists of a nibble wide data bus TXD [3:0], a transmit enable control signal TX_EN [6]. These nibble wide data signals are then sent to W5300 wiznet chip through RXD [0:3]. The wiznet chip then transfers these nibble wide data signals to FPGA and from FPGA the signals are finally given to WIZ830MJ Ethernet module. Finally the host computer receives those signals from the Ethernet module. W5300 chip and DP83640 chip both operate at 25 MHz clock speed. Hence 25 MHz crystal clock source is used.

In the Design individual Optical Transmitter and Optical Receiver is also used. These operate at +5V power supply. The input signal of transmitter and output signal of receiver are differential PECL logic signals. Since FPGA operates at 3.3V, single ended signals, level translator IC is used to convert 5V to 3.3V and vice-versa. Also in order to convert differential signals to single ended signals, PECL to TTL

convertor IC SN65ELT21 and TTL to PECL convertor IC SN65ELT20 is used.

All the differential signal paths are made short and of same length with equal termination impedance. Multilayered PCB is designed with separate digital plane, analog plane and ground plane. An impedance controlled PCB is designed. The PCB component placement diagram is shown below:

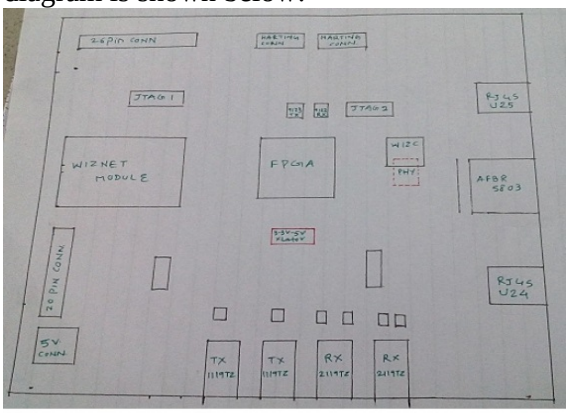

Fig -8: PCB Component Placement

V. SYSTEM SOFTWARE PART

The software implementation of the Data Transmission System is based on the Quartus II development Environment using top-down design ideas. The FPGA logic is written using Verilog code. For communication to take place between host computer and data transmission system we are using W5300 as the Ethernet controller. There are two methods to establish connection one is TCP-SERVER mode that is waiting for connection request. The other is TCP-CLIENT mode that sends connection request to a server. W5300 has total of eight SOCKETS each of which can be configured independently. When communication is established only one socket is active.

A. Test Code

The test code is written using Verilog code. The logic in FPGA is written for wiznet controller. The data in the FPGA is stored in FIFO memory of FPGA that is TX-FIFO and RX-FIFO. When the data is to be transmitted the wiznet controller reads the TX-FIFO of FPGA and stores it into TX-FIFO of the activated Socket of wiznet and When the data is to be received the wiznet controller reads the RX-FIFO of FPGA and stores it into RX-FIFO of the activated Socket of wiznet . Here we are using two sockets viz; socket 0 and socket7. Socket 0 is used as command port and socket 7 is used as data port. The wiznet controller performs the following function:

- Wiznet initialization
- Wiznet ROM initialization
- TCP socket 0 controller
- TCP socket 7 controller

Of the eight sockets only one socket is granted bus. The TCP can be operated either in Server mode or Client mode depending upon the register configuration.

B. Test Results

The test code is compiled successfully and it is debugged and burned into the target FPGA board. It is tested using off-the-shelf internet tool Hercules.

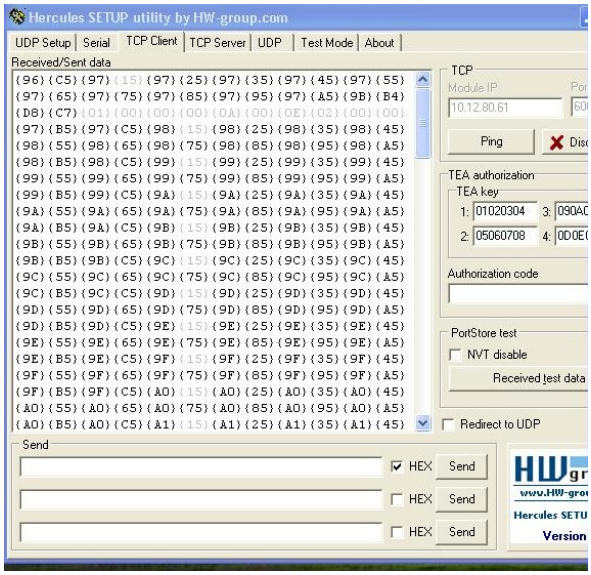

Fig -9: Hercules Test setup

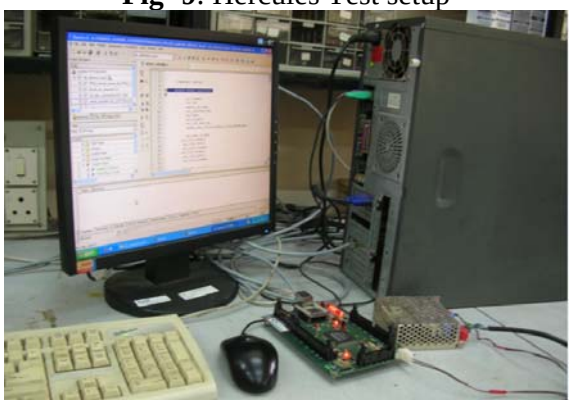

Fig -10: Hardware Test Setup

When the test is performed we observed that when the packet size is less, the number of packets received per second are large but as the packet size is less the data present in the packet is less. And when the packet size is increased, the number of packet received per second are less and hence the actual data processed is more.

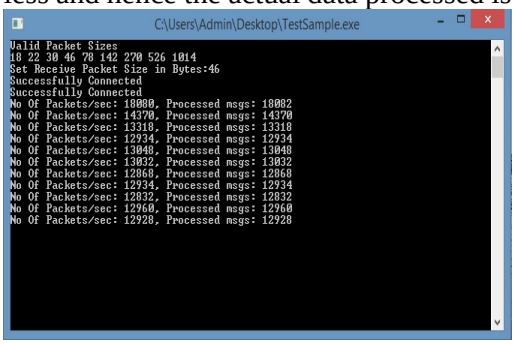

Fig -11: Test results

VI. CONCLUSION

The complete circuit schematics of Data transmission System is designed using Protel 99SE software tool according to PCB component placement with FPGA as the master control unit. The use of Fiber optic link in the system, transfer the data at a very high speed with negligible loss. Also the data can be transferred up to several kilometers without having to worry about losses. The program design of the proposed data transmission system based on the Verilog is detailed. The debugging of the test code is done with Quartus II development environment and it is tested on the FPGA board. The Test results shows that the data Transmission System program can be feasible and the Data Transmission System can be look as the bridge between the host computer and the measurement control system.

VII. REFERENCES

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