COMPARATIVE STUDY OF 64-BIT SRAM MEMORY USING 6T AND 7T SRAM CELLS

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Abstract: The growing market of portable electronics devices demands lesser power dissipation for longer battery life and compact system. With increasing technology, usage of SRAM Cells has been increased to large extent while designing the system On-chips in CMOS technology. Power consumption and the speed are the major factors of concern for designing a chip along with the leakage power. As Static Random Access Memory (SRAM) is used in high speed applications such as cache memory and occupies about 90% of silicon area. The one CMOS transistor leakage current due to various parameter is the vital role of power consumption. This article presents the simulation of 6T and 7T SRAM cells using low power reduction techniques and develops a modified model for the 64-bit memory cell that provides the consumer with a product that costs less and having reduced power delay product. All the simulations have been carried out on 90nm at Tanner EDA tool. The entire circuit verification is done using the Tanner tool.

Key words: Static random access memory (SRAM), bit lines; 6T, 7T VLSI.

1. INTRODUCTION

In present scenario everyone wants hand held electronics devices with high performance, high speed, long battery life and lot of features. Considerable attention has been paid to the design of low-power and high-performance SRAMs as they are critical components in both handheld devices and high-performance processors. Especially system on chip (SOC), and range of single chip memory has reached terabyte. But with the increase of size and interconnections between the cells in the circuits, power consumption and delay also increases which restricts the size of memory cells and its packaging [1]. In this paper we have calculated the dynamic power means short circuit power dissipation and extends low power cell to 64-bits.

2. BASIC SRAM ARCHITECTURE

Static random-access memory (SRAM or static RAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit [2]. But it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The basic SRAM cell design used bi-stable latching circuitry to store each bit. The two bi-stable states are 0 and 1, which are stored in cross coupled inverters. Both inverters have opposite values. The basic SRAM cell structure and the two stable states of the inverters are shown in fig-1(a) and 1(b) respectively. 6T SRAM cell is considers as the basic cell architecture, other kinds of SRAM architectures used 4, 8, 9, 10T or even more transistors to store single bit.

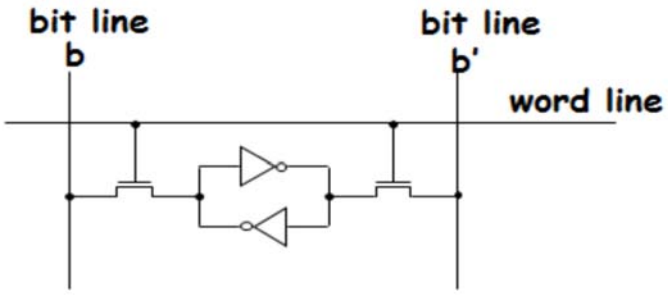

Fig-1 (a): Basic SRAM structure.

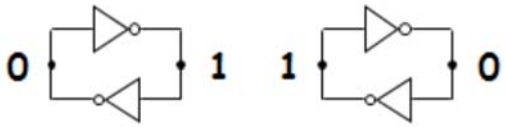

Fig-1(b): The two stable states of cross coupled inverters in SRAM cell.

Non-volatile SRAM -Non-volatile SRAMs have standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. Are used in a wide range of situations—networking, aerospace, and medical, among many others [3] -where the preservation of data is critical and where batteries are impractical. By transistor type-Bipolar junction transistor (used in TTL and ECL) – very fast but consumes a lot of power. MOSFET (used in CMOS) –low power and very common today. By function-Asynchronous – independent of clock frequency; data in and data out are controlled by address transition. Synchronous – all timings are initiated by the clock edge(s). Address, data in and other control signals are associated with the clock signals. By flip-flop type-Binary SRAM, Ternary SRAM.

3. CONVENTIONAL 6T SRAM CELL

The conventional 6T SRAM cell is shown in Fig 2. The cell consists of 4 NMOS and 2 PMOS transistors. Structure can be visualized as two cross-coupled inverters with two NMOS transistors as word select. The write and read operations are:

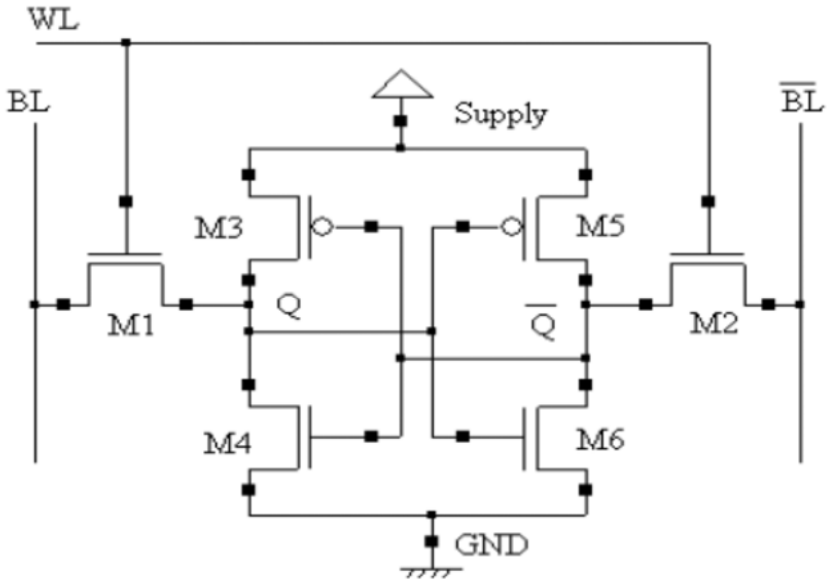

Fig2. Conventional 6T SRAM Cell [5]

a. Write Operation

In write operation two signals 'bI' and 'bIb' are generated from the input data such that 'bl' = data and 'bIb' = compliment of data. Then word line ('wI') is asserted which turns ON the access transistors m5 and m6 and the data will be written in the cell [6].

b. Read Operation

For read operation both bit lines ('bI' and 'bIb') are charged to a pre-charge voltage Vpre after that 'wI' is asserted, since the cell is already either in state '0' or in '1', then according to the state one line discharges to Gnd and a voltage difference is establishes between 'bI' and 'bIb' lines. Sense amplifier will sense this difference and stored bit will be available at the output of sense amplifier. From the working of 6T SRAM cell explained above, it is observed that power dissipation in SRAM can be divided into two parts. The first one is dynamic power, due to reading and writing of data, switching activity of transistors and charging and discharging of bit and bit-bar lines. Second is when the cells are in steady state, because of leakage current of the MOS transistors [6].

4. LOW POWER 6T SRAM CELL

Figure shows the write mode of low power SRAM cell. Word line is used for enabling the access transistors M1 and M2 for write operation. BL and lines are used to store the data and its compliment. For write operation one BL is High and the other bit line on low condition. In low power SRAM cell we introduced one Control signal transistor for controlling these transistors. But due to one more transistors area for low power SRAM cell is increased in comparison to Conventional approach. This control transistor uses control select signals which can be properly control the short circuit power dissipation. During write operation this transistor which has control signal works as in on condition. During read operation it will remain in off condition. When this transistor is in off condition will break the path which is in between Vdd and Ground.

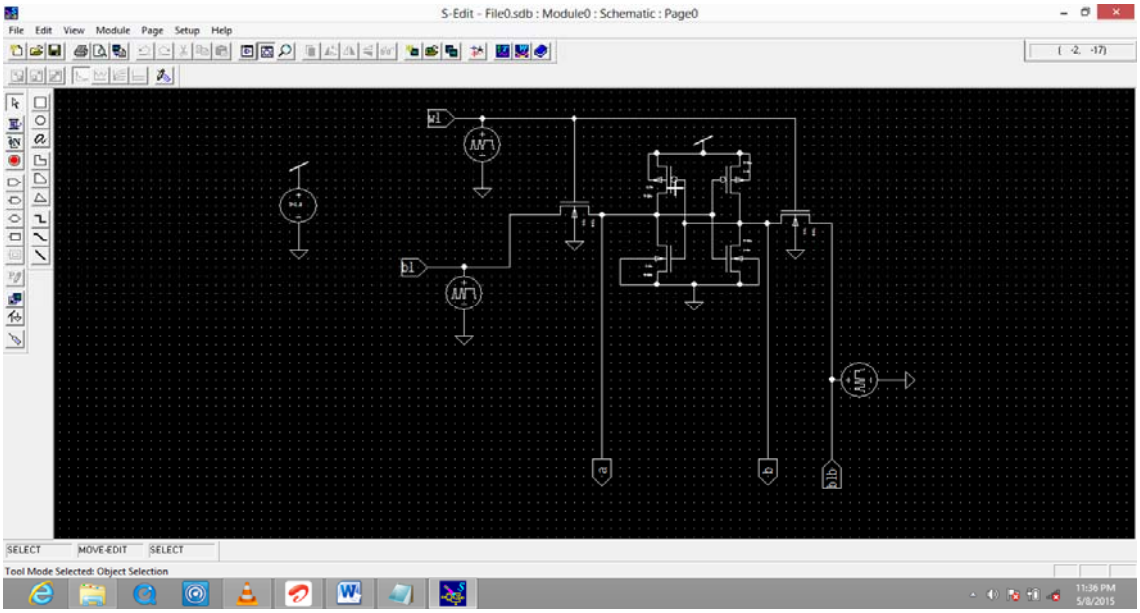

Fig3. Simulated Schematics of Low power 6-T SRAM cell

5. LOW POWER 7T SRAM CELL

The circuit of 7T SRAM cell is made of two CMOS inverters that connected to cross coupled pass NMOS transistors connected to bit lines and bit-lines bar respectively. Fig-4 shows circuit of 7T SRAM Cell, where the access transistors MN3 is connected to the word-line (WL) to to each other with additional NMOS Transistor which connected to read line and having two

perform the access write and MN4 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL and BLB). Bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation, or from write in the memory cells during write operations. All transistors have minimum length (LMIN =90nm according to used Technology), while their widths are typically design parameters. The value of WP1 and WP2 defines PMOS transistors width and WN1 and WN2 defines the NMOS driver transistors width use in CMOS Invertors, while WN3 and WN4 is the access transistors width.

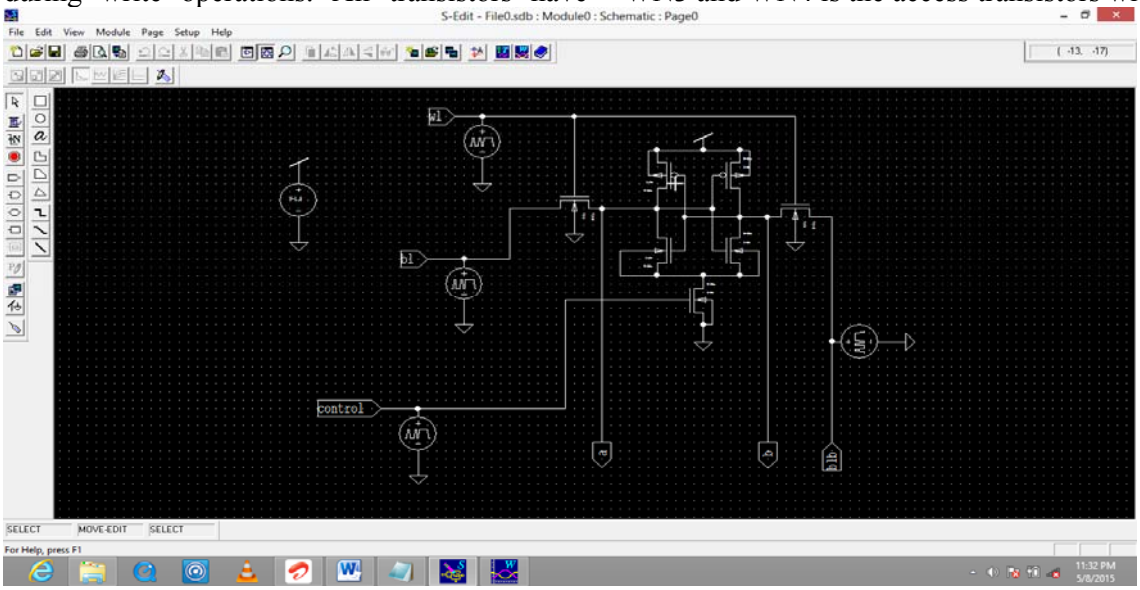

Fig4. Simulated Schematics of Low power 7-T SRAM cell

6. SIMULATED SCHEMATICS USING TANNER TOOL

All the circuits have been simulated using 90 nm technology on Tanner EDA tool. To make the impartial testing Environment all the circuits have been simulated on the same input patterns. Here, above one-bit SRAM cell using 6T and 7T is extending to store 64-bit (i.e. 8rows and 8 columns).

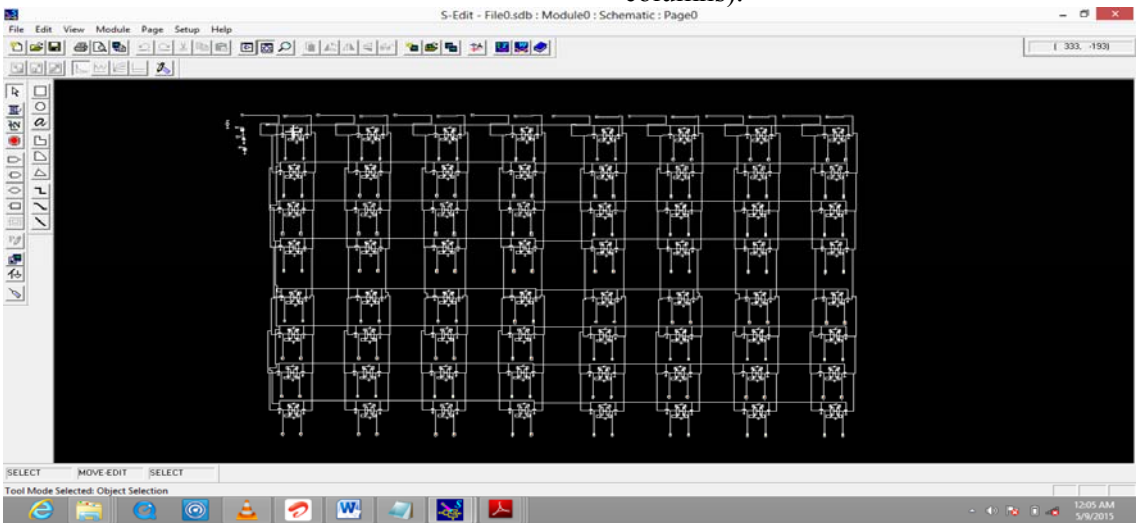

Fig5. Schematic of 64-bit memory SRAM Cell using 6T (i.e. 8 rows and 8 columns)

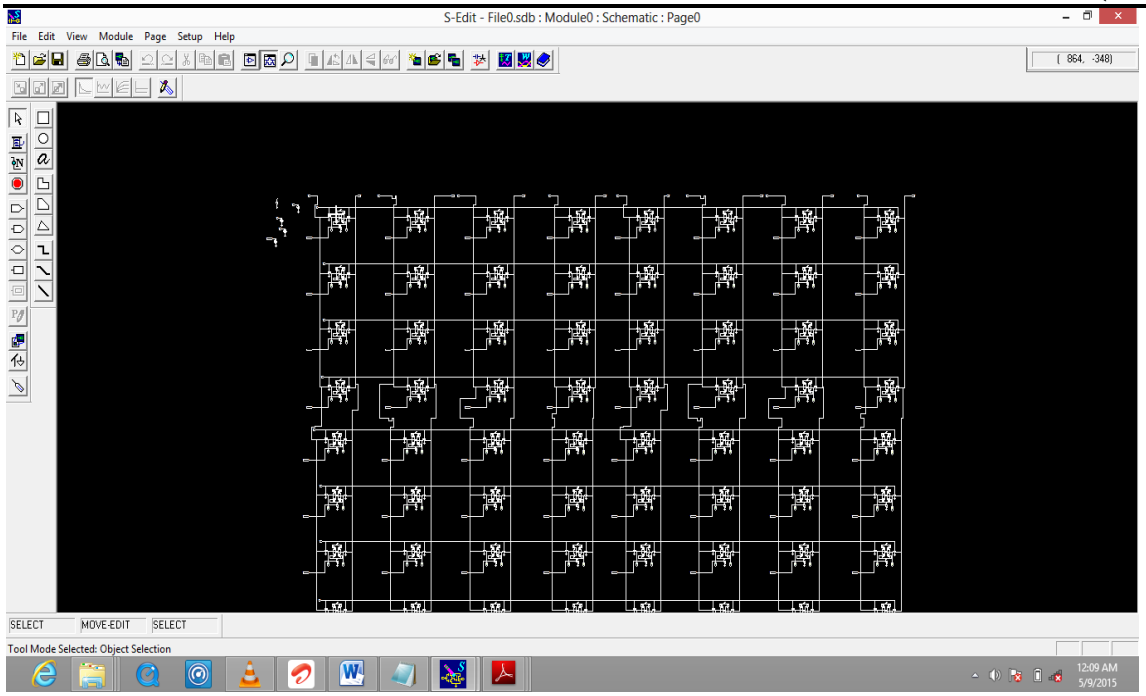

Fig6. Schematic of 64-bit memory SRAM Cell using 7T (i.e. 8 rows and 8 columns)

7. SIMULATED WAVEFORMS RESULTS

The work has been developed using Tanner Tool version 7. And the waveform shows the Read/Write Waveforms of SRAM Cell at different technologies. Here v(wl) v(blb) v(bl) are the inputs and v(a) v(b) are the outputs.

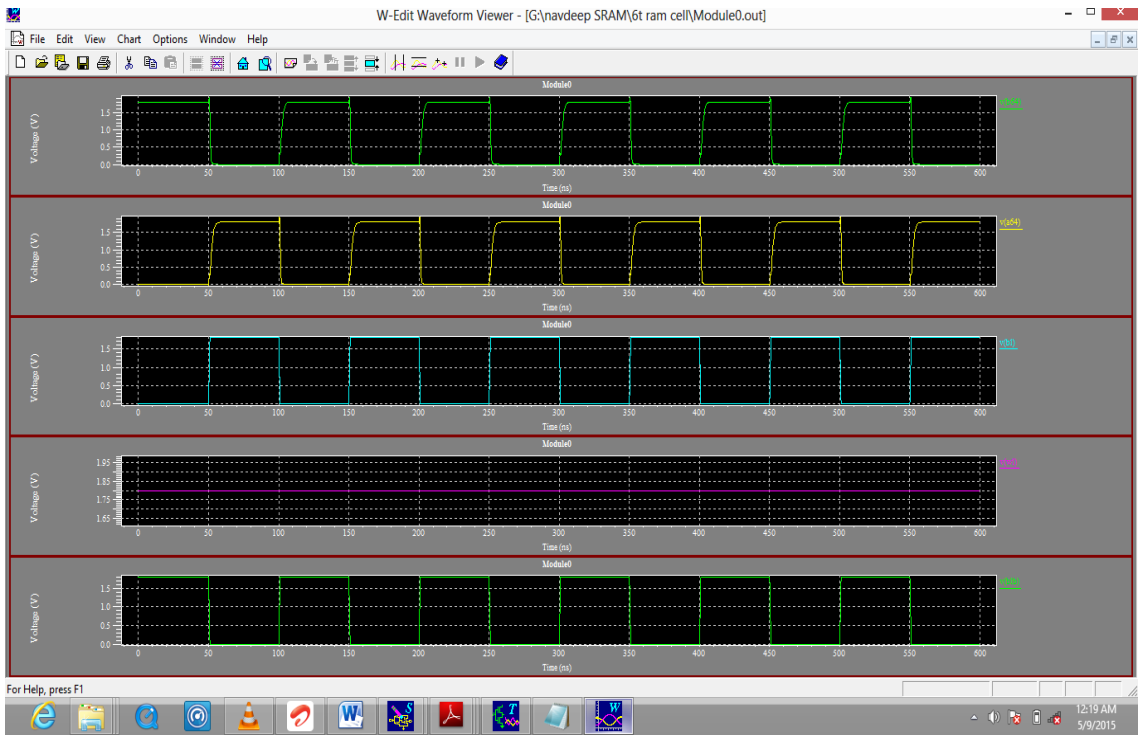

Fig7. Read/Write Waveforms of 64-bit SRAM Cell using 6T at 90nm

Fig8. Read/Write Waveforms of 64-bit SRAM Cell using 7T at 90nm

8. RESULTS AND COMPARATIVE ANALYSIS

All memory cells are simulated using T-SPICE 7.1v. In this section, comparison based results are presented in following tables. These results have been obtained from simulation of 6T memory cell and 7T memory cell in asymmetric configuration at the 90nm technology. And simulation of 64-bit SRAM memory cell in asymmetric configuration at the different configurations (i.e.6T and 7T).

Table1. Simulation results of 1-bit SRAM Cell for area, power and delay.

Design style	No. of transistors	Technology file (µm)	Avg. power consumptions (watts)	Prop. Delay at a (sec)	Prop. Delay at b (sec)
SRAM	6	0.90	$3.83x10^{-10}$	$9.15x10^{-10}$	$9.15x10^{-10}$
SRAM	7	0.90	$3.71x10^{-10}$	$8.99x10^{-10}$	$8.99x10^{-10}$

Table2. Simulation results of 64-bit SRAM Cell for area, power and delay.

Design style	No. of transistors	Technology file (µm)	Avg. power consumptions (watts)	Prop. Delay at a64 (sec)	Prop. Delay at b64 (sec)
SRAM	384	0.90	$2.47x10^{-3}$	$2.82x10^{-10}$	$9.15x10^{-10}$
SRAM	448	0.90	$2.39x10^{-3}$	$2.55x10^{-10}$	$8.95x10^{-10}$

9. Conclusions

The most efficient technique to reduce the power dissipation is the reduction of the supply voltage. The power dissipation reduction in SRAMs is not only due to power supply voltage reduction, but also due to operating frequency and temperature. Technology scaling demands a decrease in both Vdd and Vt to sustain delay reduction, while restraining active power dissipation. The 7T SRAM memory is designed to accomplish read stability. The total power consumption is also significantly lower as compared to the existing 6T SRAM memory system. So 7T SRAM memory can be used in internal CPU.

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