A REVIEW ON HIGH PERFORMANCE2:1 MULTIPLEXERS

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Abstract: Design of low power circuit for high performance is the essential priority of VLSI tech. The present paper shows the analysis for various available 2:1 mux design using Tanner EDA tool and improved version of 2:1 MUX is also simulated in Dsch (digital schematic) and microwind 3.5 version tool for optimized logic verification and area estimation of circuit design respectively.

Index Terms—power consumption, speed of operation, CMOS logic

[1] INTRODUCTION

Today is the era of portable system but it limits power consumption as a result there is a demand to design low power circuit to fulfill the present consumers need.The essential requirement behind these developments are miniaturized device applications. The miniaturized device require low power consumption and high throughput due to their small chip size with large density of components.it increases the complexity of the circuit and high frequencies to operate.the miniaturized devices may consist of many components like adder subtractor, multiplexer, demultiplexer, shifters, ALU,etc. according to type of application designed. A2:1 multiplexer is a basic building block used as programmable logic devices.logic circuits are implemented as combination of switches,rather than logic gate. So 2:1 multiplexer is a playing key role for designing switch logic.the basic architecture of 2:1 mux is shown in the following figure.

II LITERATURE REVIEW OF VARIOUS CIRUITS USING 2:1 MULTIPLEXER

2.1 NMOS 2:1 MULTIPLEXER CIRCUIT

The logic diagram of NMOS 2:1 MUX is shown in Fig.1(a). There are two select lines S,S1 and inputs are a,b. Gate terminals of NMOS are connected with select lines.This circuit is based on Complementary Pass Transistor Logic[1,2].

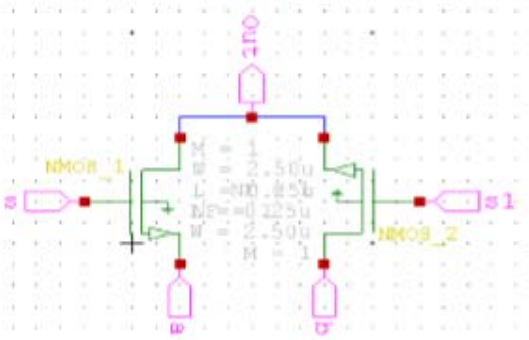

Fig 1 logic diagram of NMOS 2:1 MUX

Advantage:Eliminates redundant transistor so number of count of transistor reduces.

2.2 CMOS 2:1 MULTIPLEXER CIRCUIT

The Fig. 1(b) shows the logic diagram of CMOS 2:1 multiplexer based Double Pass Transistor Logic. DPL reduce some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors

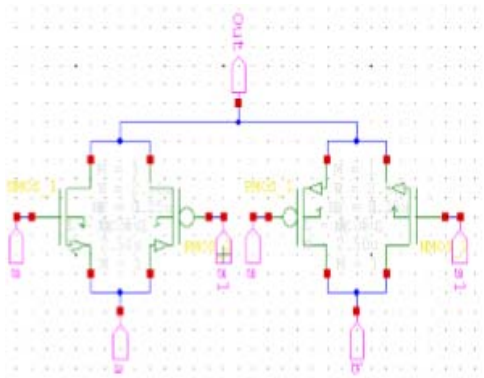

Fig 2 logic diagram of CMOS 2:1 MUX

Advantage:While it has high speed due to low input capacitance.
Limitation: It has only limited capacity to drive a load .

2.3 MSL (MUX single with level restoration block) 2:1 MULTIPLEXER CIRCUIT:
The logic diagram of MSL.The complementary pass transistor logic [1]requires both non inverting and inverting signals as inputs, so the larger area will be occupied by 2:1 MUX. So to eliminate this drawback of circuit only the non inverting input signal is used which is output of complementary pass transistor logic multiplexer acts as input to p-latch inverter.

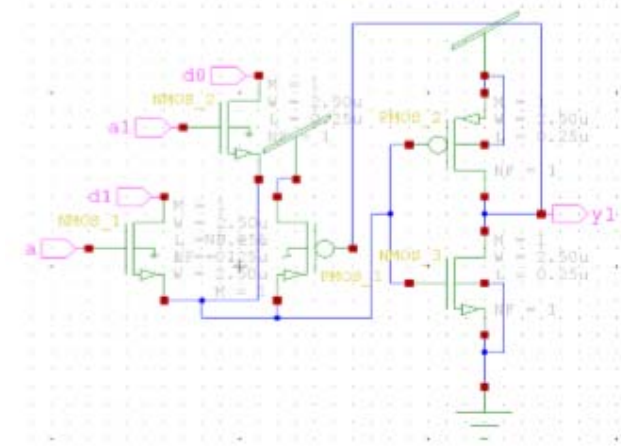

Fig 3 logic diagram of MSL 2:1 MUX

Advantage:This new logic design uses only non inverting output of CPL.
2.4 *MD (multiplexer double) 2:1 MULTIPLEXER CIRCUIT*:

The above figure 4 shows the circuit of MD 2:1 mux, the MD means for Multiplexer Double [6]. In this design double means we get output and its inverted output respectively.In this circuit a and a1 are select lines, d1 and d0 are data input lines and y and y1 are output and its inverted output respectively.

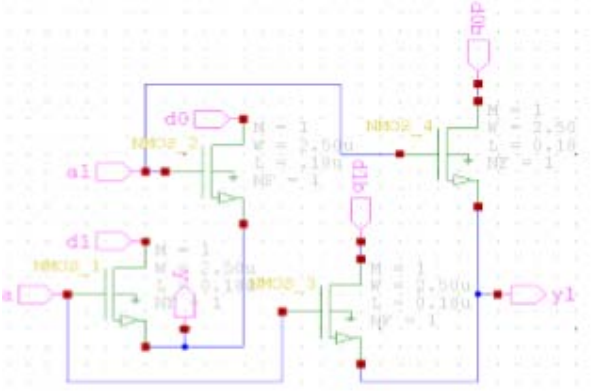

Fig 4 logic diagram of MD 2:1 MUX

2.*5 MDL 2:1 MULTIPLEXER CIRCUIT*
The logic diagram of MDL[6] 2:1 mux circuit is shown in fig 5. MDL stands for multiplexer double with level restoration block.with addition of restoration block we can avoid swing problems and this is the main advantage of circuit.

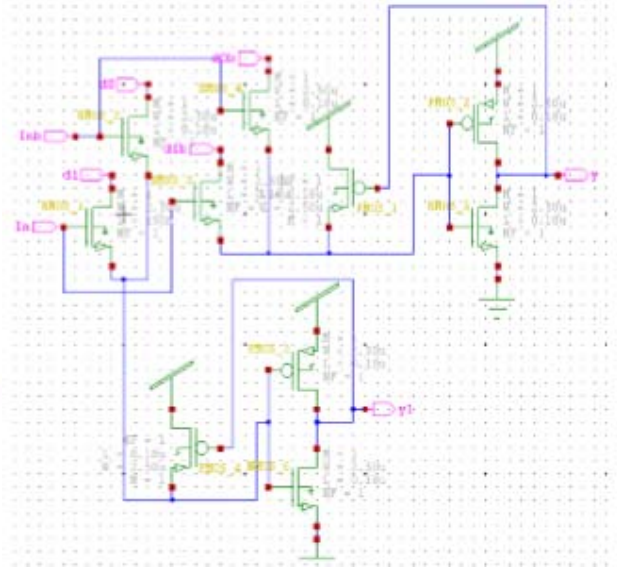

Fig 5 logic diagram of MDL 2:1 MUX

Disadvantage :Due to large number of MOS device used in this circuit it consumes high power and required high-area.

2.6 DCVSL 2:1 MULTIPLEXER CIRCUIT:

Fig 6 is depicting the circuit diagram of DCVSL . The major advantage of DCVSL are consumes no static power like CMOS. Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family [2,,3]which is designed

for certain advantages. A logic function and its inverse are automatically implemented in this logic style.The pull-down network implemented by the NMOS logic .

Fig 7 shows the design of DCVSL in Dsch (digital schematic) tool.

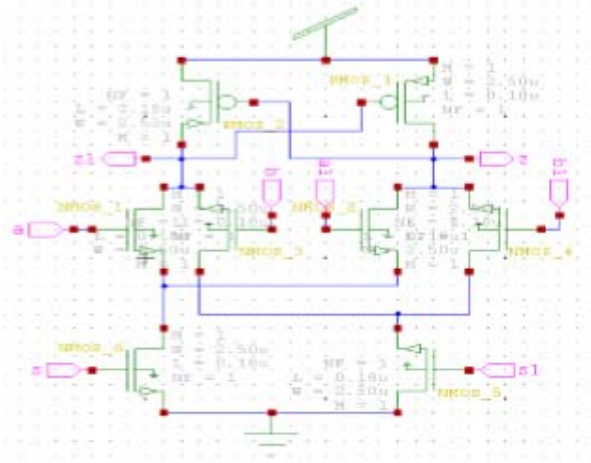

Fig 6 logic diagram of DCVSL 2:1 MUX

Advantage:The most important benefits of DCVSL are it consumes no static power as CMOS.due to absence of PFETS from each logic function the logic density of circuit is improved.

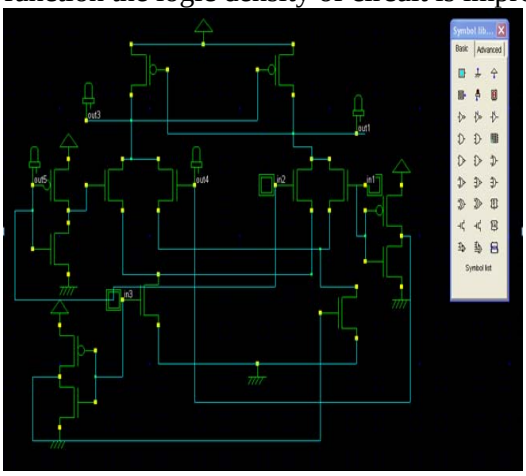

Fig 7 Digital schematic of DCVSL 2:1 MUX

2.7 MDCVSL 2:1 MUX

Figure 8 shows that MDCVSL 2:1 mux[7] which consist s and s1 select line, a and b data inputs, a1 and b1 are inverted data inputs and z and z1 are output and its complement respectively.

Fig 9 shows the layout design of MDCVSL using microwind 3.5 version tool ,which helps us to find the area required to design this circuit on chip.

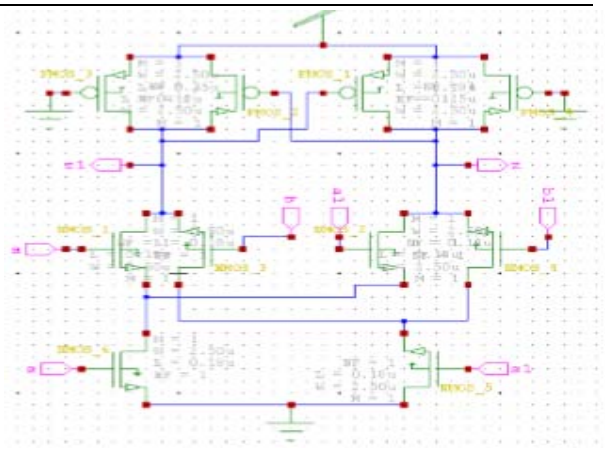

Fig 8 logic diagram of MDCVSL 2:1 MUX

Advantage:In the above design due to excess added transistors so reduction in threshold loss occur,which further causes the reduction in overall power consumption of the circuit.

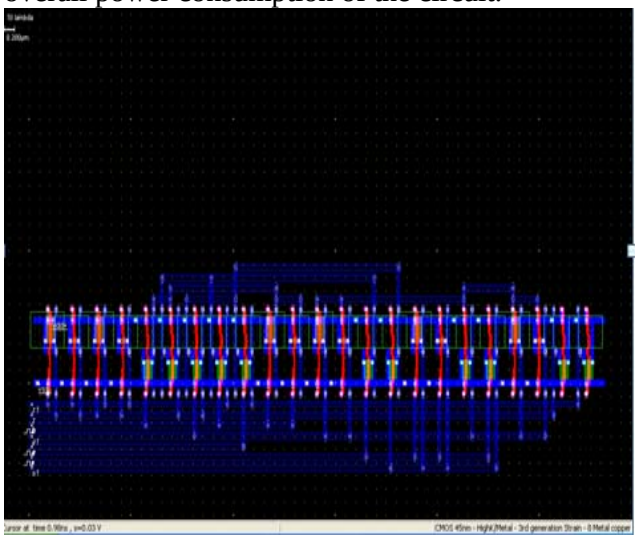

Fig 9 Layout diagram of MDCVSL 2:1 MUX for area estimation on chip

SIMULATION AND COMPARISON

All the circuits have been designed using tanner EDA tool . Tanner EDA provides a complete line of EDA software that drive innovation for the design, layout, and verification to tape-out of analog and digital integrated circuits (ICs). Tanner EDA offers a complete design environment support.

DCVSL multiplexer shown in fig 7.is designed using Dsch tool also because the DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation

with delay analysis, which allows the design and validation of complex logic structures. .

MDCVSL layout diagram is obtained using microwind 3.5 version which allows us to find out the area consumed by the circuit on IC. MICROWIND is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination. MICROWIND integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities.

CONCLUSION

The most essential requirement of optimized circuit designed using VLSI technology is least power consumption and high speed of response. This paper provide us the high performance 2:1 MUX for designing of any application like arithmetic and logic unit, shifter, rotators, barrel shifter etc.so by keeping above criteria in mind. we can conclude MDCVSL 2:1 MUX is best in term of static, dynamic power dissipation and more accuracy in results can be obtained when we simulate the design using Dsch and microwind tool.

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