A NEW MULTILEVEL INVERTER TOPOLOGY WITH REDUCED NUMBER OF SWITCHES

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Abstract -- Multilevel inverters are generally used in medium-voltage and high-power applications. The new structure of multilevel inverter proposed in this paper uses less number of switches compared to conventional topologies. Hence provides lower switching losses and economically advantageous unit than conventional cascaded H-bridge inverter. The new multilevel inverter topology suggested here is simulated using level shifted carrier pulse width modulation technique for gate signals for switches. This structure allows reduction of the system cost and size. Effectiveness of the proposed topology has been demonstrated by comparative analysis and simulation.

Index Terms-- Multilevel systems, Circuit topology, Pulse width modulation inverters.

I. INTRODUCTION

The Multi-Level Inverter (MLI) has been the life of the modern day medium and high voltage power electronic device based applications. It can provide higher voltages with nearly sinusoidal voltage waveforms. Owing to different switching strategies, it has been now possible to control the lower order harmonics in the multilevel inverter output voltage.

Some of the widely used MLI are Neutral Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-bridge (CHB). They have become popular due to their modular structure and ability to produce quality sine wave in their output with fewer harmonic [1]. Yet the losses in the inverter, optimal use of switches and reduction in required number of switches have been the matter of interest in research. Different carrier based PWM techniques are explained that helped in selecting suitable PWM strategy for the proposed topology in [2-3]. Based on the study of different topologies in [4-6], the scope of new topologies with reduced number of switches in MLI design can be realized.

Many new topologies have been suggested to reduce the switches and hence losses occurring in the MLI. The presented topology reduces the losses by reducing the number of switches for given number of output voltage levels. To produce m voltage levels in the output of the MLI, (m+1) power electronic semiconductor switches are used. Compared to conventional topologies the number of switches used is less and hence the losses in the MLI are less.

In the presented paper, section-II describes in brief the Cascaded H-Bridge MLI topology as the presented topology is going to be compared with it. The proposed MLI topology and its basic working are discussed in section-III. For the presented MLI topology, the control strategy using PWM techniques is described in section-IV. In section-V, the simulation results of the proposed MLI topology are presented. The comparative analysis of proposed MLI topology with the conventional topologies is presented in section-VI. Section-VI contains the conclusion.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascade Multilevel Inverter (CMLI) is one of the most important topologies in the family of multilevel inverters [1]. It is built to synthesize a desired AC voltage from several levels of DC voltages. The DC levels are considered to be identical since all of them are batteries, solar cells, etc. [2], [3]. It requires least number of components when compared to diode-clamped and flying capacitors type multilevel inverters and no specially designed transformer is needed as compared to multi pulse inverter [3],[4],[6]. A cascaded multi-level inverter consists of a number of H-bridge inverter units with separate dc source for each unit and it is connected in cascade or series as shown in Fig.1 [1].

Each H-bridge can produce three different voltage levels: +E, 0 and -E by connecting the dc source to ac output side by different combinations of the four switches S1, S2, S3, and S4.

The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs [5].

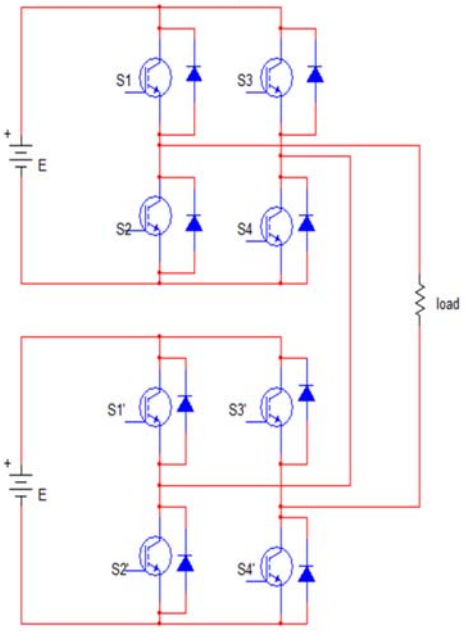

Figure 1 Single phase structure of a multilevel cascaded H- bridge inverter

The number of output phase voltage levels, m, in a cascade inverter is defined by m=2s+1, where s is the number of separate dc sources. The phase voltage of m level multilevel inverter can be given as:

$$V_{an} = E_1 + E_2 + E_3 + \cdots + E_{[(m-1)/2]}.$$

III. PROPOSED TOPOLOGY

In many of the well-known multilevel inverter topologies, the required number of power electronics devices depends on the voltage level. However, increasing the number of power semiconductor switches also increases the inverter circuit size, cost, and installation area and control complexity. To provide higher number of output levels with reduced number of switches, a new topology for multilevel inverter is proposed in this paper. Fig. 2 shows proposed five-level MLI topology.

With this topology five levels are obtained in output that is +2E, +E, 0,-E & -2E if only one module as shown in Fig. 2 is used, where the E is the value of voltage of a single DC source. Here (m-1)/2 number of DC sources of equal values are used for producing m levels in output voltage waveform. The circuit connection for producing m = 5 levels is shown in Fig. 2.

The switching table for proposed five-level inverter is given in Table I. For value of voltage level E and –E the diodes D4 and D5 conducts. Thus diodes D4, D5 does not only work as freewheeling diodes but also as active switches carrying load currents.

The proposed structure is modular that allows increase in MLI output level by adding the module as shown in Fig. 2. One can add number of modules to increase levels in

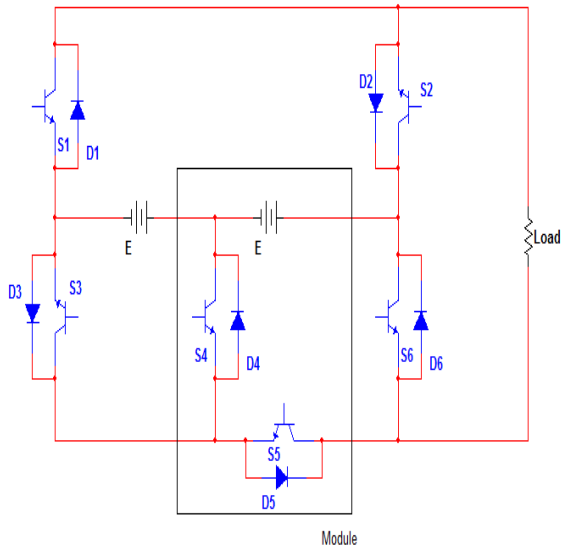

Figure 2 Basic unit of proposed multilevel inverter

TABLE I
SWITCHING TABLE FOR PROPOSED FIVE LEVEL MLI

Sr. No.	Voltage level	Switches(1= ON, 0= OFF)						
		S1	*S2*	*S3*	*S4*	*S5*	*S6*	*Conducting diode*
1	+E	0	1	0	0	1	0	D4
2	+2E	0	1	1	0	1	0	-
3	0	0	0	0	0	0	0	-
4	-E	1	0	0	1	0	0	D5
5	-2E	1	0	0	0	0	1	-

output voltage. As we increase the number of modules, with each module, two more switches are added and two additional levels can be obtained in the inverter's output phase voltage.

IV. PWM SIGNAL GENERATION FOR PROPOSED MLI SWITCHES

For switching of this inverter switches, the level shifted carrier PWM technique has been used. Four signals are generated by comparing four level shifted triangular waveforms with single sine wave as shown in Fig. 3.

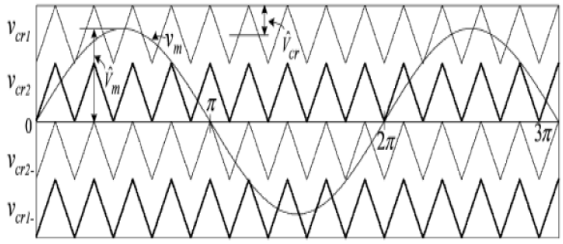

Figure 3 Four level shifted carrier and a reference sine signal [2]

These four signals are further combined to create six gate signals for six inverter switches which are placed in MLI as shown in Fig. 2.The simulation block diagram of gate signal generation is shown in Fig. 4 and Fig.5.

V. COMPARISON OF PROPOSED MLI TOPOLOGY WITH CONVENTIONAL CASCADED H-BRIDGE INVERTER AND OTHER CONVENTIONAL TOPOLOGIES

Compared to conventional cascaded H- bridge inverter, where for m levels, the numbers of switches used are 2*(m-1) per phase, in this topology the number of switches used are (m+1) for m levels. For example if we take five level inverter then in cascaded H-bridge inverter the number of switches used are 2*(5-1) = 8 while in this topology the number of switches used will be (5 + 1) = 6. Thus requirement of switches are reduced by two in this case.

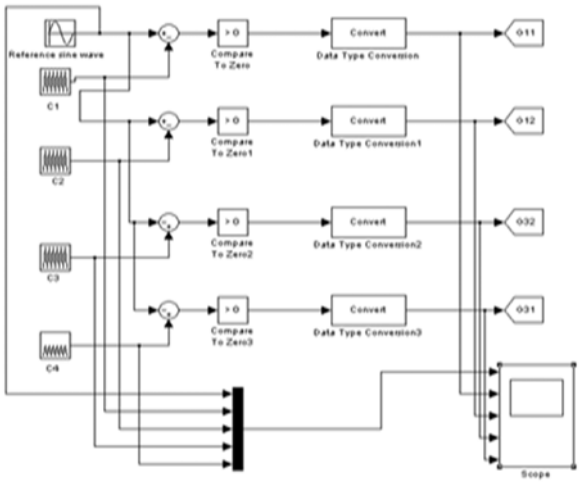

Figure 4 Signal generation using level shifted carrier sine PWM

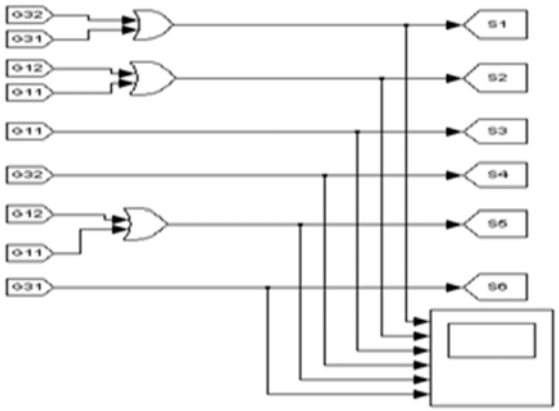

Figure 5 Gate signal generation for six inverter switches from four signals obtained from level shifted carrier PWM

The comparison of number of switches used in cascaded H-bridge MLI and proposed MLI for 5, 7 and 9 voltage levels MLI is presented in the Table II.

TABLE II
COMPARISON OF CASCADED H-BRIDGE AND PROPOSED MLI FOR NUMBER OF SWITCHES USED FOR 5, 7 AND 9 VOLTAGE LEVELS

	Cascaded H-bridge MLI		Proposed MLI	
Number of Voltage levels	1-phase	3 - phase	1-phase	3 - phase
	No. of switches used	No. of switches s used	No. of switches used	No. of switches use
	(2*(m-1))	3*(2*(m-1))	(m+1)	3*(m+1)
5	8	24	6	18
7	12	36	8	24
9	16	48	10	30

From the comparison study, it can be observed that for three-phase 9-level MLI circuit (48-30) =18 switches can be saved. In general with this topology, for an inverter producing m levels in output voltage waveform, (m-3) switches can be saved (Reduced) compare to cascaded H-bridge multilevel Inverter. Even the number of switches taking part in conduction is also less in presented MLI compared to CHB. The maximum number of switches taking part in conduction in five level CHB MLI is Four while in the said topology the maximum number of switches taking part in conduction is three.

With reduced number of switches, losses can be reduced as well as considering bulk production of units; it can turn into significant savings.

VI. MATLAB SIMULATION AND RESULTS FOR FIVE LEVEL AND SEVEN LEVEL MLI OF PROPOSED TOPOLOGY

The proposed topology for single phase five level and seven level MLI has been simulated for combined resistive and inductive load (RL load) using MATLAB/simulink using level shifted carrier based PWM technique. Fig. 6 shows the MATLAB/simulink model of proposed five-level topology.

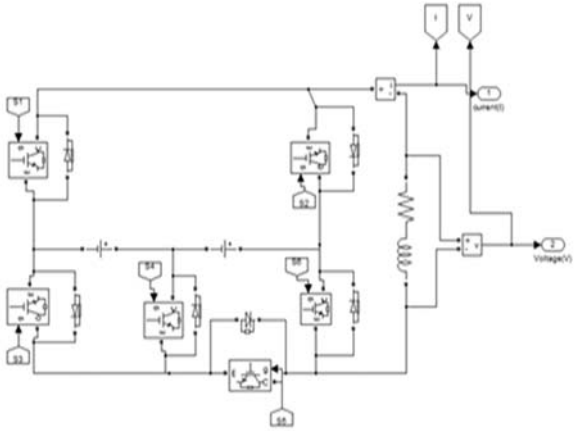

Figure 6 Simulink block diagram of proposed MLI topology for single phase five output voltage level.

The simulation of proposed five-level MLI is carried out in continuous mode using following parameters:

DC source voltage E = 100 V.
Resistance(R) of load = 12Ω.
Inductance (L) of load = 3.82mH.
Fundamental frequency = 50 Hz
Carrier frequency = 750 Hz

The resulting output phase voltage is shown in Fig. 7.

The FFT analysis has been done in the MATLAB for the five level inverter output phase voltage waveform. Total Harmonic Distortion (THD) is observed to be 19.21 % as shown in Fig. 8.

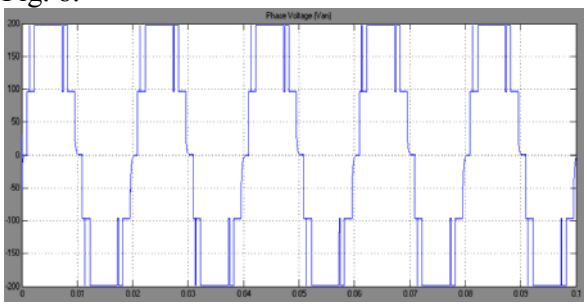

Figure 7 Five Level output phase voltage waveform for RL Load

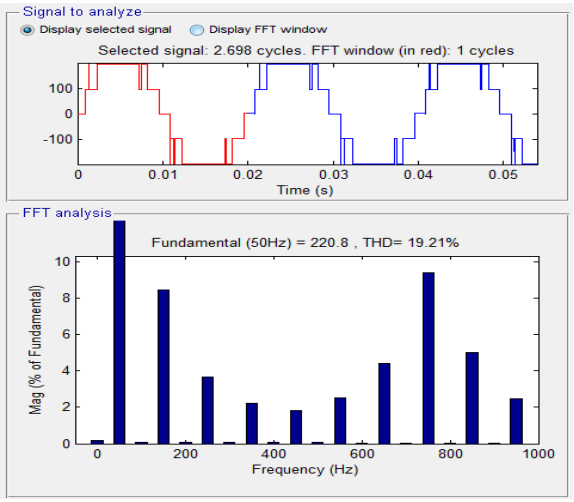

Figure 8 FFT analysis of output phase voltage waveform of five level MLI of proposed topology.

The simulation is also preformed for seven-level structure of proposed topology in order to validate the feasibility of the said topology using an additional module consists of one extra DC source of E = 100 V and two more switches as shown in Fig. 2. The simulation model parameters for seven level MLI are same as used for five-level topology. The resulting output phase voltage waveform is shown in Fig. 9.

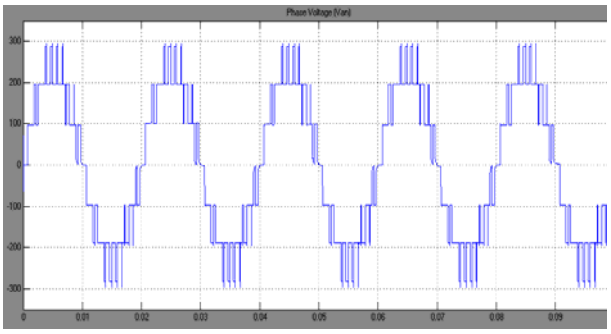

Figure 9 Seven Level output phase voltage waveform for RL Load (R = 12 Ohms, L= 3.82 mH, ma = 1.2, mf = 15)

VII. CONCLUSION

In this paper, a new MLI structure is proposed without making use of any transformer and capacitors. Hence, it reduces the size, cost and losses.

With reduced number of switches, losses can be reduced as well as considering bulk production of units, it turns into significant saving.

The modular design can help in increasing the number of output voltage levels as per requirement. Of course the switching device voltage and current ratings have to be taken into consideration for each incremental change in level. The limitation of this topology is that the switches are not equally stressed. Also, the topology requires equal voltage isolated DC source. Owing to comparative economic benefit this drawbacks can be looked over.

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