CONTROL SCHEME FOR ULTRA SPARSE MATRIX CONVERTER

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Abstract— Research on the matrix converter has focused on modulation schemes and digital generation of the PWM switching patterns. The derivation of alternative topologies showing identical functionality but a lower count of unipolar turn-off power semiconductors demands attention. A matrix converter that is of particular interest is the indirect matrix converter (IMC) since its two stage structure affords simpler switch commutation requirements and a simplified modulation strategy. This paper presents the closed loop control of an Ultra Sparse Matrix Converter (USMC) as it provides features like reduced switches and absence of DC link. Unlike the conventional topology the converter does not require bidirectional switches. The control scheme incorporates the features like safe commutation. The USMC and the control scheme is tested in MATLAB/Simulink. Superiority of USMC and the control scheme over conventional converter employing diode-bridge is demonstrated through simulation results for closed loop operations. Results display better performance in terms of low THD in output voltage and source current. Even with step change in reference voltage or sudden load change superior performance is observed with RL load.

Index Terms— Matrix converter, Topology of MC, USMC, Simulation results

I. INTRODUCTION

With the progress of the power semiconductor devices technology, research in direct AC/AC power frequency converter experienced a renewed interest to provide efficient way to convert electric power for motor drives, uninterruptible power-supply, variable frequency generators, and reactive energy control [1]. One of the solution to it is a Matrix Converter (MC). The matrix converter is nothing but a three-phase to three-phase forced commutated cycloconverter. It consists of nine bidirectional switches that connect each phase of input to output as shown in Fig. 1.
These 9 bidirectional bipolar switches are usually obtained using 18 unipolar turn-off power semiconductors (IGBTs) and 18 diodes.

The matrix converter topology was originally presented in 1976 but it was in 1980 that the basic configuration and control of three-phase matrix converter was introduced by Venturini[1-3]. The high switching frequency control algorithm presented in [1], also commonly known as scalar control, has a limitation that the magnitude of output voltage is restricted to half of the input voltage and also gives difficulty in the input power factor control. This can be avoided by an alternative control algorithm employing Space Vector Pulse Width Modulation (SVPWM) and controlling the conventional matrix converter by treating it as a black box comprising of fictitious controlled rectifier and an inverter [5]. This indirect

approach gives the output-input voltage ratio of 0.866. Though the principle of control is that of two-stage rectifier-inverter approach, it still employs the conventional matrix converter with 9 bidirectional switches each having 2 IGBTs and 2 anti-parallel diodes. It requires sensing of current direction and accurate control for the implementation of a safe multistep commutation strategy to avoid short circuit of input lines. Thus, the control scheme has to ensure the safe commutation which makes it difficult.

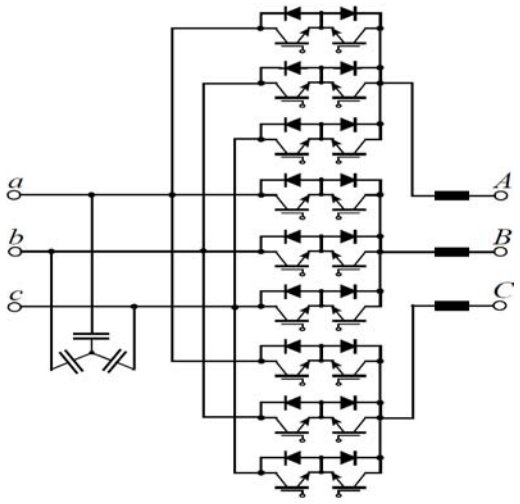


Fig. 1. Conventional Matrix Converter

Other approaches based on the concept of classical rectifier-inverter control methods are also available where two-stage AC-AC conversion is suggested. The first stage, which is a controlled rectifier employing self-controlled switches is directly connected (without a DC link capacitor) to a second stage, which is a conventional inverter. The matrix converter based on this principle are referred as Indirect Martix Converter (IMC). Various configurations of matrix converter have been proposed on this line and different control strategies have been suggested [2-6]. These works targeted improvement in the input-output voltage ratio, lower THD in input current, higher efficiency, reduction in switches, safe commutation etc.

Fig. 2 represents classification of matrix converter topologies. Unlike the conventional matrix converter, the IMC does not require bidirectional switches for the inverter as the conventional voltage source inverter inherently has the bidirectional power flow capability. This reduces the number of switches required for the AC-AC conversion. Table-I shows the comparison of various IMC in terms of the switches employed. The Sparse Matrix Converter (SMC) [2,7] requires lesser devices than Conventional IMC (CIMC). With a view to decrease the number of switches further Very Sparse MC (VSMC) [8] and Ultra Sparse MC (USMC) [10] came into existence.

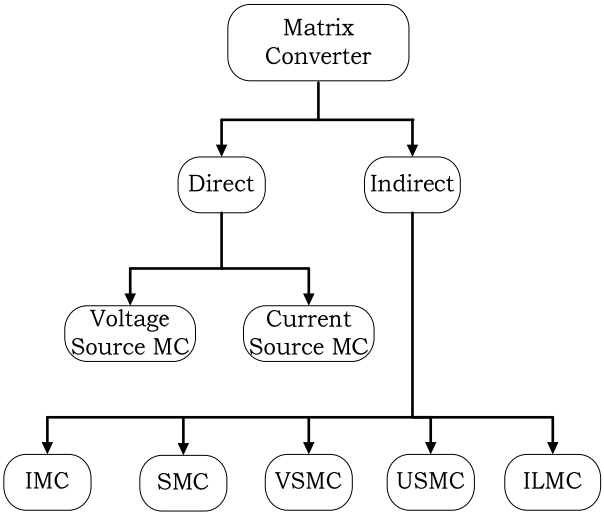


Fig. 2. Classification of AC-AC converter topology

Table I : Comparison of the devices used in various MCs

Converter Type	Transistors	Diodes	Isolated Driver Potentials
CMC	18	18	6
IMC	18	18	8
SMC	15	18	7
VSMC	12	30	10
USMC	9	18	7

This paper presents the analysis and simulation of a USMC matrix converter. Section II presents the USMC topology and the system configuration employed for the simulation study. The operating principle and the analysis on which the control scheme is designed is covered in detail in Section III. The effectiveness of the control scheme is demonstrated through the simulation results in Section IV.

II. BASIC MATRIX CONVERTER TOPOLOGY

Fig. 3 shows the USMC [10], which comprises of two stages: rectifier and an inverter connected directly without any DC link capacitor. It comprises of 6 switches (S1 through S3 and S1' through S3') for the inverter and 3 switches (Sa through Sc) for the rectifier. Thus, just 9 switches are required.

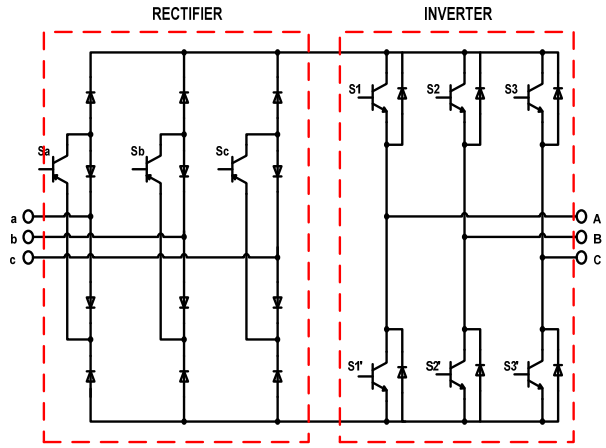


Fig. 3. Ultra sparse matrix converter (USMC)

The block diagram shown in Fig. 4 shows the system configuration which is designed to give the regulated AC output. The three-phase rectifier stage is controlled using SVPWM while the inverter is controlled using Sinusoidal Pulse Width Modulation (SPWM). The harmonic currents that result from high frequency switching are prevented from entering into the input line with the help of LC filter. Though RL load is used, any other AC load like induction motor can be powered through this USMC.

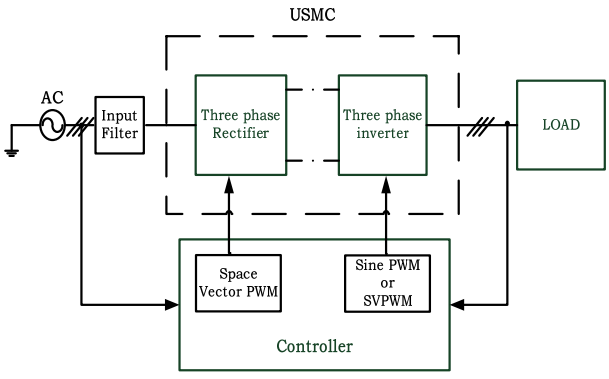


Fig. 4. Block diagram of closed loop USMC Topology

III. PRINCIPLE OF OPERATION

In a conventional matrix converter employing 9 bidirectional switches, a complex, multi-step commutation strategy is employed to prevent short-circuits of the input phases and open circuits of the output phases. However, with the USMC, a simpler zero dc link current commutation scheme can be used since the converter is separated into input and output stages. To commutate the input stage, the output inverter stage can be set into freewheeling mode, allowing the input stage to commutate under zero current. Consequently the input stage does not incur switching losses[4,5,9].

The analysis and the principle of the control of rectifier stage and inverter stage of the USMC are presented in this section. The SVPWM is employed for the both the rectifier and the inverter stage of the USMC. First the control and operation of rectifier stage is discussed which shows the selection of the appropriate switches are fired to the space vector of input voltage, appropriate switches at a particular function to obtain the DC output with minimum ripple. Next the control scheme employed for the inverter stage is presented.

The SVPWM strategy is designed for the rectifier to generate a constant voltage V_{pn}, which feeds the inverter stage. Three-phase input voltages expressed by (1) are sensed to obtain the space vector.

$$V_a = V_{in}\cos(\omega t)$$
$$V_b = V_{in}\cos(\omega t - 2\pi/3)$$
$$V_c = V_{in}\cos(\omega t - 4\pi/3) \quad (1)$$

The instantaneous location of the space vector is obtained to operate appropriate switches so that the ripple in the output voltage is minimum. Also, it is ensured that at all the times two input lines remain connected to the inverter through the two switches that are turned ON. Six different intervals are identified to trigger appropriate switches to achieve above objectives. This is explained next in length

Out of the switches Sa through Sc, the switches that are connected to the most positive potential and the most negative potential are turned ON. Thus, the rectifier is made to mimic the performance like a diode-bridge rectifier with a difference that the switches are triggered at higher frequency and not kept on continuously for 120° unlike diodes of diode bridge. Figure 4

shows these six switching intervals, each of 60° (marked I through VI), that are identified depending on the instantaneous values of the three phase input voltages. In interval I, phase a is at the highest potential throughout for the 60° period and for the first 30° phase b is at the lowest potential while from 30° to 60° phase c is at the lowest potential. Hence, for the entire interval 1, Sa is kept ON while the switch Sb is triggered for 0° to 30° and Sc is triggered from 30° to 60°. The duty cycle d_{ba} for the period 0° to 30° when input phase a is at the highest potential and input phase b is at the lowest potential is obtained using (2).

$$d_{ba} = \frac{-V_b}{V_a} = \frac{-\cos(\theta_b)}{\cos(\theta_a)} \quad (2)$$

where θa and θb are the phase angle of input voltage a and b respectively. The DC voltage V_{pn} during this portion is given (3)

$$V_{pn} = d_{ba} * V_{ab} \quad (3)$$

Similarly, during period 30° to 60° when phase a is at highest potential and c at the lowest, duty cycle for switch Sc and the DC voltage Vpn can be obtained by (4) and (5), respectively.

$$d_{ca} = \frac{-V_c}{V_a} = \frac{-\cos(\theta_c)}{\cos(\theta_a)} \quad (4)$$

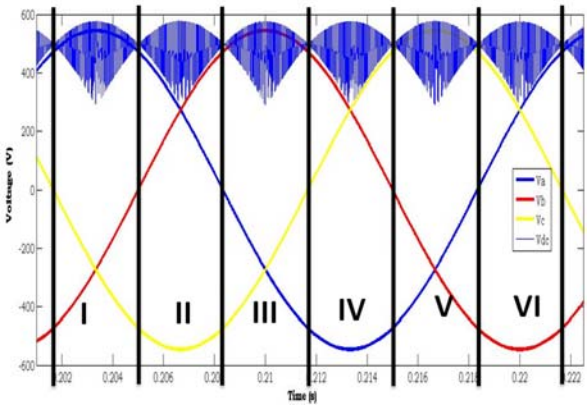


Fig. 5 Six intervals based on the input voltage and output voltage

$$V_{pn} = d_{ca} * V_{ac} \quad (5)$$

where θa and θc are the phase angle of input voltage a and c respectively.

Table II : Comparison of the devices used in various MCs

Intervals	Input angle	V_p	V_n	V_{dc}
I	0 – 60	v_a	v_b , v_c	v_{ab} , v_{ac}
II	60 – 120	v_a , v_b	v_c	v_{ac} , v_{bc}
III	120 – 180	v_b	v_a , v_c	v_{ba} , v_{bc}
IV	180 – 240	v_b , v_c	v_a	v_{ba} , v_{ca}
V	240 – 300	v_c	v_a , v_b	v_{ca} , v_{cb}
VI	300 – 360	v_a , v_c	v_b	v_{ab} , v_{cb}

The same principle is applied to other intervals as well. Table II gives the information about the various intervals and the input phases that gets connected to the inverter to provide a DC voltage V_{dc}.

The switches of the voltage source inverter circuit are controlled using SVPWM technique. Since the input lines of the VSI must never be shorted and a conducting path for the inductive load current must be provided, the switches of the VSI can only assume eight combinations, as shown in Figure 5. The combinations produce non-zero output voltages and are known as the non-zero switching states whereas the remaining two combinations are zero output voltages, and are known as the zero switching states, as shown in Figure 5.

The switching states (non-zero and zero switching states) of the VSI generate seven discrete values as shown in Fig. 6, and are known as voltage vectors V0 – V7. are zero magnitude voltage vectors placed at the origin of the α-β plane as shown in Fig. 6. The area enclosed by two adjacent vectors within the hexagon as shown in Figure 5, is known as a sector. The desirable output line voltages of the inverter can be represented by an equivalent space vector Vo rotating in a counter clockwise direction at a speed of θ angular frequency as shown in Fig. 6.

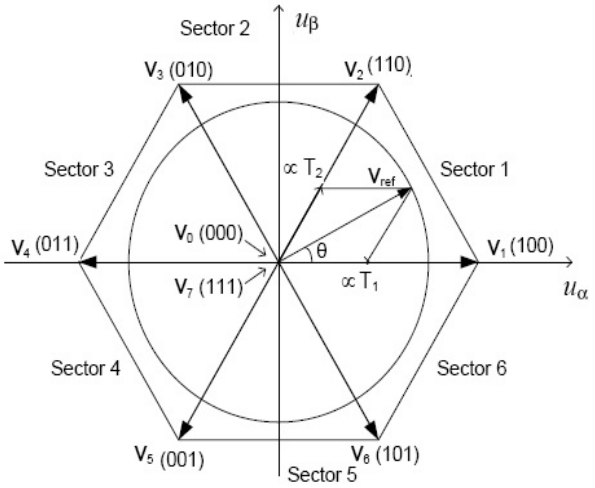


Fig. 6. The switching state vectors of SVM

The resulting space vector of the desired output phase voltages is given by (6)

$$V_{op} = V_{AB} + V_{BC}e^{j2\pi/3} + V_{CA}e^{-j2\pi/3} \quad (6)$$

Let's consider the VSI is a standalone converter with three-phase output voltage V_A, V_B and V_C supplied by a DC voltage source V_{pn}. It is assumed that the desired output voltages of the inverter are given as:

$$V_A = V_{op}\cos(\omega_o t)$$
$$V_B = V_{op}\cos(\omega_o t - 2\pi/3)$$
$$V_C = V_{op}\cos(\omega_o t - 4\pi/3) \quad (7)$$

Switching States			Phase Voltages			Line Voltages		
a	b	C	V_a	V_b	V_c	Vab	Vbc	Vca
0	0	0	0	0	0	0	0	0
1	0	0	2/3	-1/3	-1/3	1	0	-1
1	1	0	1/3	1/3	-2/3	0	1	-1
0	1	0	-1/3	2/3	-1/3	-1	1	0
0	1	1	-2/3	1/3	1/3	-1	0	1
0	0	1	-1/3	-1/3	2/3	0	-1	1
1	0	1	1/3	-2/3	1/3	1	-1	0
1	1	1	0	0	0	0	0	0

Table III : Switching states and corresponding phase and line voltages.

$$V_{AB} = \sqrt{3}V_{op}\cos(\omega_o t + \pi/6)$$
$$V_{BC} = \sqrt{3}V_{op}\cos(\omega_o t + \pi/6 - 2\pi/3)$$
$$V_{CA} = \sqrt{3}V_{op}\cos(\omega_o t + \pi/6 - 4\pi/3) \quad (8)$$

In complex form, the space vector of the desired output phase voltages is

$$V_p = \frac{3}{2}kV_o\angle\theta \quad (9)$$

where $0 < k \leq \sqrt{3}/2$ is the modulation index of the inverter stage.

The desired space vector output voltage Vo rotating at an angle θ approximated by the two non-zero active voltage vectors and the zero voltage vector is given by

$$V_o = d_\alpha * V_1 + d_\beta * V_2 + d_0 * V_0 \quad (10)$$

The corresponding duty cycles of the non-zero active state voltages and the zero state voltages are:

$$d_\alpha = \frac{2}{\sqrt{3}}k\sin(-\frac{\pi}{3} - \theta')$$
$$d_\beta = k\sin(\theta')$$
$$d_0 = 1 - d_\alpha - d_\beta \quad (11)$$

If the desired output space vector voltage is in sector I and the synchronization input phase angle is in interval I, the duty cycles are calculated as:

- During the first sub-interval,

$$d_1 = d_\alpha * d_{ba}$$
$$d_2 = d_\beta * d_{ba}$$
$$d_0 = 1 - d_1 - d_2 \quad (12)$$

- And during the second sub-interval;

$$d_1 = d_\alpha * d_{ca}$$
$$d_2 = d_\beta * d_{ca}$$
$$d_0 = 1 - d_1 - d_2 \quad (13)$$

The switching time corresponding to the calculated duty cycle is given as the product of the duty cycle and the switching period Ts . A time sequence of both rectifier side and inverter side switching is shown in Fig. 7.

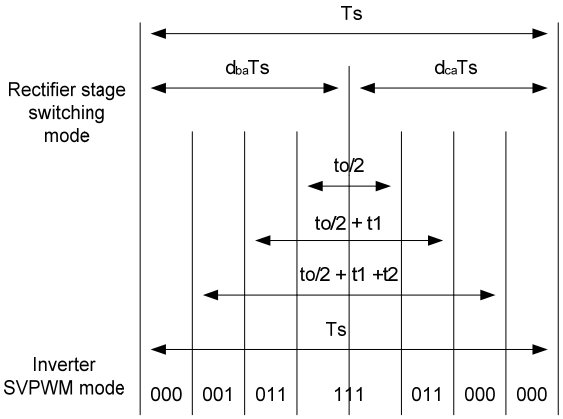


Fig.7 PWM sequence of the Ultra Sparse Matrix converter

All line side switches can be turned on or turned off at zero current and all load side switches can commutate similarly to a conventional DC/AC inverter. The line side switches commutate at both the beginning and end of each portion. If a zero vector is selected for the inverter on the load side at this time, then the line side switches can commutate at zero current

IV. SIMULATION RESULTS

This is divided into two main sections; a section that presents the closed loop simulation results of Ultra sparse matrix converter topologies with step change in reference voltage, while the other section presents the closed loop simulation results of the Ultra sparse matrix converter topologies with step change in load. Parameters considered for the simulation study are mentioned in Table IV .

Table IV : Circuits parameters for closed loop Implementation

Parameter	Symbol	Values
Supply voltage (Phase)	Vs (RMS)	230V
Frequency of Supply & switching	f & f_s	50Hz & 7.2kHz
Source filter inductances	L_{f1}, L_{f2},L_{f3}	6mH
Source filter capacitances	C_{f1}, C_{f2}, C_{f3}	210μF
Resistance of loads	R_{L1}, R_{L2}, R_{L3}	5Ω
Inductive reactance of loads	L_{L1}, L_{L2}, L_{L3}	5Ω

A. USMC with step change in reference voltage

The Ultra sparse matrix converter circuit shown in Fig. 8 is operated to give constant output frequency (50Hz) using the modulation strategy discussed earlier. The reference voltage is set to 170 V till t=0.2s and at t=0.2s the reference voltage is suddenly changed to 200V. The reference voltage is once again lowered to 170V at t=0.4s. Fig. 8 through 10 shows the response of the system under these conditions. It is observed that the RMS output voltage tracks the reference voltage and takes about 2 fundamental cycles to settle down. The input current (filtered current) and the output current are nearly sinusoidal as observed in Fig. 9 and as shown through the THD analysis in Fig. 10.

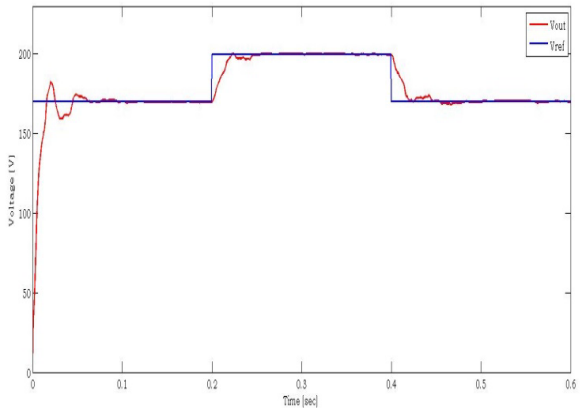
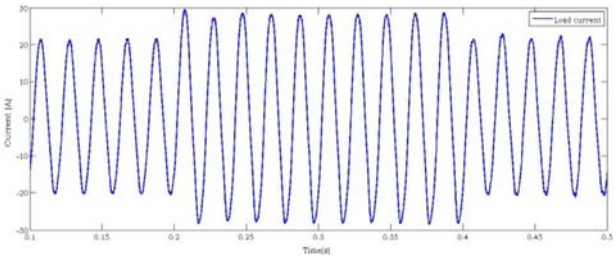
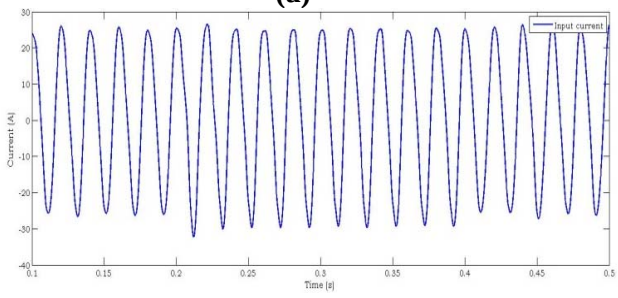


Fig. 8 Reference voltage and output voltage



(a)



(b)

Fig. 9 (a)output current and (b)input current

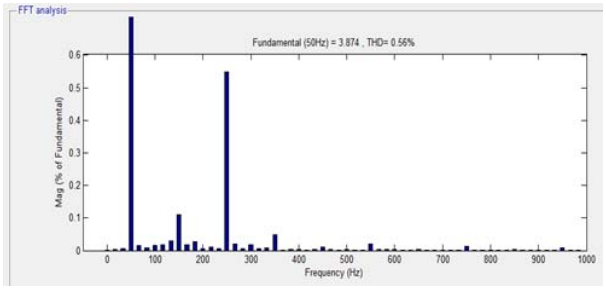


Fig. 10 THD analysis of input current

B. USMC with step change in load

The Ultra sparse matrix converter circuit shown in Fig.11 is operated to give constant output frequency (50Hz) using the modulation strategy discussed earlier. The reference voltage is constant, and load to half till t=0.15s and at t=0.15s the load is suddenly changed to full. The load is once again lowered to half at t=0.3s. Fig. 11 through 13 shows the response of the system under these conditions. It is observed that the RMS output voltage tracks the reference voltage and takes about 3 fundamental cycles to settle down. The input current (filtered current) and the output current are nearly sinusoidal as observed in Fig. 12 and as shown through the THD analysis in Fig. 13.

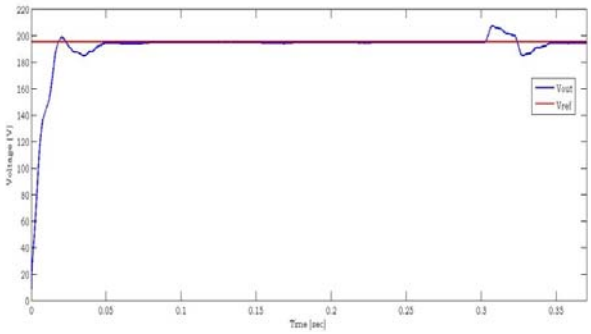
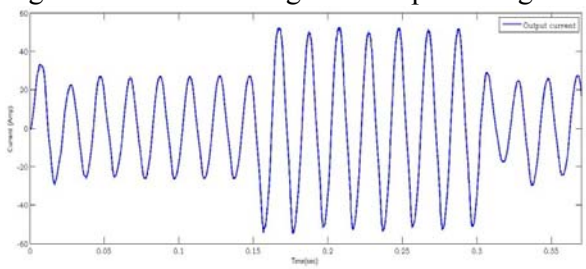
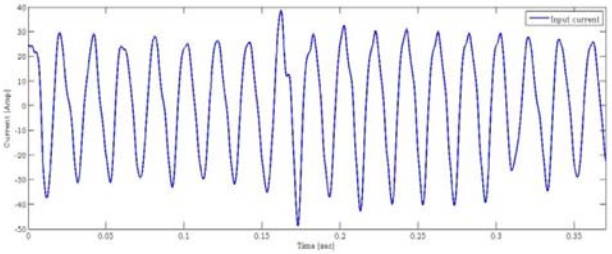


Fig. 11 Reference voltage and output voltage



(a)



(b)

Fig. 12 (a) output current and (b) input current

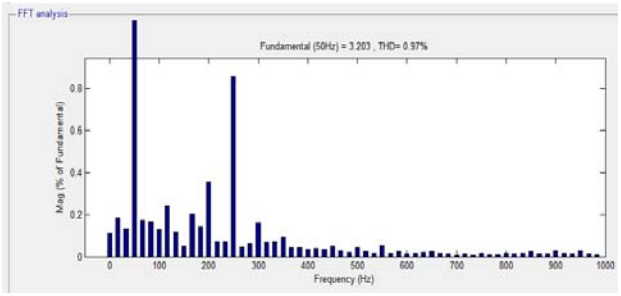


Fig. 13 THD analysis of input current

The performance of the USMC was evaluated with an RL load. The dc link voltage and input and output current are measured and results are shown in figure. It can be seen that the average value of the dc link voltage is approximately 560V, and that its shape is typical of the space vector modulation scheme used for the USMC. The THD of the input current was measured and results are shown in figure 10, 13. It can be seen that at full loads the THD is 1%.

V. CONCLUSION

The USMC is the most reduced form of the indirect matrix converter. It has minimal semiconductor requirements, comprising only 9 unidirectional switches and 18 diodes. Like the other converter in the indirect matrix family, the USMC uses simple commutation scheme to reduce the switching losses of the rectifier stage. The closed loop control scheme effectively tracks and regulates the AC output voltage at the desire valued. The USMC offers advantages like suppression of power harmonics and longer operating life due to the absence of electrolytic capacitor at dc link. The input (filtered) current THD is limited to less than 1%.

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