CONTROL OF ASYMMETRIC CASCADED H-BRIDGE MULTILEVEL INVERTER

[1]Atithi B.Patel, [2]Hiren H. Patel
[1]PG Student, [2]Professor
Electrical Engineering Department,
Sarvajanik College of Engineering and Technology, Surat , Gujarat, India
Email:[1]atithipatel1391@gmail.com, [2]hiren.patel@scet.ac.in

Abstract— This paper presents the performance of single phase seven and nine level Asymmetric cascaded H-bridge multilevel inverter. Unipolar Carrier based level shifted Pulse Width Modulation (PWM) technique is used for pulse generation. Unipolar carrier based modulation reduces the number of carriers required. The ACHBMLI when operated with the level shifted carrier based PWM shows more levels in the output voltage and hence gives lower total harmonic distortion. Simulation results obtained using MATLAB/Simulink are included to demonstrate the effectiveness of the closed loop control scheme used to provide a regulated AC output voltage.

Keywords—*Multilevel inverter, cascaded H-bridge inverter, R-L load, THD analysis, simulation results*

I. INTRODUCTION

In recent years, Multilevel Inverters (MLI) are becoming increasingly popular for high power applications due to lower dv/dt, stress on the switches, reduced EMI and increased power ratings. In addition, multilevel conversion reduces the output variables harmonic distortion and sometimes, in spite of the devices count increment, the conduction losses can also be decreased by increasing the number of level [1].The reduction of harmonic distortion is achieved by increasing the number of levels of output voltage. This will further reduce the switching losses by reducing the inverter carrier frequencies.

Various MLI have been proposed over the years. However, still the most popular MLI converter configurations include Neutral Point Clamped (NPC) MLI, Flying Capacitor MLI (FCMLI) and Cascaded H-Bridge MLI (CHBMLI). Out of these the CHB converter is mainly into the focus especially for the researchers working with the renewable sources like photovoltaic and fuel cell. The reason being they provide isolated sources required for CHB configurations. Further it offers modularity and can help increase the output voltage level by using the cascaded connection. [1]

Figure.1 shows a CHBMLI having H-bridges connected in cascade. Each H-bridge of a CHB is termed as H-cell. Usually the DC sources of the H-cells of a CHBMLI are identical to maintain the modular structure. For the H-cell with V_{dc1} as the source, the three different output voltage +Vdc1, 0, -Vdc1 can be obtained by appropriate switch combinations of the switches S_1 through S_4.

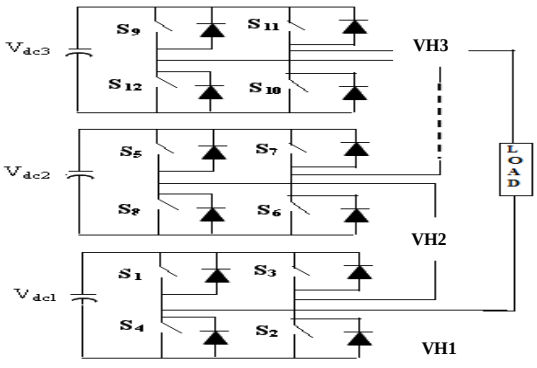

Figure.1 General Circuit for H-bridge Inverter [1]

The switches S_1 and S_2 turn on to obtain $+V_{dc1}$ while to get $-V_{dc1}$ the switches S_3 and S_4

must turn on. The output is 0 when the switches S1 and S4 or S3 and S2 turn on. Similarly other H-cells can give $+V_{dc2}$, 0, $-V_{dc2}$ and $+V_{dc3}$, 0, $-V_{dc3}$. The total output voltage of the CHBMLI is expressed by (1),

$$Vout = VH1+VH2+VH3 \quad (1)$$

Where VH1, VH2 and VH3 are the output voltage of three series connected H-cells. When $V_{dc1}= V_{dc2} =V_{dc3}$ the CHBMLI can give 7 levels in output voltage.

If the CHBMLI inverters have unidentical DC sources i.e. $V_{dc1} \neq V_{dc2} \neq V_{dc3}$ then such converters are called Asymmetric CHBMLI. Now a day, ACHBMLI has received increasing attention because it is possible to synthesize voltage waveforms with reduced harmonic content, even using few series-connected cells [2].

This paper presents the control scheme and simulation of seven and nine level ACHBMLI. Section II discusses the ACHBMLI used and the system configuration considered for the simulation. The control scheme used for controlling the ACHBMLI is discussed in Section III while Section IV shows the simulation results.

II. SYSTEM CONFIGURATION

Figure. 2 shows a seven level ACHBMLI employing two unidentical DC input sources with their magnitudes in the ratio 2:1. With unidentical DC sources of values V_{dc} and $2V_{dc}$, the ACHBMLI can synthesize seven output levels: $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, -Vdc, -2Vdc, $-3V_{dc}$. If the two unidentical DC input sources are selected with their magnitudes in the ratio 3:1, the ACHBMLI can synthesize nine levels in the output voltage. These levels are $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, V_{dc}, $2V_{dc}$, $-3V_{dc}$ and $-4V_{dc}$. [3]

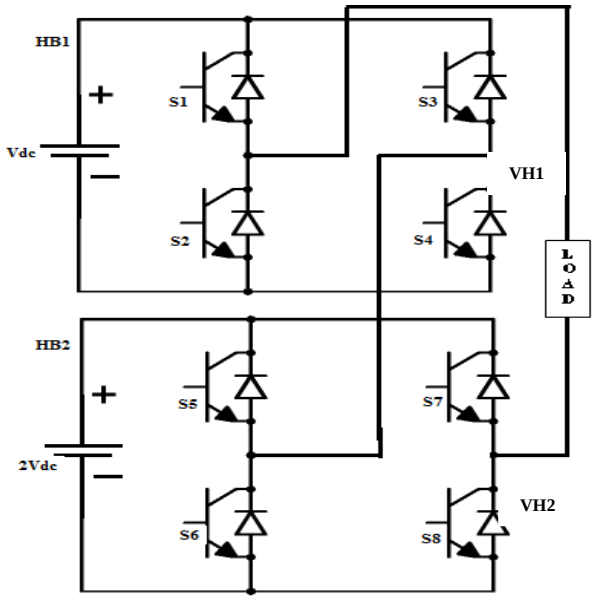

Figure.2 Diagram for 7-level Asymmetric CHBMLI [3]

Table I shows the various switch combinations to achieve 7-levels for the ACHBMLI shown in Fig. 2. It can be observed that certain levels ($+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$) can be obtained by more than one switch combinations. These redundant states can be appropriately selected to minimize the switching losses.[4]

Figure.3 shows the block diagram representing the system configuration employed to generate a regulated ac output voltage across the R-L load. The ACHBMLI is controlled using the level shifted carrier based PWM technique. The control scheme is presented at length in the next section.

Table I Switch Status to generate 7-level in output voltage

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$3V_{dc}$	1	0	0	1	1	0	0	1
$2V_{dc}$	1	0	1	0	1	0	0	1
$2V_{dc}$	0	1	0	1	1	0	0	1
V_{dc}	1	0	0	1	1	0	1	0
V_{dc}	1	0	0	1	0	1	0	1
V_{dc}	0	1	1	0	1	0	0	1
0	1	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1

0	0	1	0	1	1	0	1	0
$-V_{dc}$	1	0	0	1	0	1	1	0
$-V_{dc}$	0	1	1	0	0	1	0	1
-Vdc	0	1	1	0	1	0	1	0
$-2V_{dc}$	0	1	0	1	0	1	1	0
$-2V_{dc}$	1	0	1	0	0	1	1	0
$-3V_{dc}$	0	1	1	0	0	1	1	0

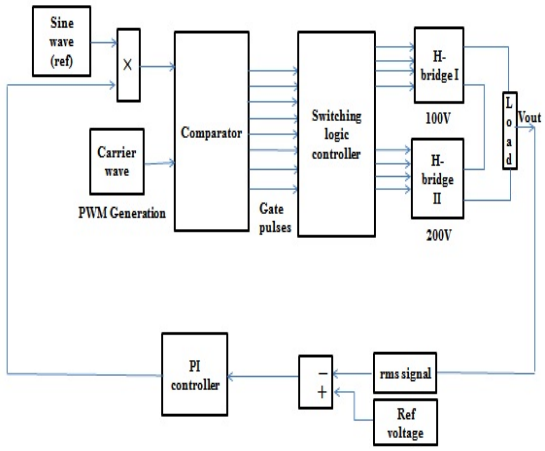

Figure.3 System configurations considered for simulation

III. CONTROL SCHEME

Pulse width Modulation refers to a method of carrying information on a train of pulses, the information is encoded in the width of each pulse. This technique helps in maintaining a constant voltage. [5] A modulation strategy for multilevel inverters is given in figure 4.

A popular approach to control the CHBMLI is to employ a carrier based PWM technique where the high frequency carriers signals are compared with reference wave (usually sinusoidal wave) of fundamental frequency. Carrier based modulation schemes are mainly divided into two categories: level-shifted (LSPWM) and phase-shifted (PSPWM) methods. Both of these have several variations, which differ by the allocation of module carriers with respect to each other. [6]

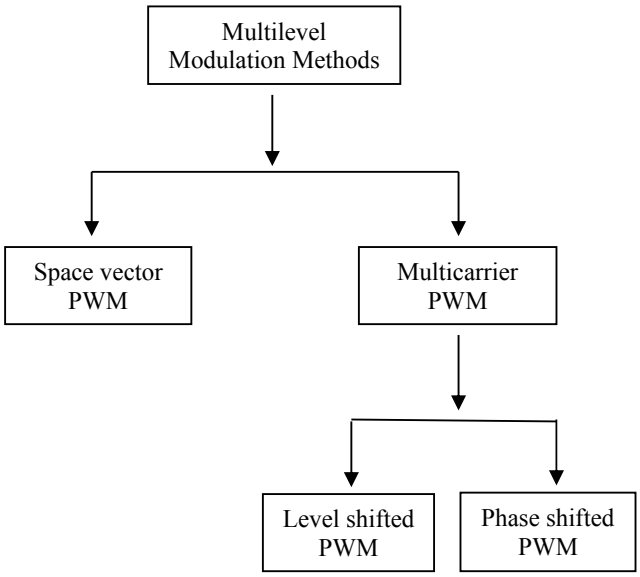

Figure.4 Modulation strategies for multilevel inverters [4]

In the carrier-based multilevel modulation, each level in a phase requires a carrier of its own. A *m*-level CHB inverter using level-shifted multicarrier modulation scheme requires (m – 1) triangular carriers, all having the same frequency and amplitude. The (m – 1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. [7].There are three kinds of level shifted modulation techniques, namely

- Phase Opposition Disposition
- Alternative Phase Opposition Disposition
- Phase Disposition

In the phase opposition disposition (POD) the carriers above the reference point, are out of phase with those below zero, by 180 degree. This is shown in Fig. 5. In the alternative phase opposition disposition (APOD), the carriers of adjacent bands are phase shifted by 180 degree while in the phase disposition (PD), all the carriers are in phase across all the bands. This gives rise to the lowest harmonic in the higher modulation indices as compared to the other disposition methods .Fig. 6 and fig. 7 shows the arrangement of the carrier waveforms with respect to the reference waveforms for APOD and PD techniques, respectively. [7]

In this paper, unipolar carrier-based N-level PWM operation is considered which consists of (N-1)/2 different carriers. Thus, unlike that

shown in Figs. 5-7, the reference is rectified sinusoidal waveform and hence, the number of carriers required is reduced to half. All the carriers have the same frequency f_0, the same peak-to-peak amplitude Ac, and are disposed to form a contiguous band. Alternate phase opposition disposition modulation scheme is used for gate pulse generation. The modulation index for PWM is defined as $M = A_m/KA_c$ where K is the number of the carriers. The modulation frequency ratio is given as $m_f = f_c/f_o$, where f_o is fundamental frequency. [8]

The polarity of the sine wave (that is rectified and used as unipolar reference for PWM), is detected. If it is positive then the comparator and logic circuit generates the positive levels and negative levels if the polarity of sine wave is negative. The value of the exact output voltage level is dependent on the ratio of the instantaneous value of the reference wave and KA_c, The output voltage is regulated by adjusting the value of M which is done based on the output of the PI (proportional plus integral) controller. The PI controller process the error in the desired output voltage and actual output voltage. [9, 10]

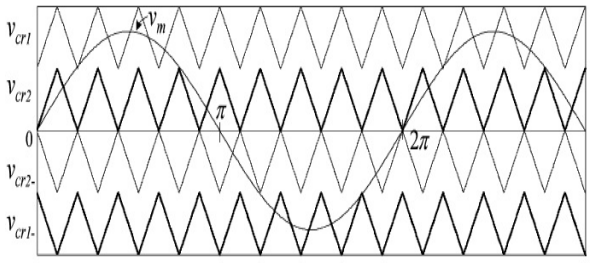

Figure.5 Carrier arrangement for POD [7]

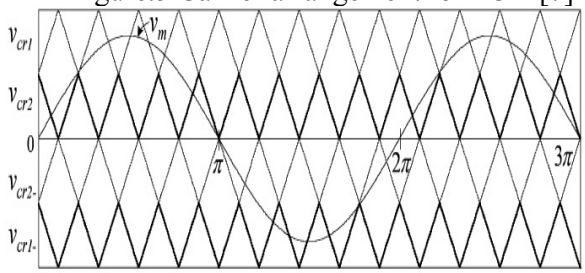

Figure.6 Carrier arrangement for APOD [7]

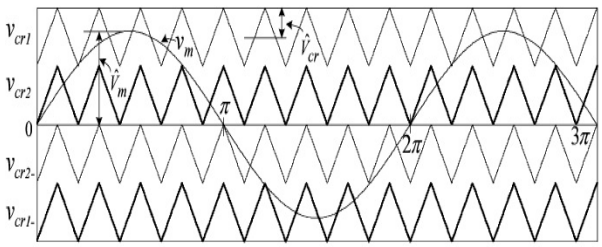

Figure.7 Carrier arrangement for PD [7]

IV. SIMULATION RESULTS

In this section, the system configuration of Fig. 3 is simulated using MATLAB/Simulink. The parameters used for the simulation are shown in Table II. The results are shown for two cases: (i) With V_{dc1} = 200V and V_{dc2} = 100V and (ii) With V_{dc1} = 300V and V_{dc2} = 100V.

Table II Parameters used for simulation

Parameter	Value
Modulation index	1
Fundamental frequency	50Hz
Carrier frequency	5KHz
Resistance	100Ω
Inductance	318.6mH
DC bus voltage	
For 7-level CHBMLI	H1=100V H2=200V
For 9-level CHBMLI	H1=100V H2=300V

Figs. 8 through 10 shows the performance of ACHBMLI with V_{dc1} = 200V and V_{dc2} = 100V. The reference output voltage (rms) is set to 200V and the actual output voltage tracks this reference voltage. The output voltage takes about 3-4 fundamental cycles to settle to a steady state value of 200V. Fig. 9 shows that switches of H-cell with DC voltage source of lower value are switched at frequencies higher than the switches of another cell. Thus, the switches of that cell has higher switching losses but lower dv/dt and also that H-cell has to handle less power. Fig. 9 also shows that the output voltage exhibits 7 levels. The steps in the output voltage waveform are uniform with a voltage difference of 100V between successive levels. The multi-stepped PWM output voltage results into a sinusoidal output current. The FFT analysis for the output voltage and current are displayed in Fig. 10. It shows that the current THD is about 1.82% and individual harmonics are also less than 0.8% and thus, comply to the standards.

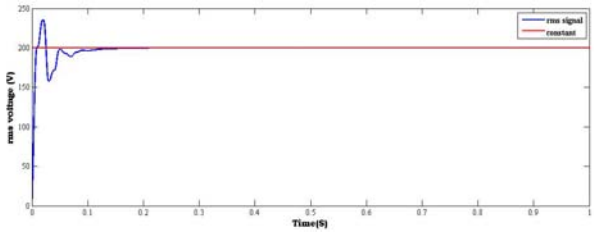

Figure.8 Output voltage and reference signal

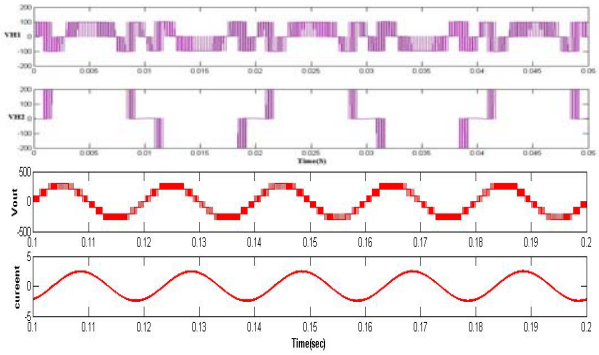

Figure.10 Output waveform of 7-level VH1, VH2, Vout and output current

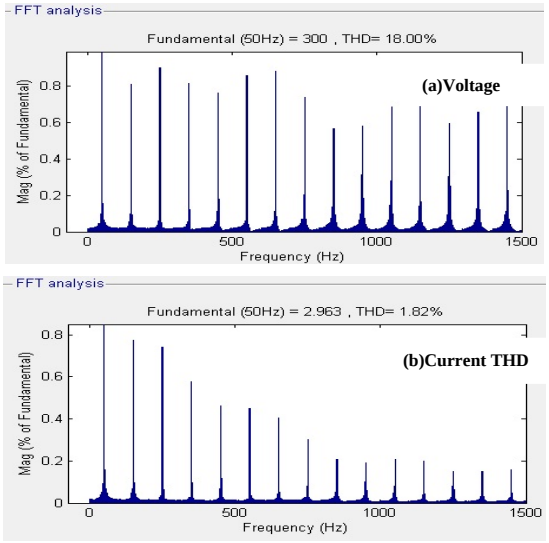

Figure.10 THD analysis of 7-level Asymmetric CHBMLI (a) Voltage and (b) Current

Figs. 11 through 13 shows the performance of ACHBMLI with V_{dc1} = 300V and V_{dc2} = 100V. The reference output voltage (rms) is set to 230V and the actual output voltage tracks this reference voltage. Fig. 11 shows that, like the earlier case here also the output of both H-cells exhibits 3 levels in the output voltage of each H-cell. However, 9 levels are obtained in the resultant output voltage of the ACHBMLI. Just like the previous case, the steps in the output voltage waveform are uniform with a voltage difference of 100V between successive levels. The FFT analysis for the output voltage and current are displayed in Fig. 13. It shows that the current THD is about 1.5% and voltage THD is 13.45% against the current THD of 1.82% and voltage THD 18.00% obtained with 7-level output voltage. Table III summarizes the performance with 7-level and 9-level output.

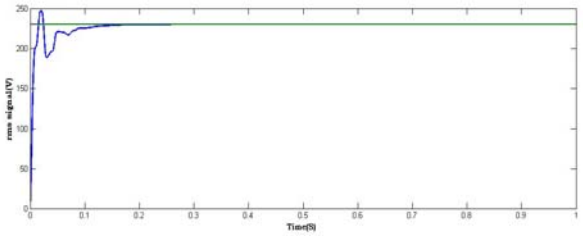

Figure.11 Waveform of reference voltage and rms voltage at ref voltage =230V

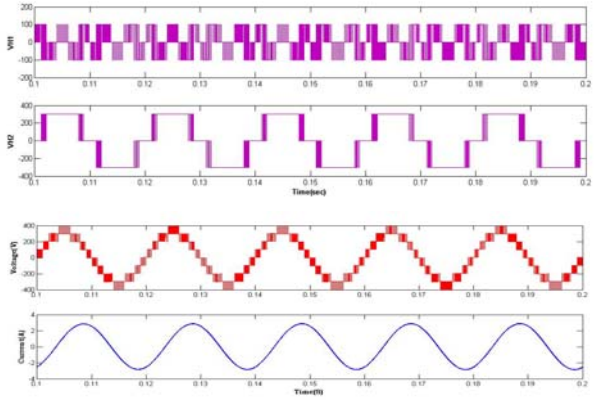

Figure.12 output waveform of 9-level VH1, VH2, Vout and current

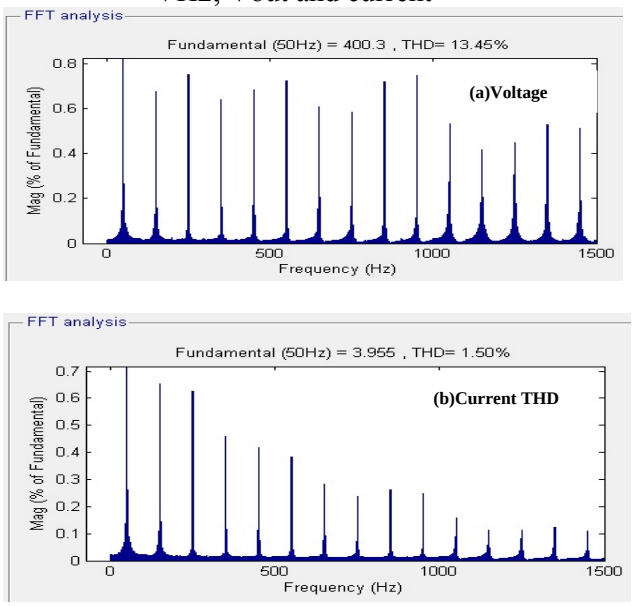

Figure.13 THD analysis of 9-level Asymmetric CHBMLI

(a) Voltage and (b) Current

Table III THD Comparison

ACHBMLI	%Voltage THD	%Current THD
7-level	18.00	1.83
9-level	13.14	1.55

V. CONCLUSION

Compared to symmetric CHBMLI, ACHBMLI generate high number of output voltage levels with less number of switches. This result into lesser losses, lesser harmonic content and better output at a lower cost However, the modularity is lost. The 9-level ACHBMLI generate better output with voltage THD of 13.14% and current THD of 1.55%. With increase in modulation index or reference voltage, THD decreases as the number of level increases in the output voltage waveform. With low modulation index the 9-level ACHBMLI result into number of levels less than 9 in the output voltage.

REFERENCES

[1] K.N.V. Prasad, G. Ranjith kumar, T.Vamsee kiran, G. Satya narayana, "Comparison of Different Topologies of Cascaded H-Bridge Multilevel Inverter" International Conference on Computer Communication and Informatics (ICCCI - 2013), Jan. 04 – 06, 2013, Coimbatore, INDIA.

[2] F. Khoucha, A. Ales, A. Khoudiri, K. Marouani, M.E.H. Benbouzid, A. Kheloui, "A 7-Level Single DC Source Cascaded H-Bridge Multilevel Inverters Control Using Hybrid Modulation" International Conference on Electrical Machines - ICEM 2010, Rome

[3] Piragateesh J, Mohanasundaram K, Anbumani D, Prabhakaran K K, "A Comparison of PWM Control and Digital Control Strategy for Asymmetrie DC-AC Caseaded H-bridge Multilevel Inverter with Rand Motor Load" International Conference on Circuits, Power and Computing Technologies,2013.

[4] Kiruthika, j.Gayathri Monika, v. Jamuna, "Multicarrier Based Asymmetric Multilevel Inverter", International Journal of Engineering science and Technology, ISSN: 2278-9510, Vol. 5 No. 04S April 2013.

[5] P.T.Josh, Jovitha Jerome, Arul Wilson, The Comparative Analysis of MultiCarrier Control Techniques For SPWM Controlled Cascaded H-Bridge Multilevel Inverter" 978-1-4244-7926-9/11 ©2011 IEEE.

[6] Jannu Ramu, S.J.V. Prakash, K. Satya Srinivasu, R.N.D. Pattabhi Ram, M. Vishnu Prasad2 and Md. Mazhar Husain, "Comparison between Symmetrical and Asymmetrical Single Phase Seven Level Cascade H-Bridge Multilevel Inverter with PWM Topology", International journal of multidisciplinary sciences and engineering, Vol. 3, No. 4, April 2012.

[7] High-Power Converters and ac Drives, By Bin Wu © 2006,The Institute of Electrical and Electronics Engineers, Inc.

[8] Satheesh Kumar, Dr. S.P.Natarajan, Dr. Alamelu Nachiappan, and Dr. B. Shanti ,"Performance Comparison in Hybrid H-Bridge Multilevel inverter for Various PWM Strategies" ,ISSN 2351-8014 Vol. 8 No. 2 Sep. 2014

[9] R.Kavitha,Dr.RaniThottungal,S. Agalya, "Implementation of Seven Level cascaded Multilevel Inverter in Closed Loop For Different Modulation Index", ISSN Certified Journal, Volume 4, Issue 3, March 2014.

[10] N. Sujitha, S.Satish Kumar, M.Sasikumar "Simulation Analysis of Hybrid Alternative Phase Apposition Disposition PWM Scheme for Cascaded Multilevel Inverters "International Journal of Scientific & Engineering Research, Volume 3, Issue 10, October-2012.