FPGA IMPLEMENTATION OF IMAGE FUSION USING DWT FOR REMOTE SENSING APPLICATION

[1]Gore Tai M, [2]Prof. S I Nipanikar
[1]PG Student, [2]Assistant Professor,
Department of E&TC, PVPIT, Pune, India
Email: [1]goretai02@gmail.com [2]sanjaynipanikar@rediffmail.com

Abstract— Earth observation satellites provide different portion of multisensory data at different resolutions. The fusion of multisensory image data has become a useful tool in remote sensing application. The DWT based image fusion approach has many fusion rules such as maximum, minimum, average. In this paper, we propose the best image fusion approach base on DWT with maximum fusion rule and hardware implementation for DWT maximum fusion rule using Xilinx System Generator (XSG) is demonstrated on FPGA. FPGA board used here is Spartan6 sp601.

Index Terms— Image fusion, DWT, Simulink, Xilinx System Generator (XSG), Hardware Co-Simulation

I. INTRODUCTION

Recently, the image fusion has great importance in digital image processing. Image fusion is a data fusion technology which keeps images as main research contents. The main goal of image fusion is to integrate complementary multisensory, multi-temporal and multi-view information into one new image which is more informative than any of the input images. The multisensory data in the field of remote sensing, medical imaging may have multiple images of the same scene providing different information. In a single image not contains all the information of objects in the image. Image fusion is used to achieve more information contents. Image fusion is the process of combining complementary information from multiple images into a single image which includes more information than any of the input images. Image fusion has widely used in remotely sensed image analysis at pixel, feature, and decision level. Images used for fusion can be taken form multimodal imaging sensors or from the same imaging sensor at different times [1].

The infrared & visible image is part of multisource data fusion for acquiring complementary information toward the formation of high performance perception system. Those images are captured by IR & Visible sensor provide different & complementary information through the fusion of these images are required to get maximum information than original one with the characteristics of information rich and easy to identify.

Image fusion is mainly divided into different levels. In this paper only used the pixel-level fusion. Pixel level image fusion method has various methods such as weighted average, Principal Component Analysis (PCA), Discrete Cosine Transform (DCT), Discrete Wavelet Transform (DWT) and Stationary Wavelet Transform (SWT). The DWT `method has important in an image fusion method for its excellent feature & time frequency analysis. Wavelet transform fusion is defined as considering the wavelet transforms of two registered input images together with the fusion rule. The fused image is reconstructed by taking inverse wavelet transform.

In this paper, we have to implementing algorithms in MATLAB using Xilinx System Generator (XSG) for DWT fusion rule. Then generator token is used to generate HDL code. Hardware implementation of DWT algorithm is demonstrated on FPGA.

II. PROPOSED DWT BASED IMAGE FUSION

The requirement step of image fusion is that images have to be correctly aligned on a pixel-by-pixel basis. We used already perfectly registered images for experiment. The basic block diagram of image fusion using wavelet transform as shows fig.1

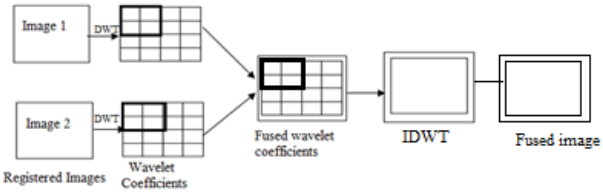

Fig.1 Block diagram of DWT based image fusion [11]

Step1: The source images infrared & visible that are taken as inputs.

Step2: wavelet transform, the source images are decomposed into low and high frequency bands to get one Approximation (A) and three detail component such as (Vertical. Horizontal and Diagonal) as shows

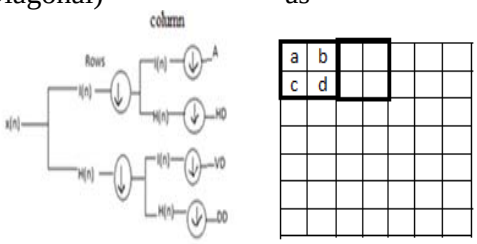

Fig.2 decomposition using DWT

Step3: Apply wavelet transform on input images to obtain the wavelet coefficients (A, H, V, D) Calculate Wavelet coefficients are as follows:

DWT coefficients for Haar wavelet transform-

$$L = \begin{bmatrix} \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} \end{bmatrix} \qquad H = \begin{bmatrix} \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{2}} \end{bmatrix}$$

Calculate approximation and Detail coefficients are as follows-

$$A = \left(\begin{bmatrix} a & b \\ c & d \end{bmatrix} xL \right) xL'$$

$$A = \left(\frac{a+b+c+d}{2} \right)$$

Detail coefficients:-

$$H = \left(\frac{(a+b)-(c+d)}{2} \right)$$

$$V = \left(\frac{(a+c)-(b+d)}{2} \right)$$

$$D = \left(\frac{(a+d)-(c+d)}{2} \right)$$

Step4: The wavelet coefficients are fused by taking maximum pixel values of input images.

Step5: The fused image is obtained by taking the inverse wavelet transform

The least important thing is these methods have advantages such as it is more robust under transmission and decoding errors, better fusion results, high accuracy, consume less area than other image fusion methods [10].

III. HARDWARE IMPLEMENTATION

Field Programmable Gate Array (FPGA) is a reconfigurable IC. Spartan6 SP601 is chosen for hardware implementation because of it has advantages like reconfigurability, contains 128mb of DDR2 component memory, low power, small size, & high speed of operations. The implementation process of image fusion algorithms on hardware has the most viable solution for improving the performance of the systems. A Field Programmable Gate Array (FPGA) is one such reconfigurable hardware, offering superior features than DSP & other hardware device due to their product reliability & maintainability advantages in digital image processing. The multiple processing data sets require in many algorithms have to be performed sequentially on a computer and fused one pass in FPGA.

The general flow diagram of DWT based image fusion algorithm as shown in fig.3

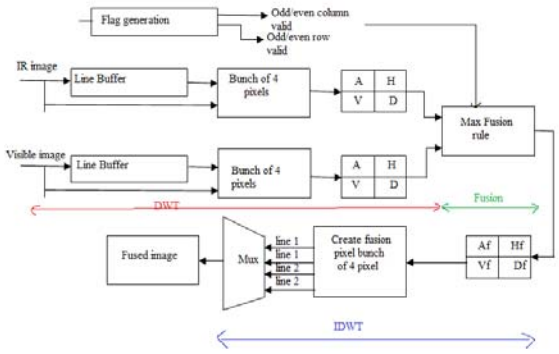

Fig.3 Block diagram of DWT based image fusion

It is very difficult to write a code for FPGA design [9]. To create an FPGA design, using Hardware Description Language (HDL) such as VHDL or Verilog. Xilinx System Generator is a MATLAB-simulink based design tool which offers high performance & require very less learning and development time. XSG for FPGA is a tool which offers block libraries that plugs into Simulink model tool is integrated with MATLAB window. Simulink has become an important part of engineering programs and industries. To start with Simulink in matlab, double-click on Simulink icon. The Simulink window opens. Then with the help of Simulink Library Browser, we can access the different toolboxes available for processing. The Video and Image processing block set contains a number of elements such as sources, sinks, math operators, parameters etc. The Xilinx Block set contains various elements shown below such as Basic Elements, Math, Shared Memory, Control logic, tools etc. Fig.4 shows the complete Simulink design model of FPGA implementation of image fusion using DWT algorithm.

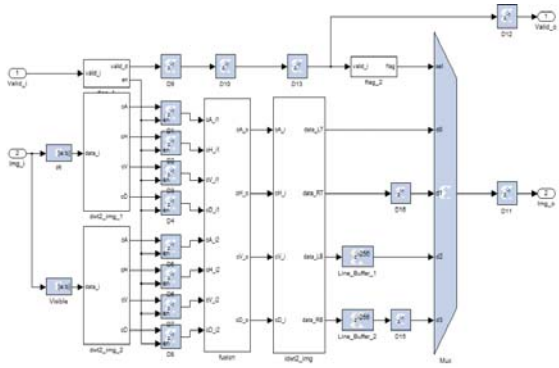

Fig.4 Simulink modeling of image fusion using DWT algorithm

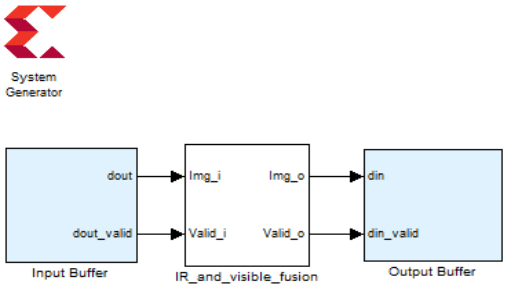

Fig.5 System generator model for DWT

Fig.5 shows the system generator model of DWT algorithm. In that, input buffer block stores the image and sends in parallel. IR and Visible fusion block receives information pixel wise from input buffer and process them and store into the BRAM. Dual port RAM reads pixel one by one and display them through output connector. After obtaining the results, system generator is configured with Spartan6 FPGA board. After that programming file in VHDL has been created and can be accessed using Xilinx ISE. After the simulation system generator model hardware co-simulation block is generated. Hardware co-simulation block is used to perform hardware co-simulation using JTAG.

To synthesis these modules first creates net list files which serve as the input to the implementation module. After generating these files, the logic design is converted into a .bit file that can be downloaded on the FPGA.

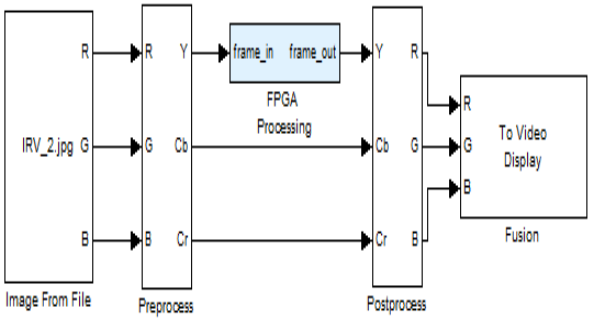

Fig.6 Test bench model of DWT based image fusion on FPGA

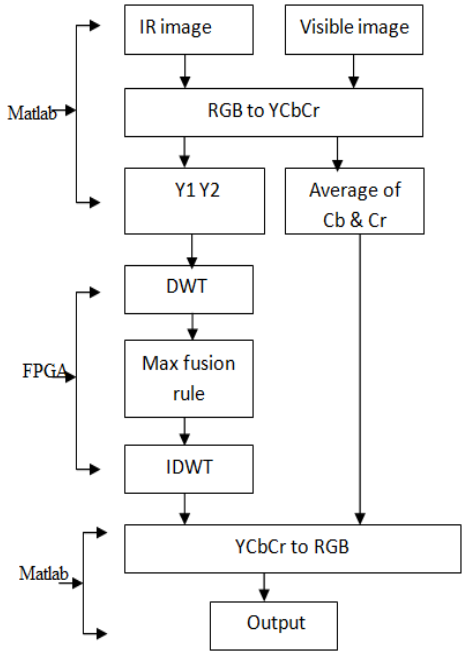

Fig.7 Project flow chart for FPGA implementation of image fusion

Step 1: Read color infrared image from image file and convert it into gray scale is pre-processed by MATLAB and converted into matrix format.
Step 2: Read color visible image from file & convert it into gray scale is pre-processed by MATLAB and converted into matrix format.
Step 3: Add Y1, Y2 component and take average of Cb, Cr for processing
Step 4: A simulink model for the proposed DWT maximum fusion rule is developed in MATLAB.
Step 5: Insertion of system generator token in Simulink Model.
Step 6: Compile HDL coding by using Xilinx System Generator to create .bit file and download into FPGA.
Step 7: Output of FPGA is stored in SRAM and post processed by Matlab. (Output image size 128x128)
Step 8: The output of SRAM feed to MATLAB to analyze output fused image.

IV. RESULT AND DISCUSSION

The hardware co-simulation results for proposed DWT based image fusion are shown fig.8. Image frames are used for hardware processing of size 128x128.

Table I. Device Utilization Summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	341	18224	1%
Number of Slice LUTs	213	9112	2%
Number of fully used LUT-FF pairs	127	427	29%
Number of bonded IOBs	95	232	40%
Number of BUFG/BUFGCTRLs	1	16	6%

Operating frequency is 151.099MHz, to calculate frame rate for maximum frequency

$$\text{Frame Rate} = \frac{F\max}{(128x128)}$$

$$= \frac{151MHz}{(128x128)}$$

$$= 9218 \text{ FRAME/SEC}$$

Minimum period= 6.621ns

Minimum input arrival time before clock= 3.87ns

Maximum output required time after clock= 5.158ns

Maximum combinational path delay= 4.965ns

According to above values, DWT maximum fusion rule has become one of the most promising methods for analysis of images in remote sensing. To process image fusion algorithm on FPGA at frame rate 9218 frame/sec and required time period of 6.61ns.

After the simulation and synthesis .bit file is generated then download on FPGA hardware through USB cable. The fused images are then observed in MATLAB with the help of JTAG port through USB cable. Fig.8 shows the fused images displayed in MATLAB.

(a) (b)

(c)

Fig.8 Experimental images (a) visible image (b) infrared image (c) fused image

V. CONCLUSION

Here, the hardware implementation of image fusion approach using DWT with maximum fusion rule is demonstrated on Spatan6 SP601 FPGA platform. The DWT maximum fusion rule provides maximum information at high speed.

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