PERFORMANCE AND COMPRESSION OF A NOVEL DESIGN WITH HYBRID LOGIC STYLE FOR ULTRA-LOW POWER

Atul kumar Pathak[1], Mukesh Kumar Silwat[2], Umesh Singh Sikarwar[3]
[1]Research Scholar, Electronics and Comm. Dept, NITM Gwalior India
[2]Research Scholar, Electronics and Comm. Dept, RJIT Tekanpur Gwalior India
[3]Assistant Professor, Electronics and Comm. Dept, SRIIT Gwalior India
Email: atulya_pathak@yahoo.co.in[1], mukesh.kumar971364@gmail.com[2],
umesh18sep@gmail.com[3]

Abstract
Full adder is the basic digital components for the region many improvements have been made to improve its architecture. In this paper, we present new adder logic style without losing the characteristic of the basic circuits with 8 transistors. The main design objectives for these adder cell modules are providing Low-Power dissipation, high speed with full-voltage swing without using extra elementary growth on design. In this design, we employed with 8 transistors. The utilizes dynamic change in the width Length ratio in order to get specified results new full adders with new methodology. This design is based on a different new approach which eliminates the need of XOR/XNOR gates for designing full adder cell; it provides high speed and Ultra Low-Power, as well as a full voltage swing without any extra component required. Many of the previously reported adders in literature suffered from the problems of extra elements required to full-fill the circuit recruitment like voltage-swing and speed when operated at low supply voltages. This new designs successfully operate at ultra low voltages. The studied circuits are optimized at 45nm and 90 nm PTM (Tanner). The comparison between these two novel circuits in terms of Power, Delay
Keywords: Propagation delay, Power consumption, Power-Delay-Product, 8T Novel Adder design, Hybrid design style.

1. Introduction

Addition is a very basic operation in arithmetic. Most of the operations based on addition. With these operations we need to minimize the power consumption and increasing speed of the system without further growth on the chip area, the low power requirement of VLSI system design have challenged the area of research towards technology, architectural design and methodology solution to allow reduce energy dissipation on CMOS Circuits. Since the full adder cell is performing regularity in the CMOS functional units, improving the performance of the 1-bit full adder is a major goal and has attracted much attention. A variety of full adders using different architectural designs and technologies have been reported in literature [1] and they commonly aim to tradeoff between energy consumption and propagation delay. Adder performance affects the arithmetic system and functional units such as multiplier ALU etc. An optimized design is required to prevent any reduction in the output signal, consume less power, have less delay in critical path and be reliable even at low supply voltage as we scale towards nano-meter, layout regularity, and interconnect complexity are also primary concern. By scaling down the feature size of devices in nanometer, the supply voltage should be scaled down to avoid effects of hot carrier in CMOS circuitry. As a result, transistor size and static power playing main role in nano-scale circuits for efficient power control [2].

II Literature Review
Hybrid full adder

In this section shows an ultra Low-Power Hybrid full adder circuit with XOR-XNOR topology. SEMI-XOR gate generate the first four states and last four states generated by SEMI-XNOR gate of the SUM output. As depicted in Table 1, in order to design the SUM circuit, these SEMI XOR-XNOR gates employed with C_{in} input used as an enable signal. When C_{in} is equal to zero, the SEMI-XOR gate is similar to the SUM, and when C_{in} is equal to one, the SEMI-XNOR gate is the output of the SUM circuit. According to Fig. 1 the circuits of these gates and the table 1 shows the Truth-Table of these two gates When we connect the SEMI-XNOR gate output to the single NMOS transistor, where the source/ drain of this transistor is connected to SUM output and its drain/ source is connected to the C_{in} the high impedance states in the output will we set to the correct value. As shown in Fig. 2, in order to provide full-swing voltage at SUM and C_{out}, we take in the structure of this hybrid full adder cell. As it is apparent, this novel hybrid adder cell minimizes the static power consumption by improving W/L ratio and eliminating any possible direct path between V_{dd} and the ground due to the use of NMOSs and PMOSs in a complementary manner.
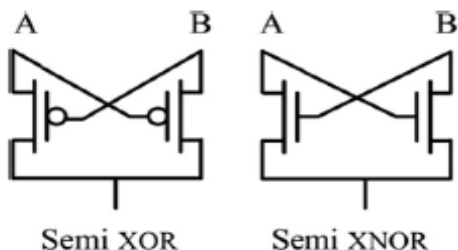

Fig. 1 Semi XOR and Semi XNOR Gate

By utilizing this technique, when one part of the circuit is on other one is in the off situation, so there is no short-circuit current.

A	B	SEMI XOR	SEMI XNOR
0	0	0	HZ
0	1	1	0
1	0	1	0
1	1	HZ	1

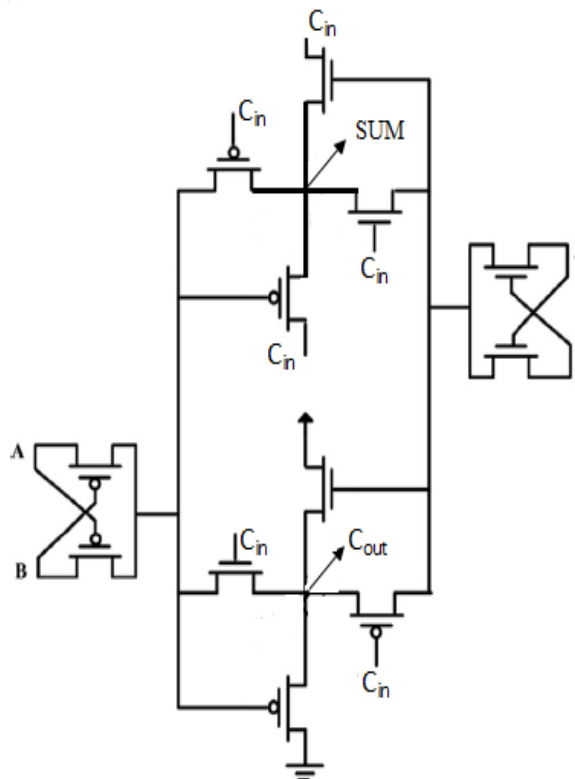Table: 1 Truth Table of SEMI XOR and SEMI XNOR Gate

Fig. 2 hybrids Full Adder

This design uses 12 transistors with dynamic W/L of transistor. We are eliminating UPLD circuit from the design and utilize the basic property of the CMOS transistor in this proposed methodology has low energy dissipation and speed without extra circuitry use.

III Proposed Design

In this work, existing 8T full adder is modified to address their discharging problem with changing through dynamic width Length ratio output for the all combinations of the inputs. Before having a detailed understanding of working principle of proposed 8T full adder we need to be aware of the design and its working principle of the existing PRPOSE-8T full adder which is as shown in the Figure.3 and it is explained as follows. This full adder is designed using combination of transistors to get appropriate result. First block generate the out of input A and B as output of   XOR between them and further XOR with C_{in} so we get output Sum but discharging are not in suitable value so next cycle of result not in get proper voltage level here we introduce third extra transistor to improve this discharging problem.

Performance of the 1-bit full adder cell is a significant goal. Thus in this work 8 transistors

full adder is proposed which addresses the discharging problem at the output for the particular combinations of the inputs in the existing full adder design. The proposed 8T full adder is implemented using the 90nm and 45nm technology library and is simulated & verified. It observed from the simulation results that the proposed 8T full adder outperforms the other existing full adders in terms of power consumption, delay PDP (power delay product) and transistor count.
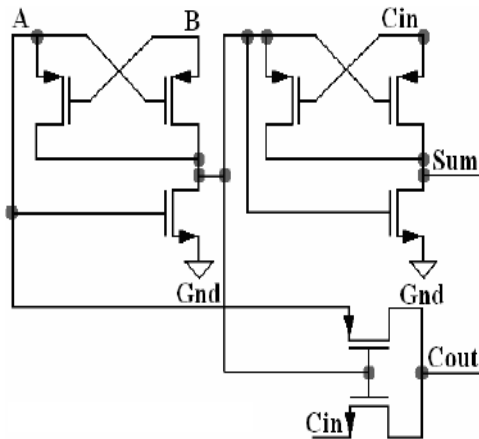

Fig. 3 PROSOSE-8T Full Adder

IV Simulation results and analysis

In this section, the proposed full adder cells shown in Fig. 8 is evaluated and compared to the ones chosen from the literature is shown in fig. 5 both the circuits are implemented using Tanner EDA and extracted using 90nm and 45 nm PTM CMOS technology.
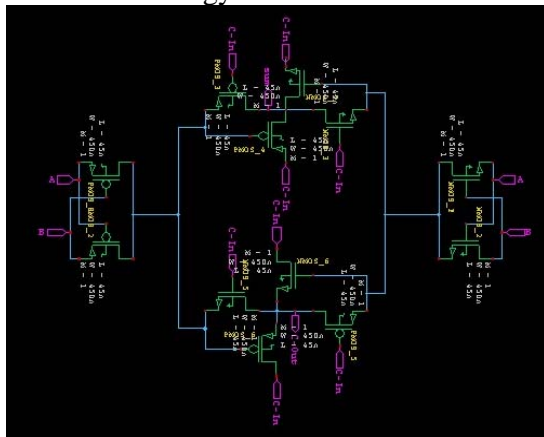

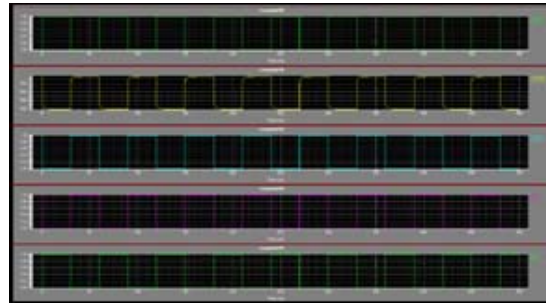Fig. 5 Schematic Design of hybrid Full Adder

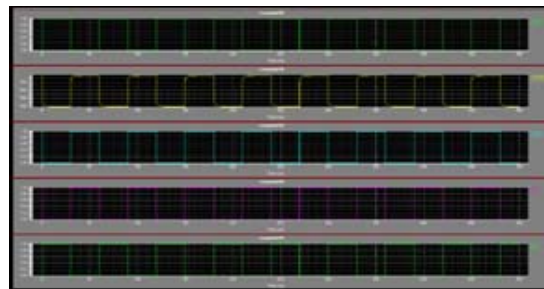Fig. 6 Simulation Wave form of hybrid Full Adder at 45nm

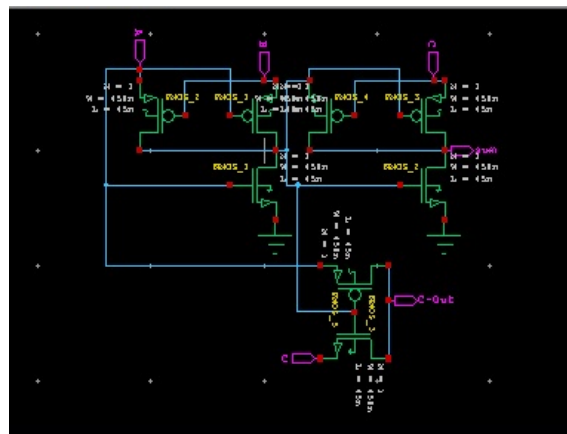Fig. 7 Simulation Wave form of hybrid Full Adder at 90nm

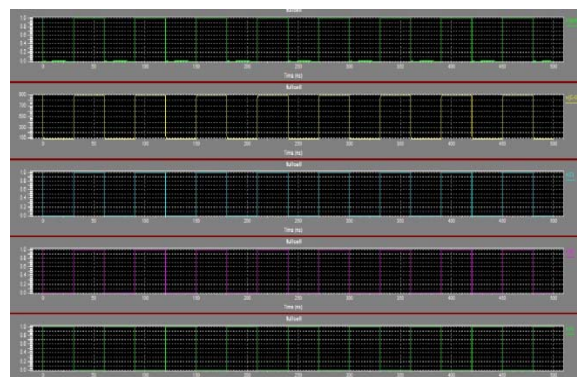Fig. 8 Schematic Design of PROPOSE 8T Full Adder

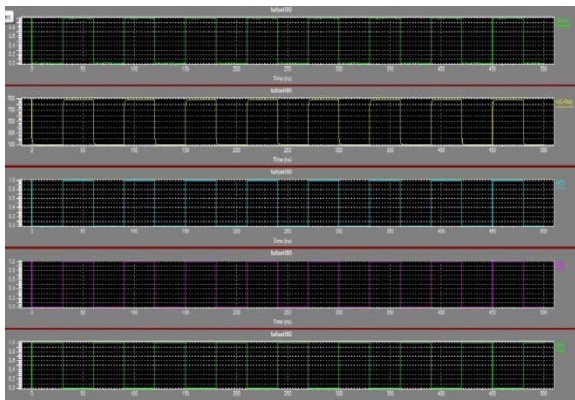Fig. 9 Simulation Wave form of PROPOSE 8T Full Adder at 45nm

Fig. 10 Simulation Wave form of PROPOSE 8T Full Adder at 90nm

Design	Delay ($\times 10^{-11}$s)	Power ($\times 10^{-6}$W)	PDP ($\times 10^{-17}$ J)	Vdd V
Hybrid	2.080	0.396	0.824	0.7
PROPSE-8T	2.215	0.322	0.714	0.7

Table: 3 Hybrid and PROPOSE-8T Results at 90nm

Design	Delay ($\times 10^{-11}$s)	Power ($\times 10^{-6}$W)	PDP ($\times 10^{-17}$ J)	Vdd V
Hybrid	1.877	.360	0.675	0.7
PROPSE-8T	2.012	0.278	0.559	0.7

Table: 4 Hybrid and PROPOSE-8T Results at 45nm

According to Simulation results we are able to measure power delay product (PDP) through Delay and Power multiplication for Hybrid Full adder and PROPOSE-8T Full Adder. PROPOSE-8T provide better PDP, Voltage Swing Compare to Hybrid Full Adder but the same time PROPOSE-8T lacking on the Basis of Propagation

Delay

Delay by the hybrid full Adder technique. For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. It is apparent that among the existing full adders, the proposed full adder cell has the smallest delay because of just having two transistors in the critical path for driving the output. The PROPOSE-8T full adder follows the hybrid adder in outperforming the other four full adder cells in delay. Propose full adder in shows the least delay because of remving a XOR-XNOR design to produce internal signals, which is based on complementary pass transistor logic (CPL).The first half

Power

The proposed 8T full adder shows the best performance among the above mentioned full adders under varying supply voltages. The PROPOSE-8T- full adder utilizes PROPOSE-8T structure as its main cell which is proved in to be one of the lowest power consumer cells that not only is suitable for designing fast, Low- Power circuits but also improves logic level swing and static power characteristics. Hybrid full adder cell follows PROPOSE-8T full adder in outperforming the other full adder cells in power consumption. The Hybrid full adder cell consume slow static power due to removal of any direct path between Vdd and the ground by employing NMOSs and PMOSs in a complementary manner. The PROPOSE-8T full adder shows minimum power consumption at all supply voltages when compared to the Hybrid full adder.

Power-Delay-Product (PDP)

The PDP is a quantitative measure of the efficiency and a compromise between power dissipation and speed. PDP is particularly important when low power operation is needed. The Power-Delay- Product for Hybrid full adder in two full adder cells is evaluated under different supply voltages (0.8–1.4V) in 90nm and (0.6–1.2V in 45nm. Illustrate the values of PDP of the 1-bit adder based on each full adder cells. Tables 3 and 4 illustrate the values at 0.7V for 90 nm and 0.7 for 45nm. As shown the PROPOSE-8T full adder has the best PDP in comparison with its counterpart.

Conclusion

In this paper two novel full adder cells using PROPOSE-8T structure and hybrid CMOS logic style for Low-Power application are proposed. These two new designs successfully operate at low voltages with tremendous signal integrity and driving capability. The circuits being studied are optimized for energy efficiency at 90nm and 45nm PD SOI CMOS process technology.

Simulations have been performed on PTM to evaluate the new designs. Hybrid full adder in and. A broad comparison to the state of the art designs cited in the VLSI literature illustrates a significant improvement in terms of power dissipation and Power- Delay product (PDP) parameter. The number of transistors used is significantly reduced resulting in a great reduction in switching activity and area. This considerable reduction in power by minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP.

References

[1] R. Shalem, E.John, L.K.John, A novel low-power energy recovery full adder cell, in: Proceedings of the Great Lakes Symposium on VLSI, February 1999, pp. 380–383.

[6] R.X. Gu, M.-I.Elmasry, Power dissipation analysis and optimization of deep submicron CMOS digital circuits, IEEE Journal of Solid-State Circuits 31(5) (1996)707–713.

[3] V. Dessard, SOI Specific Analog Techniques for Low-noise ,High-temperature or Ultra-low Power Circuits, Ph.D. Thesis, UCL, Louvain, Belgium,2001.

[4] D. Hassoune, I.O Flandre, Connor, J.D.Legat, ULPFA: a new efficient design of a power-aware full adder, IEEE Transactions on Circuits and Systems—I: Regular Papers 57 (8) (2010).

[5] V. Kilchytska, D.Levacq, L.Vancaillie, D.Flandre, On the great potential of non- doped MOSFETs for analog applications in partially-depleted SOI CMOS process, Solid State Electronics 49 (5) (2005) 708–715.

[6] J.-M. Wang, S.-C.Fang, W.-S.Feng, New efficient designs for XOR and XNOR functions on the transistor level, IEEE Journal of Solid-State Circuits 29 (7) (1994) 780–786.

[7] Arkadiy Morgenshtein, A.Fish, Israel A.Wagner, Gate-diffusion input (PROPOSE-8T): a power-efficient method for digital combinatorial circuits, IEEE Transactions on VLSI Systems (2002) 566–581.

[8] Vahid Foroutan, Mohammad Reza Taheri, KeivanNavi, Arash Azizi Mazreah, Design of two Low-Power full adder cells using PROPOSE-8T structure and hybrid CMOS logic style, INTEGRATION, the VLSI journal 47(2014)48–61.