IMPROVEMENTS IN BIST DESIGN OF SEED GENERATOR FOR LOW POWER TPG

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Abstract

In this paper, an overview of existing techniques for reduction in power dissipation in a Built-In Self-Test (BIST) is done, with more emphasis on the Linear Feedback Shift Register (LFSR)-based pattern generation approach. A novel technique for seed generation using combinational logic is then proposed in place of the LFSR for seed generation. This can then be XOR-ed with a gray code generator driven by an m-bit counter, to give a new test pattern generator (TPG) which will have a notable improvement in transition density at the source pattern input. The proposed technique gives a minimum hamming distance of one, between each consecutive test pattern, thus improving coefficient of correlation between successive test patterns, without significantly affecting fault coverage. A reduction in power dissipation of 63.27% was obtained. Results were verified with the help of simulations obtained through the Cadence tool.

Index Terms: BIST (Built-In Self-Test), LFSR (Linear feedback Shift Register), Low power, TPG (Test Pattern Generator).

I. INTRODUCTION

With the constant scaling down of technology of micro components in SOC and other electronic devices, and the increasing requirement of portability of devices, power dissipation is a key parameter for reduction. A circuit under test mode has a notably higher level of power dissipation than a circuit under normal mode of functioning.[1] This may be due to three possible reasons:

1. Due to randomness in generation of test patterns, power dissipation due to increased switching activity will increase. This is due to reduced correlation between the generated test pattern inputs.
2. Parallel testing processes used in test mode will reduce application time of the test, however increasing the power dissipation.
3. DFT (design for test) circuit which is in-built, will be active for a large time in test mode, as opposed to its idle state in the normal mode of functioning.

BIST or Built-In Self-Test, is a technique that allows lesser overhead and faster testing by incorporating testing capability within the device itself, thus reducing reliance on expensive machinery such as ATE (Automatic Testing Equipment). It is essential to counter the high power dissipation in test mode for BIST in order to create better circuit designs in VLSI. Three main types of seed generators used in BIST include scan-based[1,9,10], counter-based[2], and LFSR-based[5,6]. LFSR based approach is the one found to be most optimum, and hence commonly used[3].

In this paper, we shall be focusing on techniques to reduce power dissipation in BIST using an LP-LFSR-based approach with a TPG. A novel approach to this seed generation shall then be proposed.

II. PRIOR WORK

The focus of research in this specific area of test pattern generation in BIST is to reduce power dissipation by improving the correlation between the pseudorandom inputs that are generated. This has been done by either using hamming distances between inputs as a parameter, thus reducing transition density, or by removing redundant patterns that do not have any impact on fault coverage [3].

Praveen J, et al [4], describe a novel approach of clock-gating wherein a slower clock is used at the inputs to reduce transition density. A normal speed clock is used at the ODA (output data analyser). Power dissipation due to switching action caused by test pattern inputs is found to be directly proportional to the transition density.

Dhanesh P [2] on the other hand, proposes the use of two different threshold voltages for the critical and non-critical path through the circuit. By using a lower threshold voltage for the critical path through the circuit, a comparatively lower level of power dissipation (static power) is obtained.

The selection of the seed pattern is also important as a correctly chosen seed can reduce bit changes by a large extent, as illustrated by R. Bhakthavatchalu [7]. A deterministic seed was found to provide the same fault coverage as an arbitrary seed but while using a lesser number of random test patterns. Further progress was shown by Emina, at al [8] involving the concurrent generation of pseudorandom numbers in an LFSR of the internal type. Internal type LFSR is one where the XOR gates are applied within the flip-flop based LFSR architecture itself, and not external to it. This Galois approach also suggested a polynomial-based dynamic LFSR which could change the primitive polynomial for which it was constructed so as to reduce switching wherever possible.

K Vasudevareddy [9] and Dr S Senthil Kumar [10], used the LFSR approach in combination with a scan-chain technique to improve fault coverage capabilities of the BIST.

III. METHODOLOGY

Built-In-self-test approach:

BIST is a DFT (Design for testability) technique. At the system level, it's a low cost test solution which eliminates the difficulties of external testing by using built in hardware features.

Additional circuitry is placed on the chip which provides easy access in testing of internal modules as well as the internal points and hence also reduces the number of test access pin required on the board. Testing can also be done at the normal operating speed which reduces the cost of using an ATE. With advances in integration the costs of adding extra circuitry on chip is decreasing, making BIST an attractive feasible and user friendly alternative to external testing.

The block level of BIST is as shown in Fig, 1. It consists of 4 major blocks:

1) TPG which is used to generate pseudo random sequences,

2) Input isolation circuitry used to select between the normal mode of operation and the test mode,

3) TCL (Test controller logic) is used to sequence and run all the activities of the BIST scheme,

4) Response analyser acts as a comparator used to compare the outputs from the circuit under test with the golden signature responses and tells whether the circuit passes or fails the test.

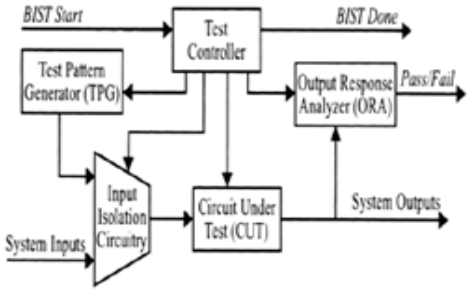

Fig. 1: BIST block diagram [5]

Working of a low power TPG:

The LP-TPG consists of a n-bit counter, gray code generator, LP-LFSR, XOR-gate and NOR-gate as shown in Fig 2. Counter and gray code generator are synchronized with common

clock.

The m-bit counter generates test patterns from zero to 2m values. When counter output is all zero pattern, the output of a NOR gate is one, when the clock signal is applied, the next seed value is produced. By using a counter and a NOR-gate, the decoder logic can be eliminated for the generation of seed value.

A low power Linear Feedback Shift Register (LP-LFSR) generates test patterns with reduced switching activities.

An XOR of the seed and the output sequence from the gray code generator are done to generate the final output. This helps in effectively reducing the switching activities and hence reducing power.

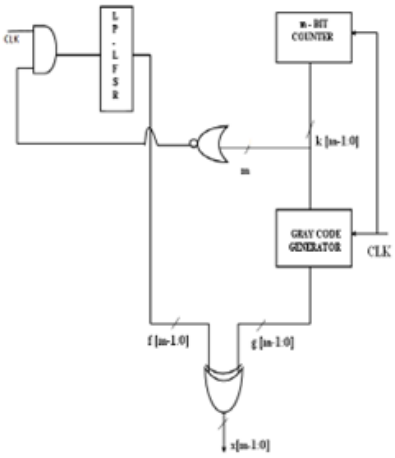

Fig. 2: Low power TPG design [5]

The algorithm for test pattern generation using LP-TPG is as given below [11]:

1. Consider an n-bit linear feedback shift register [n>2] which consists of n-flip flops with a common clock.
2. If the output of last stage flip flop is one then any one of the flip flop output value is swapped with its adjacent flip flop output value.
3. If the output of last stage of the flip flop is zero then swapping will not be carried out.
4. Multiplexers are used for exchanging the output of adjacent flip flops. The select line for the multiplexer is selected to be the output of the last stage.
5. The output of the multiplexer gives the finally generated seed values.
6. Gray converter is XOR-ed along with seed values to generate random test patterns `with 1-bit difference between two successive values.

We have proposed a slight modification in the LP-LFSR design as shown which further reduces the switching action in the LP-LFSR and hence reduces the power consumption.

Proposed Modification

The following design gives fewer transitions as compared to the previous design and hence reduces power. The design also eliminates the XOR-gate used in LFSR previously.

Algorithm:

1. The select line for the multiplexers are the outputs of the adjacent D-flip flop.
2. If the select line is zero, then the output is same as the input and if the select line is one then the output is the negation of the output from the flip flop i.e. when select=0, output is taken from Q else output is taken from Qbar.
3. The output of the mux gives the finally generated seed values

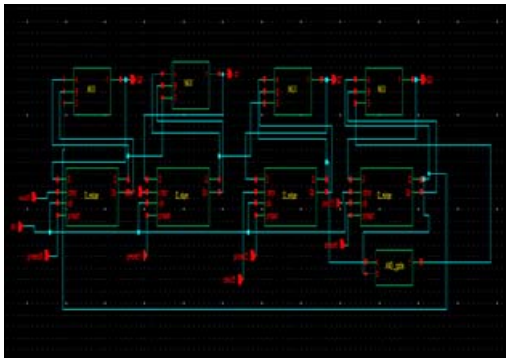

Fig. 3: Proposed design for seed generation

The power obtained through this design was found to be notably lesser than that obtained in [2], as illustrated in the results section.

IV. RESULTS

As obtained by Dhanesh [2], the results of employing bit swapping with dual thresholds shows a decrease in static power. In mobile devices, static power is a major concern as standby mode is more probable to occur than active mode. The comparison with the design proposed in this paper was found to be as shown in Table 1:

TABLE I POWER CONSUMPTION

Seed Pattern	Static	Total Power

Generator	Power	
BS-LFSR[2]	1.2601uW	1.2601uW
BS-LFSR with dual threshold[2]	1.2012uW	4.7861uW
Proposed Design	0.4628uW	2.7203uW

Thus a reduction in static power of 63.27% was achieved in this technique.

V. CONCLUSION AND FUTURE SCOPE

A. Conclusion

Different techniques to reduce power dissipation in BIST were overviewed, and a novel technique for reducing switching action at the source inputs was designed by replacing the traditional LFSR approach for seed generation, with a combinational circuit such that the final TPG would have minimum hamming distance between test patterns. The proposed design was simulated and verified using the Cadence tool. A further implementation of this approach by employing dual threshold voltages was suggested based on finding the critical and non-critical paths through the circuit.

B. Future Scope

The bit-swapping LFSR used by Dhanesh [2] generates a random test sequence with low switching power by finding hamming distance between two adjacent patterns and minimizing that distance by using combinational logic. To further reduce the average power, dual threshold voltages are assigned. By using this method and finding out the critical and non-critical paths present in BIST and then assigning a low threshold voltage for critical path, and high threshold voltage for non-critical path, a further reduction in total power, especially leakage power, can be obtained.

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