LOW POWER WIDE FAN IN DOMINO OR LOGICS

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Abstract

A low power design technique for high fan in domino logic circuits is presented. An nMOS transistor stack is used to reduce the leakage current of the pull down network due to the stacking effect, hence improving the robustness of the circuit against deep sub-micron sub-threshold leakage. This decreases current contention and leakage current too. The proposed technique exhibits considerable improvement in power dissipation as compared to standard domino logics. Domino comparator is designed using the proposed scheme and conventional techniques to demonstrate the effectiveness of the proposed scheme in improving leakage-tolerance and performance of high fan-in circuits. The simulation is done using MENTOR GRAPHICS TOOL with 180 nm technology.

Keywords: domino logic, delay, power consumption, threshold voltage, technology scaling.

I. INTRODUCTION

As the technology shrivels in the modern period the demand of the higher speed, smaller chip area as well as lower-power consumption in the microprocessors has come into the existence. Domino CMOS logics are extensively used in current days for the designing of high-fan in higher-performances circuits of the latest IC chips and the microprocessor. Property of higher speed in addition to the lesser-area of domino logics in comparison to former schemes makes them the better widespread prime selection in the designing of the higher speed systems. By means of advancements in great performance processor, high fan-in comparator is progressively more being engaged for the Arithmetic-Logic Unit (ALUs), Central-Processing Unit (CPUs) which forms critical path. The processing technologies and the supply-voltages which are scaled at a quicker rate, V_{th} (threshold voltages) should be reduced down in the way similar to achieve the higher performance because of the scaling of the threshold-voltage, leakage-power also surges considerably in the ultra-deep sub-micron (UDSM) technology.

As technology is scaled down, power supply must be scaled to decrease power consumption which in turn increases leakage current and parasitic capacitance contributing towards increased power dissipation. Here a new domino circuitry is proposed which has very low power dissipation. This is achieved by stacking effect. This decreases current contention and leakage current too. The simulation is done using MENTOR GRAPHICS TOOL with TSMC 180 nm technology.

The paper is organized as follows: Literature review about existing domino circuit discussed in section II. The proposed circuit description is in Section III. Section IV details on the design example to demonstrate the effectiveness of proposed design. Simulation result is presented and compared in section V with the brief conclusion of the paper in section VI.

II. LITERATURE REVIEW

Several domino circuits have been proposed in the literature such as conventional higher fan-in domino OR logic with footer less and footer transistor, high speed domino, conditional keeper

domino, wide OR gate diode footer domino. The main goal of these circuit design technique is to improved Power consumption, Delay and Area for high circuit performance, especially for wide fanin circuit.

Using a keeper transistor helps to address the problems of leakage and charge sharing but increases power dissipation. So sizing the keeper transistor helps to overcome the problem but then tradeoff occurs between reliability and performance.

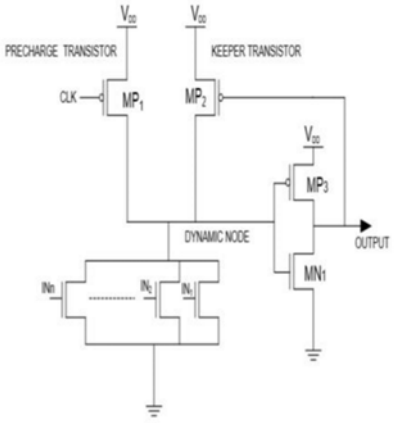

Fig. 2.1 Standard Footless Domino Logic Circuit

SFLD is shown in fig. 2.1.Footless design [1] is featured by fact that the discharge of the dynamic-node is done at faster rate. This characteristic is exploited by high-performance circuits.

The footed domino logic [1] as shown in fig. 2.2, footer nMOS transistor MN2 is connected to the source of evaluation nMOS transistor to obtain the FDL design which basically reduces the leakage current. The speed the SFDL is lower than the footless one because of the stacking effect, but the noise immunity is higher.

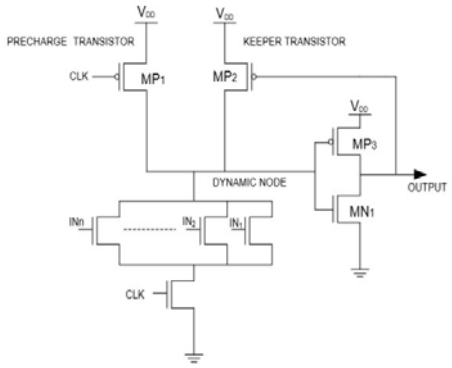

Fig. 2.2 Standard Footed Domino Logic Circuit

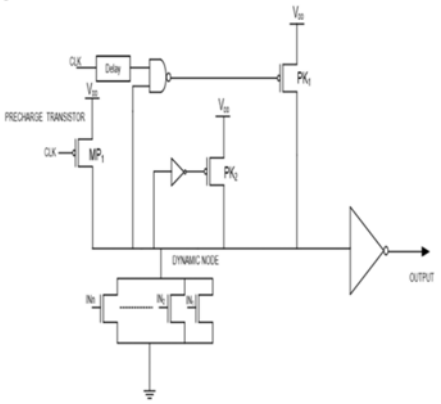

Fig. 2.3 Conditional Keeper Domino Logic Circuit

Conditional Keeper [1] is named so because it employs two keeper transistors shown in fig. 2.3; a smaller keeper and larger keeper which are activated based on the condition evaluated by NAND gate. In this design scheme, the keeper-transistor (PK) is conventional domino keeper is divided into the two smaller transistors, PK1 and the PK2. As the clock goes high Pk2 is ON, after delay of two inverters keeper Pk1 goes ON only if output of NAND gate goes LOW. NAND output is low only if both delayed inverters and dynamic node are HIGH. Main drawback of this circuit is delay increases due to two inverters and NAND gate.

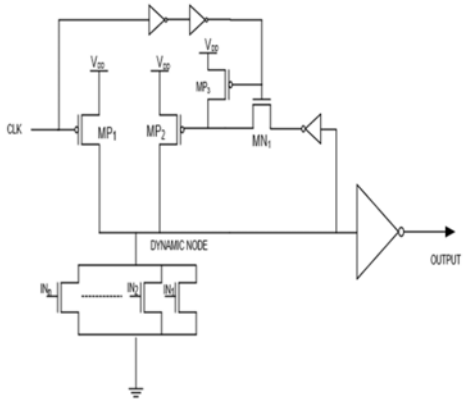

Fig. 2.4 High Speed Domino Logic Circuit

One of the existing leakage tolerant domino circuits is high speed domino logic (HSD) as shown in Fig 2.4. At the beginning of the evaluation phase, the input delay element is low and the clock is high. PMOS transistor MP3 is ON and therefore it turns OFF the keeper transistor MP2. After a delay equal to the delay of the inverters, when clock delayed is high, if the output node is high, MN1 remains in the OFF.

III. PROPOSED DOMINO CIRCUIT

The proposed scheme employs stacking effect for improvement in power dissipation, robustness and the performance of the circuit. The operation of the proposed-circuit is analyzed for the different operational phases:

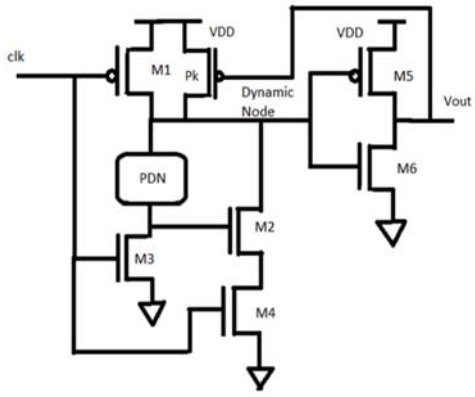

Fig. 3.1 Proposed Domino Logic Circuit

Pre-charge mode: While the clock is at lower logic, the domino-logic circuit is in the pre-charge phase. The dynamic-node charges to the VDD at the same time node output stays at low logic. The output is fed back to keeper transistor Pk and then activates it. The keeper transistor Pk aids to sustain the charges at the dynamic-node which may be lost due to the leakage. During this phase the NMOS-transistors M2, M3, M4 are off. As these transistors form a series stack, they prevent any leakage-current during this phase.

Evaluation mode: All the inputs are zero: As the clock becomes high during the evaluation-period M1 is turned off; transistors M3 and M4 are turned on. Charge at the dynamic-node is maintained by keeper transistor Pk. Since the applied inputs are at low logic, the pull-down network is in standby mode. This makes the one of the transistor in stack to be off, so by stacking effect again there is no leakage current. Similarly the transistor M2 is off while M4 is conducting forming the stack and reducing the leakage.

The input switching high: When minimum of one of input to PDN is higher, the dynamic charge gets cleared through the PDN making output node to go high-logic level. The dis-charge of dynamicnode charge also takes place through the second path which comprises the M2 and M4 transistors. This faster dis-charge of the dynamic-node enhances speed of circuit.

IV. DESIGN EXAMPLE

To demonstrate the effectiveness of the proposed technique, we have employed it in the design of a high fan-in comparator. This design is described and compared with the conventional counterparts in this section.

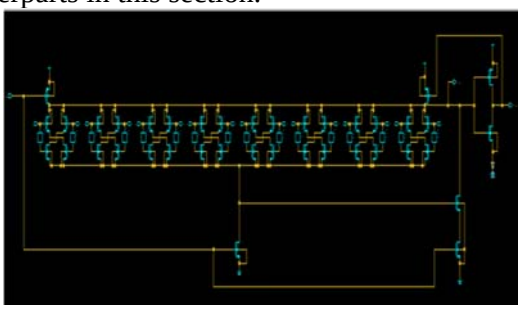

Fig. 4.1 Schematic of Proposed scheme

Fig. 4.1 shows the schematic of a high fan-in (8-input) domino comparator based on proposed domino scheme. The operation is explained in the two phases:

Inequality: If the two inputs A and the B are not same at least at the single bit, that leg corresponding to inequality becomes active in pull down networks, gives the path for discharging to the dynamic-node via the footer transistors. As the dynamic-node starts discharging, output node voltages starts to increase corresponding to high logic. With presence of the proposed-domino circuit, the rate of the discharging of the dynamicnode is faster. Since the additional 3 transistors are conducting only for the petite duration of time, these transistors do not cause any extra power dissipations.

Equality: The case when of all the bits of both the inputs are equivalent, none path of PDN is conducting and every leg has at least one of the transistors OFF. As now there are no discharging paths available to the dynamic node, node voltage maintained. And hence the output is at low-level.

V. SIMULATION RESULTS AND DISCUSSIONS

The proposed circuit and conventional techniques are simulated using mentor graphics in the TSMC180nm technology at 27^0c and 110^0c.

The supply voltage used in the simulations is 1.8V.

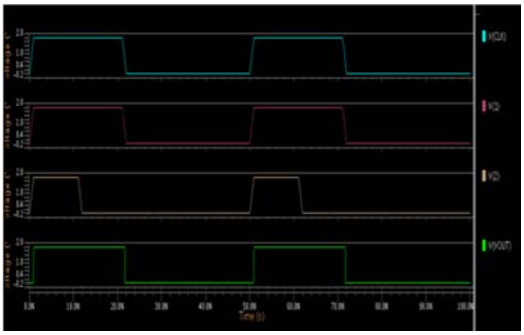

Fig. 5.1 shows output of OR gate using proposed scheme

The above fig. 5.1 shows the transient analysis of the waveforms of inputs, output and clock with respect to time. Table I and II provides the power dissipation and delay for the 8 input Domino OR logic.

Table I Comparison of power-dissipation

DOMINO LOGIC	POWER DISSIPAT -ION (uW) 27°C	POWER DISSIPAT -ION (uW) 110°C
OR	198.101	271.185
SFLD	127.859	204.7648
SFD	93.271	184.958
CKD	129.219	249.867
HSD	71.581	171.510
PROPOSE D	35.6481	89.2561

Table II Comparison of Delay of domino logics

DOMINO LOGIC	DELAY (ns)	POWER DELAY PRODUC T(pJ)
OR	257.21	0.509
SFLD	80.01	0.1023
SFD	189.96 2	0.1771
CKD	119.86 7	0.1548
HSD	107.81	0.0771
PROPOSE D	119.08	0.0423

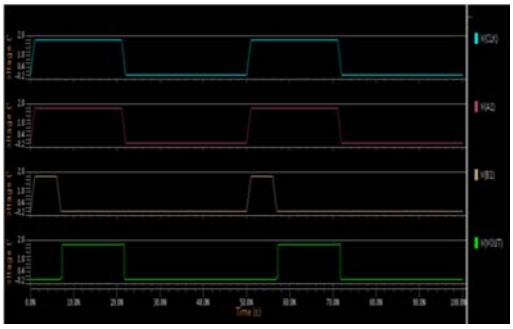

Fig. 5.2 shows output of domino comparator using proposed scheme

Table III Comparison of power-dissipation of domino Comparators

DOMINO LOGIC	POWER DISSIPATION(uW) 27°C
SFLD	171.4364
HSD	107.1543
PROPOSED	92.941

Table IV Comparison of Delay of domino comparators

DOMINO LOGIC	DELAY (ns)	POWER DELAY PRODU CT(pJ)
SFLD	91.427	0.1567
HSD	111.842	0.0198
PROPOSED	114.941	0.0106

From the simulation results it is clear that the proposed circuit provides less power dissipation, better performance compared to the various domino logics.

VI. CONCLUSION

In this paper a new scheme for the domino logic is proposed which is robust and noise tolerant. The existing and proposed circuit is simulated using Mentor Graphics simulator using TSMC 180nm at the power supply of 1.8V for 8 input for Wide fan-in OR gate. The proposed circuit can be used in design of high-speed embedded processors where low power consumption is an essential requirement. The circuit is flexible and quite applicable for large fan-in gates.

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