LOW POWER VLSI TESTING – OVERVIEW

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Abstract

An unintended consequence of technology scaling has increased power consumption in a chip. Without specialized solutions, level of power consumption and the rate of change of power consumption is even greater during test. VLSI testing encompasses all spectrums of test methods and structures embedded in a system-on-chip to ensure the quality of manufactured devices during manufacturing test. Test methods typically include fault simulation and test generation, so that quality test patterns can be supplied to each device. The test structures often employ specific design for testability (DFT) techniques, such as scan design and built-in-self-test (BIST), to test the digital logic portions of the device. The test methods and structures are required to improve the product quality and reduce the defect level and test cost of the manufacturing devices, while at the same time simplifying the test, debug, and diagnosis tasks.

Keywords: ATE-Automatic Test Equipment, CAD-Computer Aided Design, EDA-Electronic Design Automation

INTRODUCTION

Logic testing involves the process of testing the digital logic portion of a circuit under test (CUT). The digital logic can be reconfigured in the test mode to include test logic to improve the testability and test quality of circuit. Logic testing typically consists of applying a set of test stimuli to the inputs of the digital logic while analyzing the output responses. Both input test stimuli and output response analysis can be generated and performed externally or inside the chip. Circuits that produce the correct output responses for all input stimuli pass the test and are considered to be fault-free. Those circuits that fail to produce a correct response at any point during test sequence are assumed to be faulty.

In general functional test patterns and structural test patterns can be used as manufacturing tests. Applying all possible input test patterns to an n-input combinational circuit illustrates the basic idea of functional testing where every entry in the truth table for the combinational logic circuit is tested to determine whether it produces the correct response. A more practical approach is structural testing where test patterns are selected based on the circuit structural information and a set of fault models. A diversity of defects makes it difficult to generate tests for real defects. Fault models are necessary for generating and evaluating a set of test patterns. Some well-known and commonly used fault models include the following:

1. Gate-level stuck-at fault model: The stuck-at fault is a logical fault model that transforms the correct value on the faulty signal line to appear to be stuck-at a constant logic value, either logic0 or 1, referred to as stuck-at-0 (SA0) or stuck-at- 1 (SA1), respectively [1].
2. Transistor-level stuck fault model: At the switch level a transistor can be stuck-off or stuck-on, which are referred to as stuck-open or stuck-short, respectively [5].
3. Bridging fault models: A short between two wires is commonly referred to as a bridging fault. The case of a wire being shorted to V_{DD} or V_{SS} is equivalent to the line stuck at fault model; however when two signal wires are shorted together, bridging fault models are needed [3].

4. Delay fault models: Resistive opens and shorts as well as parameter variations in transistors can cause excessive delays such that the total propagation delay falls outside the

specified limit. Delay faults have become prevalent with decreasing feature sizes and different fault delay models are available. In gate-delay fault and transition fault models, a delay fault occurs when the time interval for a transition through a single gate exceeds its specified range. The path-delay model, on the contrary, considers the cumulative propagation delay along any signal path through the circuit [2].

As tests generated for one fault model can potentially detect faults of other models, identifying a good fault model to target during test generation can help reduce the number of test vectors and in turn test time. A common practice is to target delay faults first, followed by gate-level stuck-at faults, bridging faults, and finally transistor-level stuck faults.

Power dissipation is one of the critical parameter during manufacturing test as the devices can consume much more power during testing than during functional mode of operation. Power consumption in CMOS circuits can be classified into static and dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply. Dynamic dissipation is due to (i) short circuit current and (ii) charging and discharging of load-capacitance during output switching. The total power consumption of the CMOS circuit is expressed as the sum of the three components:

$$Ptotal = Pstat + Pd + Psc$$

In typical CMOS circuits, the capacitive dissipation was by far the dominant factor. However, with the advent of deepsubmicron regime in CMOS technology, the static (or leakage) consumption of power has grown rapidly and account for more than 25% of power consumption in SOCs and 40% of power consumption in high performance logic (ITRS 2007).

Power management strategies such as dynamic voltage scaling, clock gating or power-gating techniques are used to control the power dissipation during functional operation. The use of these strategies has various implications on manufacturing test, and power aware testing is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. Reliability, test throughput and manufacturing yield can be affected by test power, thus impacting overall product quality and cost, dedicated test methodologies have emerged over the past two decades. Test techniques were proposed with the intent to reduce or constraint power during manufacturing test.

Over the years, this research area has gained more importance, especially from the industrial community and efforts were brought to propose power aware solutions not only efficient in reducing power consumption but also in minimizing the negative impact on design flow, circuit performance, test data volume, test time, area overhead etc.,

Organization of the paper: The paper is divided in to four sections. Section-1 gives the reasons for excessive test power, Section-2 discusses main test power issues, and Section-3 covers briefly power aware testing strategies and Section-4 briefs on testing low power designs.

Section-1: Reasons for excessive test power

Power during at-speed scan testing can be 3.8 times the power consumed during functional mode. Main reasons that can explain this excessive power during test are

- No correlation between consecutive test vectors while there is usually a strong correlation between consecutive vectors used in normal mode of operation.
- Test vectors may ignore functional power constraints and hence stress the circuit under test much more than it is in functional mode.
- Non functional clocking schemes are used during test while low-power clocking schemes can be used during functional mode.
- Design for testability (DFT) circuitry is intensively used, while it is in idle mode during functional operation.
- Concurrent testing is often used for test time efficiency, thus increasing the overall switching activity well above the switching activity during functional mode.
- Compression and compaction are often used for test data volume reduction, hence leading to test vectors with higher switching induced capabilities.

The problem of excessive test power has become worse with the wide spread use of at-speed scan

testing, which is now mandatory for performance verification. Irrespective of the test scheme used the problem of excessive power during testing can be split into two sub-problems

1. Excessive power during shift cycle
2. Excessive power during Launch-To-Capture(LTC) cycle

As no value has to be captured during the shift cycles, the occurrence of one excessive peak of current is not relevant. However, if several successive high peaks of current occur then the problem amounts to high average power consumption, and one may lead to test power issues. On the other hand, logic values have to be captured during the LTC cycle; in this case only one excessive peak of current may be an issue and lead to test-induced yield loss.

Section-2: Main test power issues are

- Issues due to excessive average power
  - Circuit related
  - Test process/cost related.

Switching operations of a circuit always leads to heat dissipation. If the circuit temperature is too high even during a short duration of on-line test session it may have the following circuit related issues.

- Chip damage
- Reduced reliability
- Yield loss and following test process/cost related issue is Low test throughput.
- Issues due to excessive peak power

  Excessive peak power consumption may occur while testing the circuit at the wafer level or at the chip level. Excessive peak power comes from a high instantaneous current demand from a high switching activity during test and may lead to considerable voltage drops at power grid nodes. Voltage drop in the power grid also called Power Distribution Network-PDN is mainly due to two components, they are IR-drop and L(di/dt).

  These two components are often referred to as Power Supply Noise-PSN. With high peak current demands during test, PSN may become much higher than during functional mode and so no longer negligible. With increased PSN, the voltages at some gates in the circuit are reduced and these gates exhibit higher delays (performance degradation), possibly leading to test failures (good dies are declared faulty) and hence yield loss. In order to avoid excessive peak power consumption and its related issues, it is important to reduce the level of switching activity during test.

Section-3: Power-Aware Testing Strategies

1. Test data manipulation for power reduction
2. Design for test power reduction
3. Power aware test data compression
4. System level power aware test scheduling

1. Power-aware test pattern generation for scan testing can be used for either shift power reduction or capture power reduction. A typical constraint is a user defined toggling activity limit that needs to be satisfied for each test pattern generated. During test pattern generation don't care bits can be replaced to keep the toggling activity under the specified limit. Judicious filling of don't care bits to achieve significant reduction in test power consumption can also be used. So far 0fill, 1-fill, minimum transition-fill and adjacent-fill techniques are used to reduce average/peak power during scan shifting or during launch to capture. The major advantage of low-power test generation is that it causes neither area overhead nor performance degradation. There are few issues that need to be addressed in the future with regard to low-power test generation. (i) More effective and efficient flows for low-power test generation need to be developed by using the best combination of individual techniques in low-power test generation and low-power design for testability (DFT). (ii) Faster and more accurate techniques need to be developed for analyzing the impact of test power instead of test power itself. For capture power, this means researchers should look beyond numerical switching activity and IR-drop to direct investigation of the impact of test power on timing. (iii) More sophisticated power reduction techniques capable of focusing on regions that really need test power reduction should be developed.

2. Dedicated DFT solutions offer a structured and configurable means to reduce test power consumption. A simple solution to drastically reduce combinational logic toggling that happens during scan shifting is to incorporate a blocking circuitry to all or some

outputs of the scan flip-flops. Various ways of implementing the blocking logic are using multiplexers, transmission gates, adding NOR-gates as a blocking element or using the scan enable of the flip-flops. Alternatively shift power can be reduced by changing the order of the scan cells in each scan chain of the design. Another technique is in inserting logic elements (XOR-gates) between scan cells so as to minimize the occurrence of transitions in the scan chains and hence in the combinational logic during shift operations. Another technique used widely is scan segmentation, in which the scan chain is divided into two or more scan chain segments and then activating one segment at a time while loading and unloading test data. Power -aware DFT techniques when used must be used such that test power should not be reduced below functional power to avoid concerns related to circuit understanding.

3. Power-Aware test data compression is an efficient solution to reduce test data volume. It involves encoding a test set so as to reduce its size and hence tester memory for storing the test data. During test application a small on chip decoder is used to decompress test data as it is fed to the scan chains. The goal of power aware code based test data compression (TDC) is to use data compression codes to encode the test data so that both switching activity generated in the scan chains after on-chip decompression and test data volume can be minimized. The TDC techniques can be code based, linear decompression based or broadcast based. Low-power test compression has received attention in the research community and commercial tools have been emerged. The DFT methods allow testing of integrated circuits without exceeding power limits and thereby reduce yield loss and test cost.

4. System level power-aware test scheduling is for SOCs with a set of defining wrapped cores. A test scheduling is a process that decides in which order to test each core. The goal of these techniques is to test the cores (memory, logic, analog etc.) of an SOC in parallel, at each stage of a test session, keeping power dissipation under specified limit, while optimizing test time.

Power-aware test planning can be used to guide the:

- Test-plan exploration, which is to find a test order with a minimal test application time while meeting power constraints
- Design exploration to find where to: o Insert power-aware DFT and/or o Over-design to handle high power

While the test plan results in a minimal test application time and minimal additional cost while meeting power constraints. Integrated circuits are increasingly designed in modular form and the advantage with modular testing is that it allows test planning, which is a low-cost alternative to control test power consumption.

Section-4: Testing of low power designs

In the nanometer technology regime, power dissipation has emerged as a major design consideration. Although dynamic power traditionally has been the significant form of power consumption in submicron process nodes, aggressive technology scaling has exposed the secondary problem of leakage power, which contributes to nearly 20–50% of total power in deep submicron modern microprocessors. Power reduction has been addressed at different levels of design abstraction: from system to architecture to circuit. Existing power reduction approaches can be broadly classified into two categories (i) dynamic power reduction techniques and (ii) Static or leakage power reduction techniques. Some of the dynamic power reduction techniques are circuit optimization for low power, clock gating, operand isolation and advanced power/thermal management, while few leakage power reduction techniques are input vector control, dual V_{th} design, and supply gating.

Advances in hardware/software based power management are dramatically driving down functional power dissipation, however they are also widening the gap between functional and test power. Among the various low power design techniques applicable from system to circuit and physical levels are

- Voltage scaling
- Clock gating and
- Power gating

These techniques have various implications on manufacturing test and need dedicated test

strategies. Most of the time above techniques are combined together to achieve maximum power optimization, thus increasing the difficulty of the task. Only few solutions have been proposed so far in literature for reducing test power of low power designs. These techniques can be classified into three categories

1. Test strategies for multi-voltage designs
2. Test strategies for gated clock designs 3. Test power management (PM) structures.

Reducing the power consumption of digital designs through the use of more than one V_{DD} value is well practiced and supported by commercial CAD tools. Multi voltage design styles lead to the creation of power islands, where the operating voltages are generated either through dedicated multiple power supplies on the chip or through adaptive voltage scaling circuitry consisting of DC-DC converters and voltage controlled oscillators. Designs that use multiple voltage settings are divided into various voltage domains during physical placement of the design. Each voltage domain feeds various logic blocks and level shifters are used to communicate logic values across logic blocks operating under different voltage settings. But designs with multi-voltage domains pose some issues to scan chain assembly. Most significant concern is that, scan chains that span multiple voltage domains cause power dissipation in level shifters. In order to minimize area overhead and power consumption in level shifters, multi-voltage aware scan-chain assembly attempts to consider the voltage domains of scan cells while ordering the cells in a scan chain so as to minimize the occurrence of chains that cross voltage domains.

Test infrastructures, like scan chains or Test Application Management (TAM) may cross several power domains and can be broken if some of these domains are temporarily powereddown for low power dissipation. Power-aware scan chain assembly allows testing of specific power domains by employing bypass multiplexers, which allows bypassing signals from power domains that are switched-off during test.

1. During scan shifting, the combinational logic need not meet the timing and so the clock frequency is usually much slower than the normal frequency of the design. So it is possible to use a power supply voltage during scan shifting to reduce both dynamic and leakage power during scan testing.

2. In low power designs, areas of logic not needed for the current state of operations are gated off with clock. By gating off clocks to state elements that are known to not needed for updating, the dynamic switching current can be reduced, thus reducing dynamic power. Not only in logic operations, but also in clock trees, clock gating is widely adopted and supported by existing EDA tools.

3. various power management techniques used to control dynamic and static power in integrated circuits are clock gating, power gating, voltage scaling. These techniques use clock gaters, state retention registers, power switches, isolation cells, level shifters etc. in power management structures, in addition to the challenges inherent in testing logic, all the structures used for power management need to be tested thoroughly including the logic that controls them. Testing techniques of the various structures used in power management structures is another area of research.

Power-aware testing is an active area of research and development that has steadily moved from research labs to practice in the past decade. With the ongoing advances in technologies such as 3D-architectures combined with the growing need for more power efficiency, innovation on poweraware testing will still be needed in the future, by considering additional constraints such as process variability, signal integrity, ATE limitations etc. In addition to the challenges inherent in testing logic that can operate in multiple power modes, it is necessary to thoroughly test all the power management features including the clock gaters, power gaters (or switches), the logic that controls them, and the low-power cells. Some of the challenges while testing power management structures include, (i) controlling clock gaters during test, (ii) impact on testability of the clock gater and its control logic, (iii) impact on power and pattern count. In designs that employ power gating strategies for reducing leakage power, the Power

Management Unit (PMU) controls power modes and orchestrates safe sequences between power modes. This in turn poses new test challenges. In addition, DFT changes are necessary to enable scan test in the presence of power gating, as well as to facilitate testing of the power control logic in the PMU.

To reduce power dissipation, especially leakage power dissipation introduced by shrinking process technologies, power switches are commonly used in modern low power designs. The insertion of power-gating transistors also introduces testing problems. Due to imperfection in the fabrication process causing manufacturing defects, the power gating transistors may not work properly. Therefore, it is extremely important to verify the correct functionality of the power switches and validate that they switch on when the control signal is enabled, and switch off when the control signal is disabled.

Designs with multi-voltage domains include a number of special cells such as State Retention Register (SRR), isolation cells, and level shifters. These cells logically behave like regular gates during normal structural tests, and are therefore tested by conventional fault models. However, their low-power features create additional test requirements.

The Power Distribution Network (PDN) delivers power and ground voltages from power pads in a wire-bond package or C4 (controlled collapse chip connect) bumps in a flip-chip package to all cells in a chip. A robust PDN is essential to ensure correct and reliable operation of modern high-performance VLSI circuits. As technology scales, designs are becoming increasingly sensitive to power supply noise impacting signal and power integrity. Power supply noise refers to the noise on the power and ground distribution network, which reduces the effective supply voltage, levels reaching gates in a circuit. In general, high average currents cause large ohmic IR voltage drops and the transient currents cause large inductive Ldi/dt ground bounce in the PDNs. The main effects of IR voltage drop and ground bounce are on circuit timing and signal integrity. Since power supply reduction will slow down the gate transition, IR drop and ground bounce affect setup and hold times as well as clock skew, which could potentially result in silicon failure. The PDN must be designed effectively to minimize the voltage drops and maintain the local supply voltage within specified noise margins. There is a fundamental difference between gate defect and PDN defect behaviour in a circuit. A gate defect can cause a gate to malfunction and impact the circuit function or timing behaviour. A PDN defect, however, may not necessarily result in a gate/circuit functional or timing failure. Contrary to the common assumption that defects in PDNs can typically be detected by implication during functional or structural tests, only a small percentage of defects that result in catastrophic failures may be detected during manufacturing test. In general, defects in PDNs could cause two types of problems in an integrated circuit:

(i) Functional/timing problem: Such problems are likely to be detected during manufacturing test.

(ii) Reliability problem: In this case, the chip under test passes the functional/ structural tests but an in-field failure occurs when the applied input pattern maximizes the effect of the PDN defect on circuit timing, or causes a malfunction in certain gates powered by the PDN. New test pattern generation methods must be developed to effectively deal with open and resistiveopen defects in PDNs. Since defects in power/ground vias and power wires adversely affect yield in addition to severely impacting reliability, time-to-market, and profitability, there is a need to detect these defects and identify their locations in the PDN to improve design quality and in-field reliability. An effective methodology must be adopted for testing the PDN faults and verifying the integrity of the PDN during pre-tapeout design validation.

Conclusion

Satisfying power dissipation requirements has become a critical component for design closure in a large number of integrated circuits. It is now in the designer's mind since the start of a design project. Traditional design-for-low-power techniques such as clock gating are no longer sufficient. Designers are forced to radically change their design practices by explicitly implementing more intrusive power management schemes. Designs are now architected based on challenging power consumption profiles, making use of multi-voltage domains, power domain shutoff, and

multi threshold cells. The creation of technology libraries requires more effort as cells need to be characterized for different voltages, and power and ground pins have to be explicitly visible in the logical domain. Because of the various challenges and tradeoffs, the test of advanced lowpower devices is more than ever in need of intelligent planning. And that planning needs to be done at early stage. Many poweraware DFT techniques do exist but each of them comes with a cost and a set of requirements. The key objective of the planning is to schedule the test of a design and decide on adequate DFT techniques while keeping power consumption under control.

The test of advanced low-power devices is making designs much more complex and very strictly optimized for power. Design for low power is changing the way designs are built. It is no longer seen as simple, contained incremental changes like gating the clocks, but it rapidly became very intrusive at the point where all of the EDA tools need to be made power aware and must have unified support for users' power intent. Looking at the low-power design flow in general, one of the important works is to enhance power analysis and estimation in terms of accuracy and speed, and have it linked at different stages in the flow where design is being optimized; which, of course, includes DFT synthesis. This will add the needed predictability which helps eliminates very costly design iterations.

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