# DESIGN OF SEQUENTIAL CIRCUITS USING MULTI-VALUED LOGIC BASED ON QDGFET

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**Abstract**

**In this paper, the design of different Ternary sequential circuits using Quantum Dot Gate Field Effect Transistor (QDGFET) is carried out. The design of various sequential circuits using QDGFET device which includes Ternary D - Flip Flop and Ternary Right Shift Register is discussed. The proposed Ternary Sequential Circuit design using QDGFET device results an improved circuit parameters and less circuit elements in implementing the sequential circuits such as Ternary D-Flip Flop and Ternary Right Shift Register using QDGFET. The results are simulated using T-SPICE simulator demonstrating that the proposed ternary Sequential Circuits using QDGFET perform better than the reported circuits in the literature.**

**Keywords: Quantum Dot Gate Field Effect Transistor (QDGFET), Ternary D – Flip Flop, Ternary Right Shift Register, Multi Valued Logic (MVL)**

## I. INTRODUCTION

The present digital logic exploits binary logic for computation. Digital equipment designed based on binary logic systems have the advantages of being low cost, consuming less power and are easy to implement. But currently, designs with binary logic have reached saturation [1]. Hence systems having radix more than 2 (i. e. binary system) known as Multi-valued logic (MVL) system come into the picture. The main advantage of MVL systems are that more number of information can be passed over channels and interconnection problems on the chip can be reduced [1].

The importance of MVL has been noted by many researchers [2]. Using Complementary Metal Oxide Semiconductor (CMOS) technology, implementation of MVL has two main types: current-mode and voltage-mode. There are advantages of current-mode circuits but the disadvantage of high power consumption due to the constant current flow. The advantage of voltage-mode for MVL circuits is low power dissipation but more complex fabrication process is essential to produce enhancement and depletion devices having multiple threshold voltages. Because of less interconnection, simple electronic circuit implementation methods and cost estimation, ternary logic is more attractive than other types of MVL.

In Quantum Dot Gate Field Effect Transistor, quantum dots are present on top of the gate region which produces an intermediate level between two levels. This generation of state can be explained by the resonant tunneling of charge carriers from the inversion channel to the quantum dots on top of the gate region [2]. The quantum dots are cladded on the gate region which results in very small charge leakage for this device, giving stability to the intermediate state generation between its LOW and HIGH states. Another advantage of QDGFET is that it can be fabricated using existing process.

Quantum dot layers and gate insulator thickness which are present on the top of gate governs the threshold voltage of QDGFET. QDGFET is different from SET which suffers from background charge problem. The main circuit element used in this work is a QDGFET which generates 3 levels in its transfer characteristics as given in [2]. Ternary logic circuits can be designed using QDGFET in the same way as they are with CMOS reducing design complexity to develop the ternary circuits.

Based on the design, a ternary system has significant advantages such as a decrease in the inter-connections demanded in the implementation of logic circuits reducing chip area, lower memory requirement and higher data throughput.

The simplest and most common memory element used in today's world is the binary D - Flip Flop and we want same popularity in the case of ternary D - Flip Flips in near future. For these circuits, the logical levels are logic 0 (0V), logic 1 (2.5V) and logic 2 (5V). The analysis is carried out with a simulation of the circuits using T-SPICE.

The paper is described as below: Section II contains the detail of Ternary D - Flip Flop with binary clock spikes. Section III contains the detail application of ternary D - Flip Flop with binary clock spikes - Ternary Right Shift Register. Section IV contains results and discussion of the proposed circuits. Section IV concluded the paper with some remarks and future works.

## II. TERNARY D - FLIP FLOP

Ternary D - Flip Flops using QDGFET are used instead of binary D - Flip Flops in a digital system. The well known operation of the binary D flip-flop and logic diagram can be easily found in the literature. The ternary D - Flip Flops are produced by replacing the binary NOT gates with simple standard ternary inverters (STI) and the binary NAND gates with ternary NAND gates. The basic logic gates of ternary logic are presented in [1]. The truth tables and output waveforms for both the ternary NAND and ternary STI are shown in Table I, Fig. 1 and Table II, Fig. 2 respectively.

For ternary D - Flip Flop using QDGFET, the information is in ternary form, low logic (0V), intermediate logic (2.5V) and high logic (5V) and the clock (CLK) used is in binary spikes form. The low and high logic levels are represented by 0 logic (0V) and 2 logic (5V) respectively.

TABLE I Truth Table for Ternary Nand with Two Inputs

| INPUT A | INPUT B | OUTPUT |
|---|---|---|
| 0 | 0 | 2 |
| 0 | 1 | 2 |
| 0 | 2 | 2 |
| 1 | 0 | 2 |
| 1 | 1 | 1 |
| 1 | 2 | 1 |
| 2 | 0 | 2 |
| 2 | 1 | 1 |
| 2 | 2 | 0 |

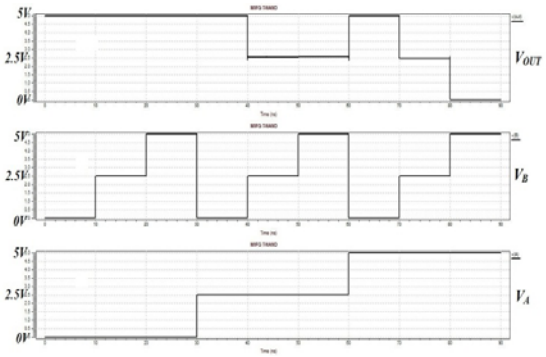


Fig. 1 Ternary NAND Gate Input-Output Waveforms

TABLE II Truth Table of Ternary STI

| INPUT | OUTPUT |
|---|---|
| 0 | 2 |
| 1 | 1 |
| 2 | 0 |

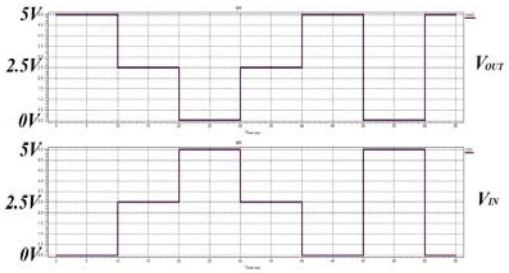


Fig. 2 STI Input-Output Waveforms

The ternary D – Flip Flop with binary CLK spike pulse can transfer the information when

the CLK spike pulse goes from low to high (i. e. positive edge). The circuit is formed by substituting the binary gates of the binary D - Flip Flop with ternary NANDs and the binary NOT gates with STI as shown in the Fig. 3. The input to ternary D - Flip Flop are Data and CLK, whereas the outputs are Q and $\bar{Q}$. The CLK signal is in binary spikes form and the logic levels are denoted by 0V and 5V. The truth table of the ternary D - Flip Flop triggered on rising edge of the binary spike CLK is shown in Table III and the simulation results are presented in Fig. 4.

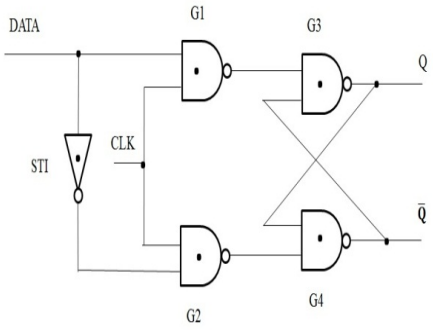


Fig. 3 Ternary D – Flip Flop

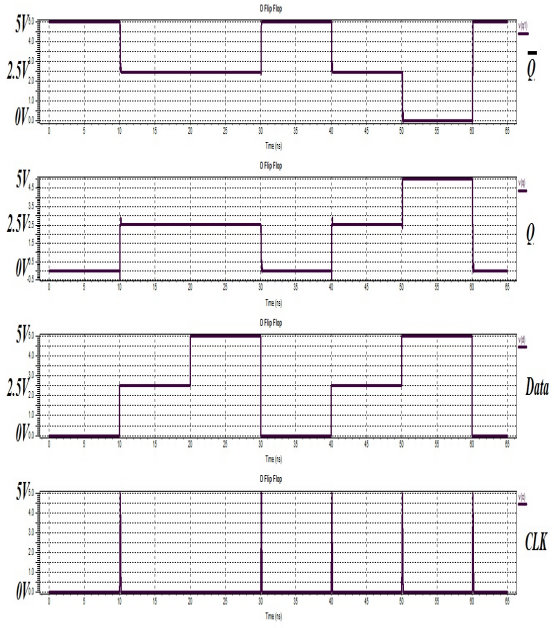


Fig. 4 Input and Output Waveform of a Ternary D – Flip Flop Using QDGFET

TABLE III Truth Table of Ternary D – FLIP FLOP

| CLK | D | Q | $\bar{Q}$ |
|---|---|---|---|
| 0 | × | No Change (Previous State) | |
| 0 - 2 | 0 | 0 | 2 |
| 0 - 2 | 1 | 1 | 1 |
| 0 - 2 | 2 | 2 | 0 |

The performance parameters of Ternary D – Flip Flop using QDGFET are shown in Table IV. Table shows the critical delays for Ternary D – Flip Flop from Input to Q and from Input to $\bar{Q}$ are 70.864 psec and 75.57 psec respectively.

TABLE IV Performance Parameters of Ternary D – FLIP FLOP

| Delay (psec) | | Average Power Dissipated (μW) | Power Delay Product (PDP) (J) |
|---|---|---|---|
| Input to Q | Input to $\bar{Q}$ | | |
| 70.864 | 75.57 | 22.24 | $1.57601\times10^{-15}$ |

The power dissipation is maximum when the input is 2.5 because the current is at its peak value here. The average power dissipated in Ternary D – Flip Flop is 22.24 μW which is lesser when compared with reported circuits in the literature. The Power Delay Product (PDP) for Ternary D – Flip Flop is $1.57601\times10^{-15}$ J.

TABLE V Input and Output Capacitance of Ternary D – FLIP FLOP

| Input Capacitance (fF) | Output Capacitance (fF) | |
|---|---|---|
| | across Q | across $\bar{Q}$ |
| 660.83 | 279.77 | 276.24 |

The input capacitance of Ternary D – Flip Flop is found out to be 660.83 fF whereas the output capacitance is 279.77 fF and 276.24 fF across Q and $\bar{Q}$ respectively.

## III. APPLICATION OF TERNARY D - FLIP FLOP – RIGHT SHIFT REGISTER

One of the applications of Ternary D – Flip flop is Ternary Right Shift Register. The Ternary Right Shift Register is formed by changing the binary D - Flip Flops with ternary D – Flip Flops,

as shown in the Fig. 5. The inputs to Ternary Right Shift Register are Data and CLK, whereas the outputs are Q and $\bar{Q}$. The CLK signal is in binary spikes form and the logic levels are denoted by 0V and 5V.

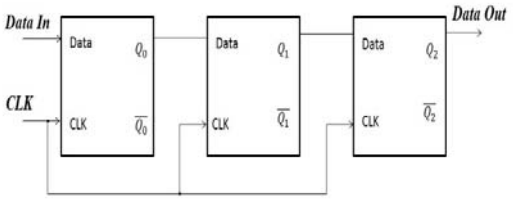


Fig. 5 Ternary Right Shift Register Using QDGFET Based on Ternary D-Flip Flop

The working of this Ternary Right Shift Register is described in the subsequent paragraph. Right shift register with binary clocks and right shift register with ternary clocks can be designed based on the type of clock signal.

Initially, all outputs of Flip Flops are reset (made 0s). On the first rising edge of the CLK, the first D – flip flop transfers the input data (5V) to the input of the second D – flip flop whereas the output of other D – flip flops will be in their previous state. On the second positive edge of the CLK spike pulse, the first D – Flip Flop transfer the input data (2.5V) to the input of the second D – Flip Flop which transfers previous data (5V) to the input of third D – Flip Flop whereas the output of the third D- Flip Flop will be 0V. For the third positive edge of the CLK spike pulse the first D – Flip Flop transfer the input data 0V to the input of the second D – flip flop which transfer previous data (i.e. 2.5V) to the input of third D – flip flop and finally the output of the third D- flip flop become 5V. In this way, each Flip Flop transfers the input data towards its output on the successive positive edge of the clock spike signal. This is verified using truth table as shown in Table IV. Thus input data is transferred to the output serially on successive rising CLK spike pulses.

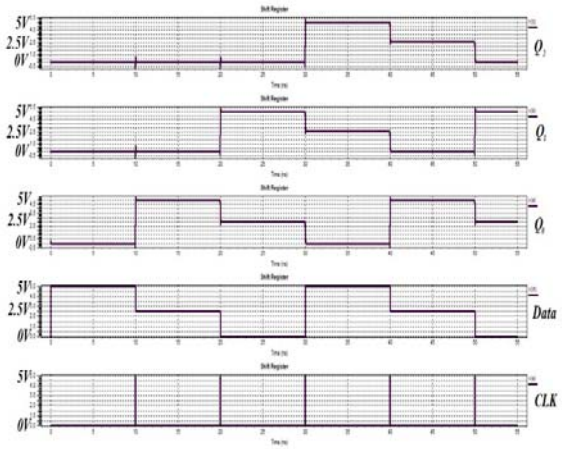


Fig. 6 Input and Output Waveform of a Ternary Right Shift Register Using QDGFET Based on Ternary D – Flip Flop

This aforementioned Ternary Right Shift Register is designed and implemented in the T - SPICE software using QDGFET device. The truth table of the Ternary Right Shift Register is shown in Table VI and the simulation results are presented in Fig. 6.

TABLE VI Truth Table for Ternary Right Shift Register

| CLOCK | DATA | $Q_0$ | $Q_1$ | $Q_2$ |
|---|---|---|---|---|
| Initially | 5 | 0 | 0 | 0 |
| 0 – 5 | 2.5 | 5 | 0 | 0 |
| 0 – 5 | 0 | 2.5 | 5 | 0 |
| 0 – 5 | 5 | 0 | 2.5 | 5 |
| 0 – 5 | 2.5 | 5 | 0 | 2.5 |

The performance characteristics of Ternary Right Shift Register using QDGFET are shown in table VII. Table VII shows the critical delays for Ternary Right Shift Register from Inputs to $Q_0$, $Q_1$, and $Q_2$ are 28.14 psec, 28.52 psec and 28.55 psec respectively. Thus total delay across Input and output is 28.55 psec. The average power dissipated in Ternary Right Shift Register is 15.17468 µW which is lesser when compared with other devices. The Power Delay Product (PDP) for Ternary Right Shift Register is $4.3324\times10^{-16}$ J.

TABLE VII Performance Parameters of Ternary Right Shift Register

| Delay (psec) | | | Average Power Dissipated (μW) | Power Delay Product (PDP) (J) |
|---|---|---|---|---|
| Input to $Q_0$ | Input to $Q_1$ | Input to $Q_2$ | | |
| 28.14 | 28.52 | 28.55 | 15.17468 | $4.3324\times10^{-16}$ |

TABLE VIII Input and Output Capacitance of Ternary Right Shift Register

| Input Capacitance (fF) | Output Capacitance across $Q_2$ (fF) |
|---|---|
| 219.55 | 84.256 |

The input capacitance of Ternary Right Shift Register is found out to be 219.55 fF whereas the output capacitance is 84.256 fF across $Q_2$.

## IV. RESULT AND DISCUSSION

Here, the comparison for sequential circuits is done in terms of number of MOSFETs required. The comparison is done for the circuits of ternary D – flip flop and ternary 3 – bit right shift register. The circuits used to design a ternary sequential circuit are same as given in previous work. But the circuit with QDGFET was found to be operating with a lesser number of MOSFETs. The comparison done in the form of a number of MOSFETs required is as follows.

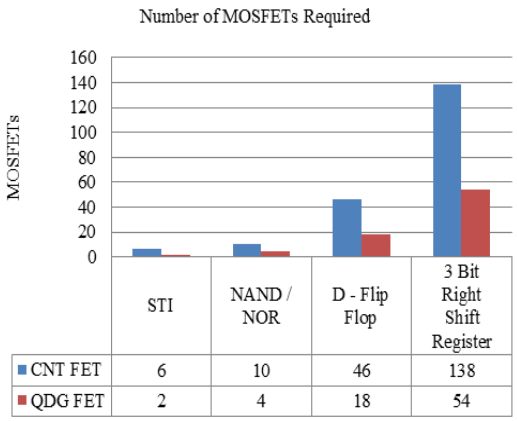


Fig. 7 Comparison Chart for Number of MOSFETs required

Thus the number of MOSFETs required for each universal gate based on QDGFETs are reduced by 60% and the number of MOSFETs required for designing ternary D – flip flop and ternary 3 – bit right shift register using ternary D – flip flop based on QDGFETs are reduced by 60.86%.

## V. CONCLUSION

This paper presents the design of Ternary D - Flip Flop, implemented with QDGFET, triggered on rising edges of a binary clock. The logic diagram, the truth table and the simulation results of the same are validated. For the Ternary D - Flip Flop using QDGFET with binary spike clock, the replacement of the binary logic gates with the corresponding ternary ones is sufficient to obtain the correct operation.

Ternary Right Shift Register, which is an application of Ternary D - Flip Flop using QDGFET with binary spike clock, is demonstrated here. The logic diagram, truth table and the simulation results of the Ternary Right Shift Register are corroborated. The simulation results validate the proposed solution to obtain the Ternary D - Flip Flop and Ternary Right Shift Register using Ternary D - Flip Flop with triggered edges control. The designed Ternary Sequential Circuits using QDGFET successfully achieves less propagation delay, low power consumption, and low Power delay product in the circuits such as Ternary D - Flip Flop and Ternary Right Shift Register using QDGFET.

Future work can be aimed at obtaining other types of ternary Flip Flops with triggered edges control (such as SR, JK, MS and T), Ternary Registers and Ternary Counters.

## REFERENCES

[1] Supriya Karmakar: Novel Three-state Quantum Dot Gate Field Effect Transistor, Springer India 2014.

[2] Supriya Karmakar, John A. Chandy, and Faquir C. Jain, “Design of Ternary Logic Combinational Circuits Based on Quantum Dot Gate FETs,” IEEE Transactions On Very Large Scale Integration (VLSI) Systems, vol. 21, no. 5, May 2013.

[3] Shah Jay and Satish Narkhede, “Design of Ternary Arithmetic Circuits Using QDGFET,” International Journal of Research in Computer and Communication Technology, vol. 4, issue 4, Apr. 2015.

[4] A. Heung and H. T. Mouftah, “Depletion/enhancement CMOS for a low

power family of three-valued logic circuits," IEEE Journal of Solid State Circuits, vol. SC-20, pp. 609-615, Apr. 1985.

[5] I. M. Thoidis, D. Soudris, J. M. Fernandez, and A. Thanailakis, "The circuit design of multiple-valued logic voltage-mode adders," Proc. Of ISCAS, pp. IV-162-165, May 2001.

[6] H. M. H. Babu, M. R. Islam, A. A. Ali, and M. M. S. Akon "A technique for logic design of voltage-mode pass transistor based multivalued multiple-output logic circuits," Proc. of ISMVL, pp. 111-116, May 2003.

[7] X. Wu and F. Prosser, "CMOS ternary logic circuits," IEEE Proceedings, 137-G, pp. 21–27, Feb. 1990.

[8] J. M. Philippe, S. Pillement, and O. Sentieys, "A low-power and high speed quaternary interconnection link using efficient converters," Proc. of ISCAS, pp. IV-689–692, May 2005.

[9] S. L. Hurst, "Multiple-valued logic –its status and its future," IEEE Trans. on Computers, C-33, pp. 1160–1179, Dec. 1984.

[10] F. Prosser, X. Wu, and X. Chen, "CMOS ternary flip-flops and their applications," IEEE Proceedings, vol. 135-E, pp. 266-272, Sept. 1988.

[11] F. C. Jain, E. Heller, S. Karmakar, and J. Chandy, "Device and circuit modeling using novel 3-state quantum dot gate FETs," Proc. Int. Semicond. Device Res. Symp., pp. 1–2, Dec. 2007.

[12] J. A. Chandy and F. C. Jain, "Multiple valued logic using 3-state quantum dot gate FETs," Proc. 38th Int. Symp. Multiple Valued Logic, pp. 186–190, May 2008.

[13] A. P. Dhande and V. T. Ingole, "Design of 3-valued R-S & D flip – flops Based on simple ternary gates", Transactions on Engineering, Computing and Technology, vol. 4, ISSN 1305-5313, Feb. 2005.

[14] John A. Chandy and Faquir C. Jain, "Multiple Valued Logic Using 3-State Quantum Dot Gate FETs." 38th International Symposium on Multiple Valued Logic, 2008.

[15] Sheng Lin, Yong-Bin Kim and Fabrizio Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits", IEEE Trans. Nanotechnology, vol. 10, no. 2, Mar. 2011.

[16] J. T. Butler and H. G. Kerkhoff, "Multiple-valued CCD circuits," IEEE Comput., vol. 21, no. 4, pp. 28–42, Apr. 1988.

[17] M. Davio and J. P. Deschamps, "Synthesis of discrete functions using $I^2L$ technology," IEEE Trans. Comput., vol. C-19, no. 9, pp. 653–661, Sep. 1981.

[18] P. C. Balla and A. Antoniou, "Low power dissipation MOS ternary logic family," IEEE Jour. Solid-State Circuits, vol. 19, no. 5, pp. 739–749, Oct. 1984.