AN AREA EFFICIENT NETWORK ON CHIP ARCHITECTURE FOR CLASSICAL AND NETWORK BASED METHODOLOGIES

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Abstract

The increasing complexity of modern digital devices demands for ever increasing communication requirements, and for an ever increasing heterogeneity of the target applications. Network-on-Chip (NoC) architectures represent a promising design paradigm to cope with increasing communi-cation requirements in heterogeneous digital systems. Classical design approaches, such as bus-based systems or point-to-point connections, are no longer suitable for highly integrated systems since they lack of flexibility and scalability with the increasing number of modules attached to the system. Nevertheless, NoC-based interconnects require additional design efforts and, in general, major resource requirements as compared to classical bus-based systems. Such an issue can be solved by directly optimizing over the different design factors. Integration of NoC (Network on Chip) architecture with Classical Bus based systems can be employed to overcome the disadvantages of both Classical and Network based methodologies. The efficiency of the proposed methodology is shown by comparing with existing methodology, taking directly into consideration the resource requirements of the target FPGA device.

Keywords: Network on Chip, Field Programmable Gate Array, Communication, System on Chip.

INTRODUCTION

When a technology matures, it leads to a paradigm shift in chip scope in LSI, VLSI and ULSI, the sequence of technologies leads to the enabling of SoC designs. In ULSI systems, a chip constitutes an entire system (hence the term System-on-Chip). SoC opens up the feasibility of a wide range of applications making use of massive parallel processing and tightly interdependent processes, some adhering to real-time requirements, bringing into focus new complex aspects of the underlying communication structure. Layered communication abstraction models and decoupling of computation and communication are relevant issues. There are, however, a number of basic differences between on- and off-chip communications. These generally reflect the difference in the cost ratio between wiring and processing resources [2].

Historically, computation has been expensive and communication cheap. With scaling microchip technologies, this changed. Computation is becoming ever cheaper, while communication encounters fundamental physical limitations such as time-of-flight of electrical signals, power use in driving long wires/cables, etc. In comparison with off-chip, on-chip communication is significantly cheaper. There is room for lots of wires on a chip. Thus the shift to single-chip systems has relaxed system communication problems. However on-chip wires do not scale in the same manner as transistors do and as we shall see in the following, the cost gap between computation and communication is widening. Meanwhile the differences between on- and off-chip wires make the direct scaling down of traditional multicomputer networks suboptimal for on-chip use.

CLASSICAL BUS BASED APPROACHES

1.2.1.1 Point-to-point interconnect

Simplicity is the major advantage of point–to-point interconnect the most significant drawback is that, the number of wire required grows rapidly as the number of channels increases by which the routing complexity is increased [9],[10].Moreover a point-to-point scheme also suffers from low wire utilization for low band width channels and a high hardware over head as dedicated interface for each channels are required [3].

1.2.1.2 Interconnect bus architectures

The most relevant efforts to realize bus-based systems for reconfigurable architectures are BUS-COM and Reconfigurable Multiple Bus-on-Chip (RMBoC) [2],[1]. Bus architecture significantly reduces the total length of wires required and also reduces hardware area necessary for interfaces, communication and control. Shared bus architectures suffer from power and performance scalability limitations.

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NETWORK ON CHIP

The NoC architecture can overcome the long wire disadvantages from bus architectures, as on-chip switches are connected in a regular topology with point-to-point basis. Long wires can be eliminated from the architecture [8], [6]. Also, the architecture is decoupled into transaction and physical layers. Thus the layered architecture enables independent optimization on both sides. With the Giga Transistor Chip era close at hand, the solution space of intra-chip communication is far from trivial.

NoC concept presents a possible unification of solutions for Electrical wires, System synchronization and design productivity. But in this Internal network contention may cause latency. Bus-oriented IPs needs smart wrappers. Software needs clean synchronization in multiprocessor systems. System designers need re-education for new concepts.

PROBLEM FORMULATION

Purpose of the present work is the integration of different bus-based systems with NoC-based approaches. From above discussion performances can be higher in NoC-based systems, but the simplicity and the presence of standards make bus-based systems more "usable".

In this context, the proposed solution is driven by the effective requirements of interoperability of different communication domains; as a matter of fact, the increasing capabilities of modern digital devices makes it possible to integrate a huge amount of computational modules within a single chip; this allows the definition of complex systems, in which there may exist multiple independent sub-systems, and it may be the case that these systems have to cooperate or at least exchange data information. This scenario is shown in figure in which two different bus-based subsystems represent independent communication domains, in which different tasks can be performed. The shared NoC can make them communicate, in a transparent and flexible way. The inter-domain communication is provided by means of the Network-on-Chip protocol, and access to it is easily provided by the network interfaces (they are seen as IP-Cores on the bus).

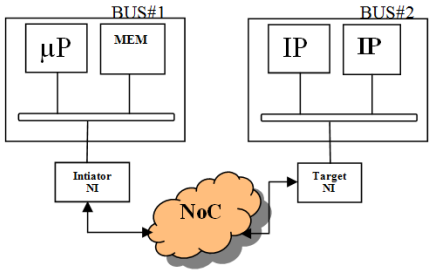
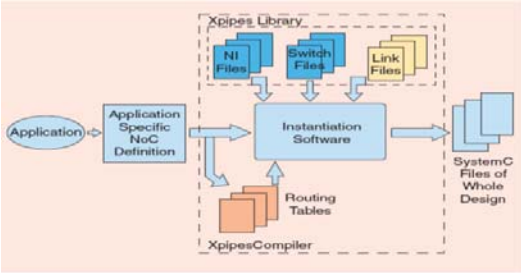


Fig:1 The integration of the NoC architecture with classical bus-based systems.

NETWORK-BASED APPROACHES

The implicit limitations previously described are overcome by the Network-on-Chip paradigm. The NoC approach is meant to interconnect subsystems in a multi-processors environment. However, they have also been applied in Systems-on-Chips (SoCs) architectures, as the connection scheme for different computational modules. The idea is to define a set of network elements, the switches, whose systematic interconnection implement the desired connectivity. To exploit full advantage of a scalable and flexible solution, packet-switching mechanism is used. Using a set of distributed elements ensures an implicit load balancing, resulting in a major level of flexibility, and a lower level of contention of the shared medium.

XPipes [5] is one of the first implementation of a Network-on-Chip approach, whose topology has to be defined at synthesis-time by enabling appropriate inter-switches communication links. The chosen topology impacts entirely on the run-time performances of interconnects, But this is certainly an undesired feature since communication requirements cannot always be known in advance.



Xpipes limitation has been solved in CoNoChi [4] (Configurable Network-on-Chip). Aim of CoNoChi is to support dynamic changes in the communication topology, adding (or removing) new (or existing) IP-Cores.

Comparisons b/w Classical and Network based designs

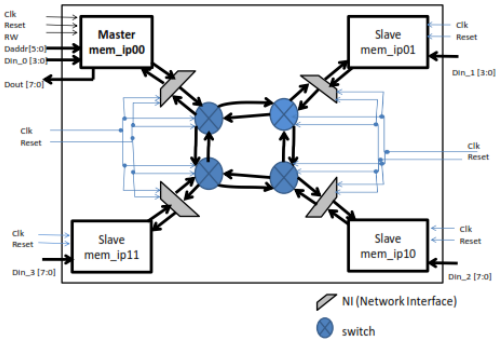
Type	Classical Design BASED	Network BASED
Parallelism achieved	Low	High
Connectivity	High	Depends on technology
Resource requirements	Low/medium	Depends on switch implementation
Flexibility	Low	High
Scalability	Low	High
Reusability	Medium	Depends on switch design
Reliability	Low	High
Contention resolution	Centralized	Distributed

DESIGN ARCHITECTURE OF NOC

In the present work initially a Master-slave will be designed using NoC architecture and in the next step for the same design the proposed architecture is used in the design and then compares the obtained results.

MASTER SLAVE DESIGN USING A NoC ARCHITECTURE

A Master Slave is designed using NoC Architecture.

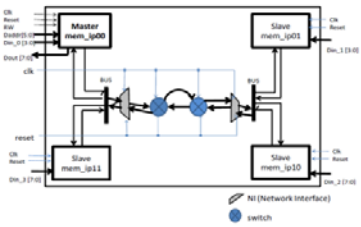


Top level block diagram of NoC Architecture

Design entities used for the designs is given below

1. Master ,2. Slave , 3. Network Interface (NI), 4.Switch

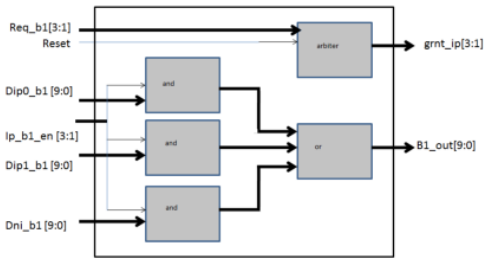
INTERGRATION OF NoC WITH BUS BASED ARCHITECTURE



The design components used and the operation of the proposed Architecture is same with NoC approach as discussed in above section, but differs in the Communication Architecture with the introduction of the OPB (On-chip Peripheral Bus).Because of OPB every internal block (except switches) gets additional signals namely **Grant** and **Request** which controls the output between blocks.

On-Chip Peripheral Bus

OPB[7] is the bus used to interconnect the cores in point-to-point approach it's block diagram and internal diagram is shown in Fig4.9.a and Fig4.9 b .Whenever cores want to send data through the OPB first it will send request to arbiter then according to arbiter grant the cores will send the data and enable signal to the OPB.



Internal Block of OPB

According to enable signal OPB will send data to output bus the same output bus is connected to all cores which linked with this OPB. According to core/ip addresses the data will receive by the cores.

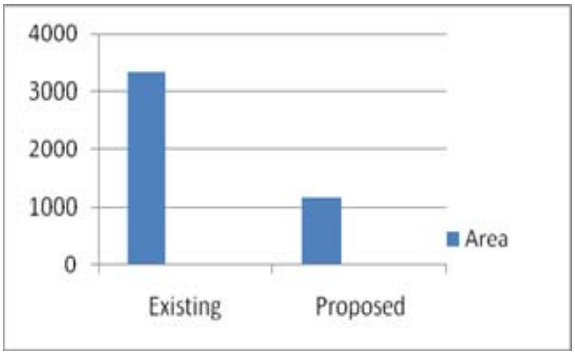
RESULTS

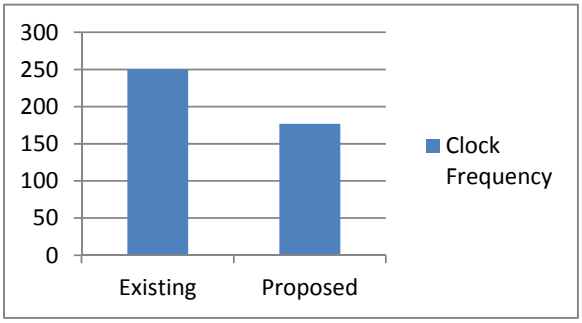
This chapter presents the Simulation and Synthesis results for the NoC and Integrated NoC with Bus architectures.

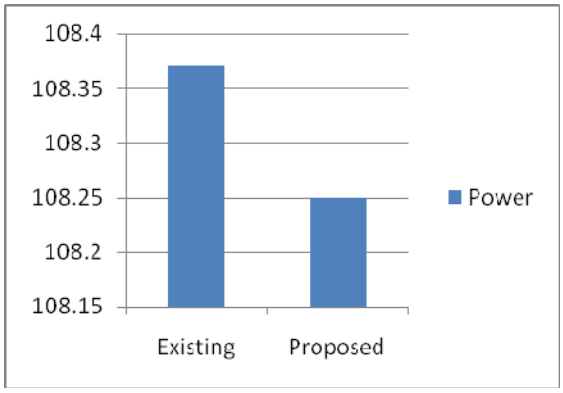
For Synthesis Cyclone III **is** used and implemented in the targeted device EP3C40F780C6

SYNTHESIS REPORT

Architecture	Area Occupied (Logical Elements)	Power Dissipation (mW)	Clock Frequency (Mhz)
Existing	3319	108.37	250
Proposed	1163	108.25	176.85







From the above table, it is clear that the proposed system is area, power and speed efficiency when compared to that of existing NoC. The reason for this efficiency is that in the Existing NoC we need four switch to implement a function and switch is a device which occupies more area when compared to the nodes. In the proposed system we have used On Chip Peripheral Bus instead of two switches. In our Bus based NoC we have used only two switches and OPB. Since OPB occupies very less area of 40 logical elements. But a Single seperate switch occupies an area of 687 logical elements. Because of the usuage of the OPB the speed of the system has increased drastically. Speed of the system is measeured by the clock frequency of the system. With proposed system we can reduce the area by 35% and increase the speed of the system by 70%.

CONCLUSION

The proposed integrated NoC with Bus based architecture is implemented on the target device EP3C40F780C6which shows that it is efficient in area as well as speed of the system when compared to the existing NoC System.

FUTURE WORK

Integrated NoC with bus based architecture can be used for designing an (re)configuration controller which can be useful in dynamic changing environment ,where the real communication requirements cannot be know in advance ,before the real application execution.

Modification can be done in the above architecture for the reduction in power dissipation.

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