A GATING SCAN CELL ARCHITECTURE FOR TEST POWER REDUCTION IN VLSI CIRCUITS

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Abstract

Testing of low power in very large scale integrated (VLSI) circuits has recently become an area of concern due to yield and reliability problems. This paper mainly focuses on reducing the power consumption during testing of the VLSI design circuits. So Power consumption in test becomes a higher barrier for VLSI to design combinational circuit, during test mode as in its normal mode of functioning seriously affects the chip reliability. There are many techniques are introduced to reduce the test power. Usually the power dissipation is due to the sequential and combinational elements presents in the circuit. In this paper proposed different methodologies and they are at cell level optimization to reduce test power.

Gating techniques are proposed to reduce the power in combinational circuits.

This paper propose a novel scan cell architecture for low power scan based technique with powerefficiency that provides combined solution for reducing total average power in both combinational part and scan cell. The proposed scan cell reduces the number of transitions during shift and capture mode. The proposed method is implemented with different combinational circuits and the experimental results were observed. Simulation results have shown that the proposed gating scan cell save 20-25% total average power in shift and capture mode as compared to conventional scan cell.

Keywords: Power consumption, Low power testing, Gating technique, combinational circuits, VLSI.

I Introduction:

With the advance in semiconductor manufacturing technology, a ***very-largescale-integration*** (VLSI) device can now contain tens to hundreds of millions of transistors. Because this trend is predicted to continue at least for the next 10 years per Moore's law [Moore 1965], severe challenges are imposed on tools and methodologies used to design and test complex VLSI circuits. Addressing these design and test challenges in an efficient way is now becoming increasingly difficult [SIA 2005]. The main motivation for considering power consumption during test is that generally, a circuit consumes much more power in test mode than in normal mode, there are several reasons that could explain this increase in **test power**. First, modern automatic test pattern generation (ATPG) tools tend to generate test patterns with a high toggle rate in order to reduce pattern count and thus test application time. Thus, the node switching activity of the device in test mode is often several times higher than that in normal mode. Second, parallel testing (e.g., testing a few memories in parallel) is often used to reduce test application time, particularly for ***system-onchip*** (SOC) devices. Third, the DFT circuitry inserted in the circuit to alleviate test issues is often idle during normal operation but may be intensively used in test mode. This surplus of active elements during test again induces an increase of power dissipation. Finally, this elevated test power can come from the lack of correlation between consecutive test patterns, while the correlation between successive functional input vectors applied to a given circuit during normal operation is generally very high [1]. In order to reduce this increased power consumption

during test application, the industry generally resorts to *ad hoc* solutions.

The solutions are:

- Over-sizing power and ground rails to allow higher current densities in the circuit under test. This allows additional power to be supplied to the circuit to satisfy the increase in switching activity that occurs during test. However, this solution raises several problems & may not be satisfactory in all cases.
- Testing with a reduced operating frequency. This solution does not require additional hardware, but it increases the test application time and may lead to a loss of defect coverage as timing-related faults may escape detection. In effect, this solution reduces power consumption at the expense of longer test time, and does not reduce the total energy consumed during test.
- Partitioning of the circuit under test with appropriate test planning. This solution, although effective from a power reduction point of view, increases test time because it reduces test concurrency. Moreover, it generally requires circuit design modifications (often with additional multiplexers), thus impacting final product cost and circuit performance.

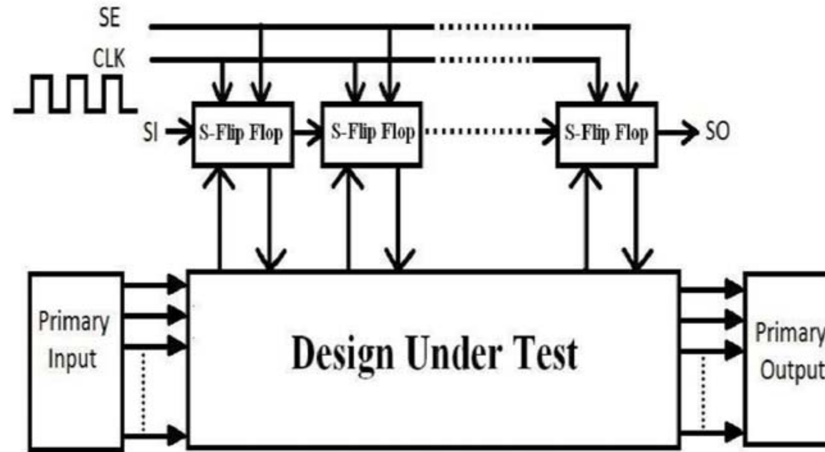


Figure. 1. Generic Architecture of Scan Testing.

However, from power dissipation point of view, Generic Architecture of Scan Testing Fig. 1, for low power designs are little very expensive due to each SCAN pattern contribution to a shift operation with high power consumption [2].

II Power Estimation in VLSI Circuits:

Regardless of short-circuit power which is consumed due to the short-circuit current flows between the supply voltage and ground during the slice time when all of the gate inputs are active, dynamic power is consumed during the charging and discharging of the output and internal nodes capacitance, which can be given by Equation (1):

$$P_{dyn} = P_{dyno} + P_{dynj} = \frac{1}{2} f(V_{DD}^2 \sum_i (\alpha_i \cdot C_{Li}) + V_{DD} \sum_i \sum_j (\alpha_{ij} \cdot C_{ij} \cdot V_{ij})) \quad (1)$$

Where, Pdyno and Pdyno correspond to the dynamic power consumption at the output load capacitance and the internal nodes capacitance, respectively. The switching activity at gate i output and that at the jth internal node of the ith gate are represented by _i and _ij, respectively. Vij corresponds to the voltage swing which is generally equal to VDD-Vth. Finally, CLi and Cij are used for gate i load capacitance and the jth internal capacitance at gate i. The average power consumption is the total energy consumption divided by the test time. This parameter is even more important than the energy as hot spots and reliability problems may be caused by constantly high power consumption. The average power consumed during the test session is presented by Equation (2), where T is the clock period and L is the total number of clocks during the test phase [5].

$$P_{average} = E_{total} / (L \cdot T) \quad (2)$$

The peak power consumption corresponds to the highest amount of power consumption during one clock cycle. If the peak power exceeds the circuit power threshold for several clock cycles, the correct function of the entire circuit is no longer guaranteed. Peak power can be expressed as follows [5]:

$$P_{peak} = \text{Max}\ P_{inst}(V_k) = \text{Max}_k\ (E_{vk}/t_{small}) \quad (3)$$

where, Pinst(Vk) (instantaneous power) determines the amount of power consumed during a small instant of time tsmall after the application of the test vector Vk. Evk corresponds to the energy consumed in the circuit after application of successive input vectors (Vk1,Vk).

III Hardware-Based Test Power Reduction Approaches:

A significant number of techniques that attempt to reduce power in the combinational part or scan chain during the test application time fall into the category of hardware-based approaches. The hardwarebased approaches require additional hardware to be added into the design, and are easy to be integrated with different embedded compression techniques [6]. Clock gating is one of the well-known power reduction techniques in the wide range of hardware-based methods [7–11].The methods proposed in [7,8] offer an algorithm for constructing an activity-sensitive clock tree that combines nodes with the same activity pattern to disconnect the clock signal efficiently. However, Shen et al. [9] have shown that merging nodes only based on the identical activity pattern may result in more transitions of the control signal. Thus, this offsets the power savings obtained by clock gating. The approach in [10] divides the scan chain into two partitions (odd and even scan cells) and uses two separate clocks for each partition. At any time instant, only one partition is active so that the peak and average power during the scan period is reduced by a factor of two. The major disadvantage of this approach is that by increasing the scan cells derived by each clock control signal, the elevated delay may make it difficult to meet the timing closure. A partial clock gating algorithm has been proposed in [11]. Since generally only a portion of scan cells participate in response capturing, a gated clock controller selectively gates the inactive scan cells during the response capture cycle. However, the power saving has been limited only to the response capture cycle at the cost of a high complexity clock gating controller. The clock skew problem in the normal mode of operation is the main disadvantage of the clock gating technique. In addition, a high complexity clock controller circuit turns out to be another drawback for this category of hardware-based approaches. Another approach known as scan partitioning splits the scan chain into multiple partitions and activates only one partition at any time interval [3, 12]. The partitioning scheme limits the scan chain transitions from propagating to combinational logic during shifting by activating only one scan path at any time interval. One of the most straight-forward methods for shift power reduction is to reduce switching activity in the combinational logic by isolating the stimulus path of scan cells from combinational logic during the shift cycle, since the major source of dynamic power in CUT is the propagation of ripple transitions from the scan cells to the combinational logic during scan shifting. These methods are less intrusive to the original designs compared with the aforementioned approaches, and they are independent of the test set. As shown in Figure 2, it bypasses the slave latch with an alternative low cost dynamic latch in the scan shifting path.

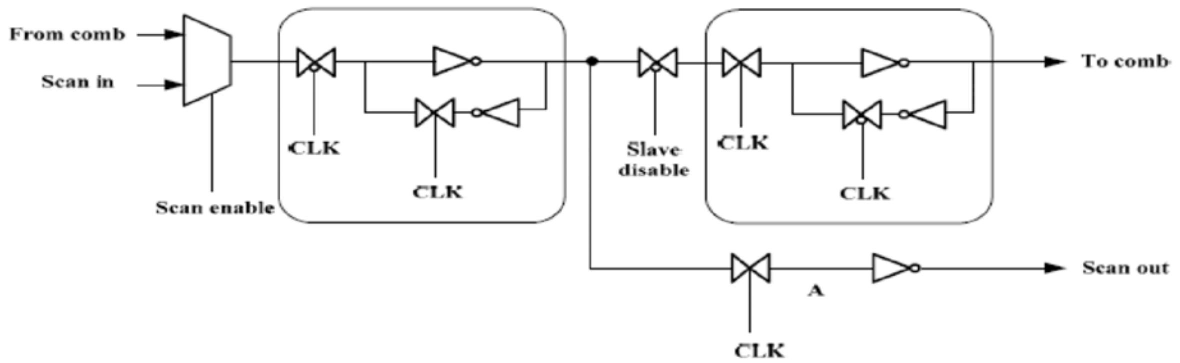


Figure 2. Modified scan flip-flop for low power delay fault testing [35].

IV Low Power Gating Scan Cell:

During the shift cycle, the rippling transitions cause great switching activities in the scan chain. The propagation of this switching activity into the combinational part contributes to large redundant transitions in the circuit lines. In order to suppress the scan chain transitions from propagating during shift cycles, we have proposed a low power gating scan cell which contains a modified slave latch augmented by a gating logic. For constructing the gating logic, we have utilized a transmission gate and an inverter to gate the scan output to the combinational logic as illustrated in Figure 2a. It uses the transmission gate to cut off the connection between the inverted scan cell output Q and the output Q of the scan cells during shift mode. As a result, the switching activities on the Q during shift mode does not affect the scan cell output Q which is used for driving the combinational logic. High resistance offered by an inactive transmission gate reduces the leakage current in the transmission gate during shift mode and the response capture cycle since the transmission gate is idling in these intervals. In addition, the transmission gate is a strong driver that feeds the gating logic inverter and pseudo primary inputs during normal/capture mode. Figure.3 depicts the proposed low power gating scan cell and the data propagation paths during shift and normal/capture modes of operation, respectively

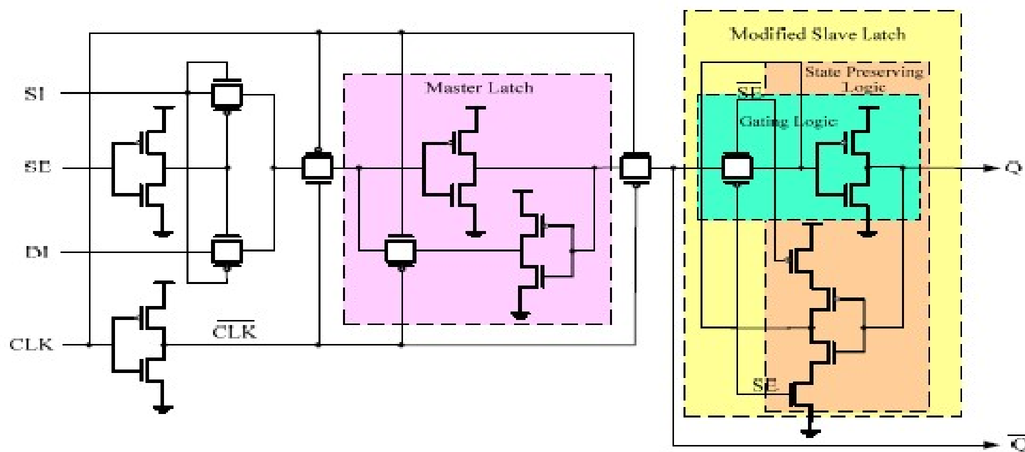
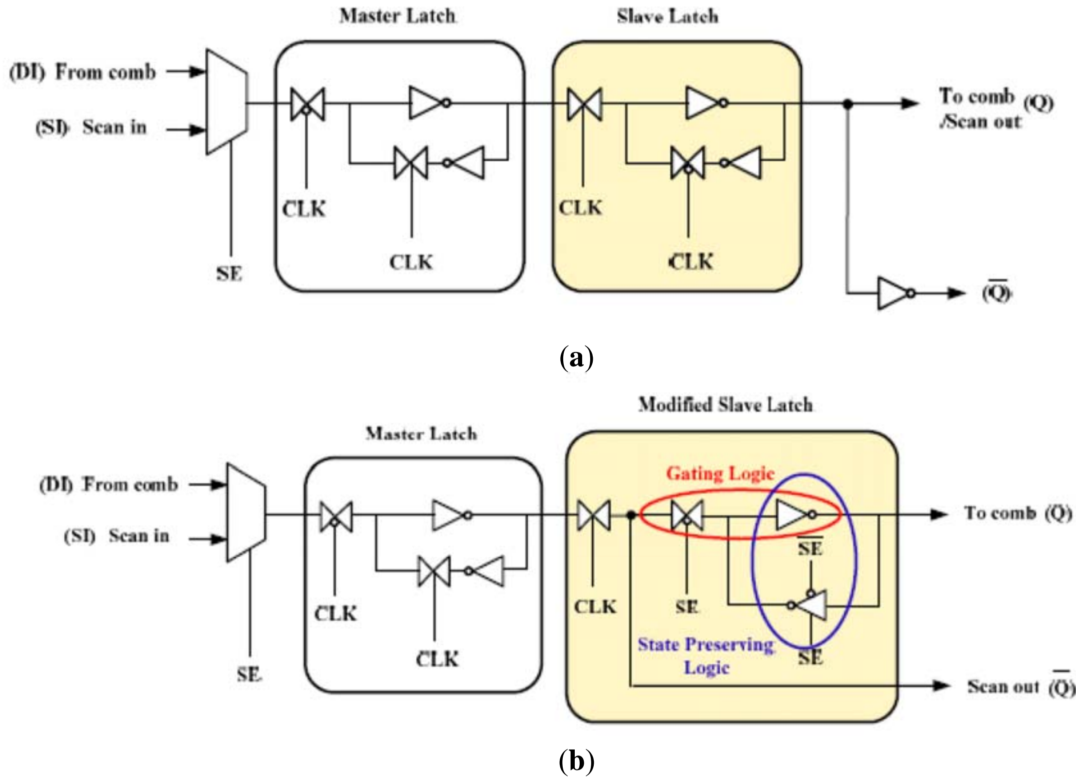


Figure 3. Proposed low power gating scan cell with gating and state preserving logic

In order to totally prevent the unnecessary transitions to the combinational logic during shift mode, a state preserving logic has been proposed. It is a feedback structure that refreshes the scan output Q with the previous logic state. The two pull-up and pull-down sleep transistors are active during shift mode which cause the state preserving logic to fix the scan output logic to the same previous logic. However, unlike gating logic, this

section is transparent in the normal/capture mode of operation since the sleep transistors are inactive. During this mode, the state preserving logic consumes low leakage power since the two sleep transistors cut off the power rail. The two pull-up and pull-down transistors also contribute to active leakage reduction due to the stacking effect [4,5]. These can alleviate the effect of state preserving on peak power during normal/capture mode. The transmission gate, pull-up, and pull-down sleep transistors are driven by the shift enable signal SE so no extra *SE* so no extra control signal is required. Sharing the pull-up and pull-down transistors of the state preserving logic among all the scan cells can alleviate the scan chain According to above discussion, in order to present a valid comparison regarding the capture peak power, it is necessary to consider every possible scenario in each scan cell at the beginning of each capture mode. Here are the possible scenarios that can happen in each scan cell during capture mode. (**a**)



(**a**)

(**b**)

Figure 4. Gate level implementation of (a) Conventional scan cell; (b) Proposed low power gating scan cell.

Conventional Scan Cell It causes both feedback inverters in the conventional slave latch to switch. In addition, there are two transmission gates in the conventional slave latch controlled by the clock that contribute to capture switching as the capture clock rises. Therefore, the total numbers of switching transistors in the conventional slave latch is eight (8) transistors[10].

4.1.2. Proposed Low Power Scan Cell:

In this case, the number of switching transistors in the modified slave latch vary depending on the time that the shift enable (SE) signal toggles from "1" to "0":The shift enable (SE) signal falls simultaneously with the capture rising clock, and then the total number of switching transistors in the modified slave latch will be six (6) transistors, including two transmission gates and two feedback inverters. Note that the inverter in the refresh feedback does not contribute in switching activity as the two sleep transistors disconnect it from the power supply and ground during the capture mode of operation. The shift enable (SE) signal falls before the capture rising clock, and then the total number of switching transistors in the modified slave latch will be four (4) transistors, including the transmission gate that is controlled by the clock and inverter in the scan cell functional path. Note that since the shift enable signal has

already switched from "1" to "0" earlier, the inverter in the refresh feedback as well as the transmission gate controlled by the shift enable (SE) signal likely do not contribute in toggling in this capture scenario, as the former is disconnected from the power supply and the latter merely behaves as a connected switch. Considering the worst case scenario for the conventional scan cell and both possible worst case scenarios for the proposed gating scan cell, it can be seen that the proposed scan cell is able to reduce the peak power compared to the conventional scan cell. This is because the proposed low power gating scan cell compared with the conventional scan cell causes less number of transistors to switch simultaneously inside the scan cell during the application of test vectors (capture mode)[1]. To the best of our knowledge, there is no gating scan cell found in the literature that is able to reduce the capture peak power over the conventional scan cell. The proposed low power gating scan cell works as a flip-flop because the inserted state preserving logic together with the gating logic function as a modified slave latch which has power reduction roles. Due to the shift path with less complexity, the scan cell speed has been accelerated during shifting which consequently alleviate the setup time violations. However, like other scan cells, the hold time violation concerns still exist. The reduced area and propagation delay due to the removal of two inverters and a transmission gate in the scan structure can moderate the area and delay overhead imposed by the augmented gating logic and also the state preserving logic. Since the shift path in the proposed scan cell has been established through the Q output of scan cell, adaptive test patterns can be used instead of original ones.

The adaptive scan process has been summarized in Figure 4.

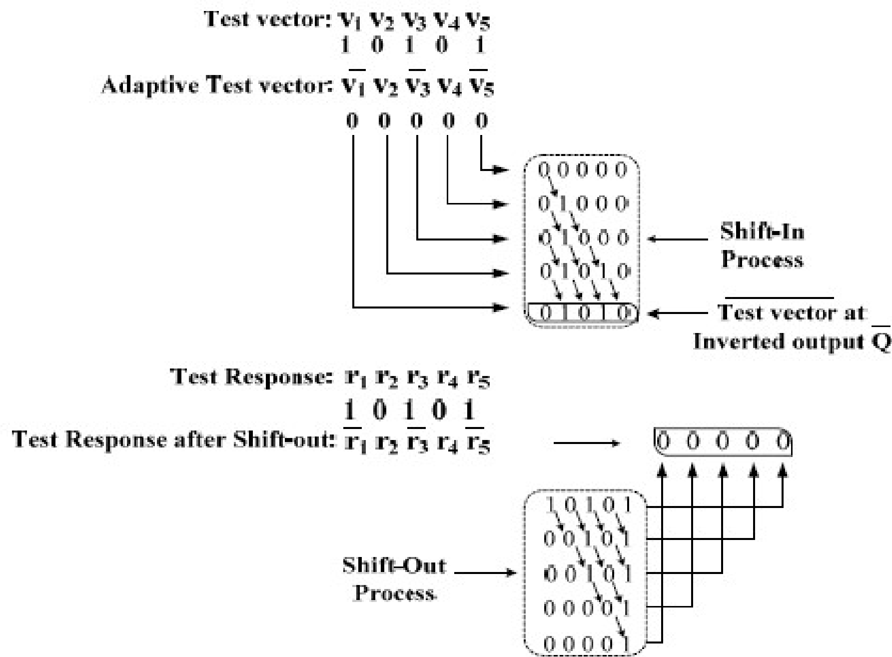


Figure 5. Adaptive scan process.

Results and Comparisons:

The low power gating scan cell has been implemented through conducting a full-custom layout design incorporating the Synopsys Custom Designer and Laker. Figure 5 shows the full-custom layout design for the proposed gating scan cell. Next, in order to verify the proposed scan cell, a set of post-layout simulations has been carried out on the parasitic included spice netlist using HSPICE in Synopsys 32/28 nm CMOS technology with the supply voltage of 1.05 Volt and clock frequency 250 MHz at room temperature. The simulation results were then compared to the conventional scan cell and the modified scan cell presented in [4] in terms of power, propagation delay, power-delay-product (PDP), and area overhead. The power consumption and propagation delay were observed by applying randomly generated waveforms

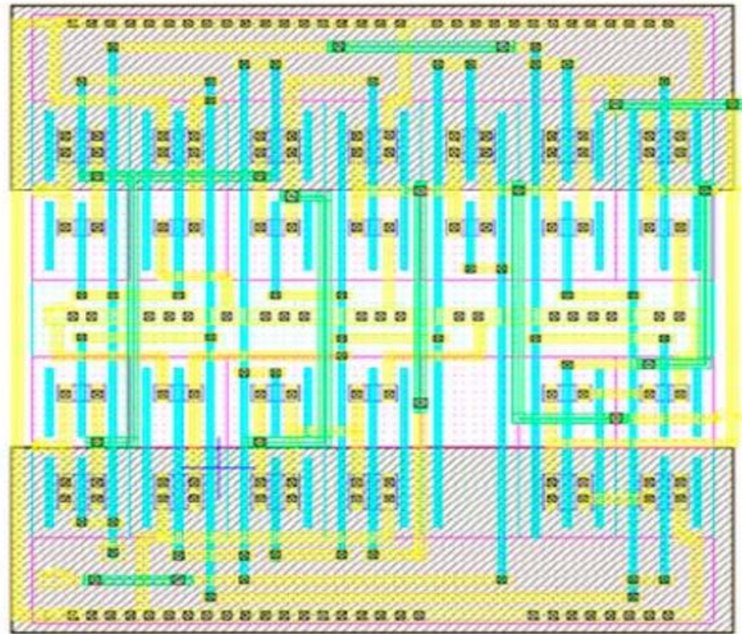
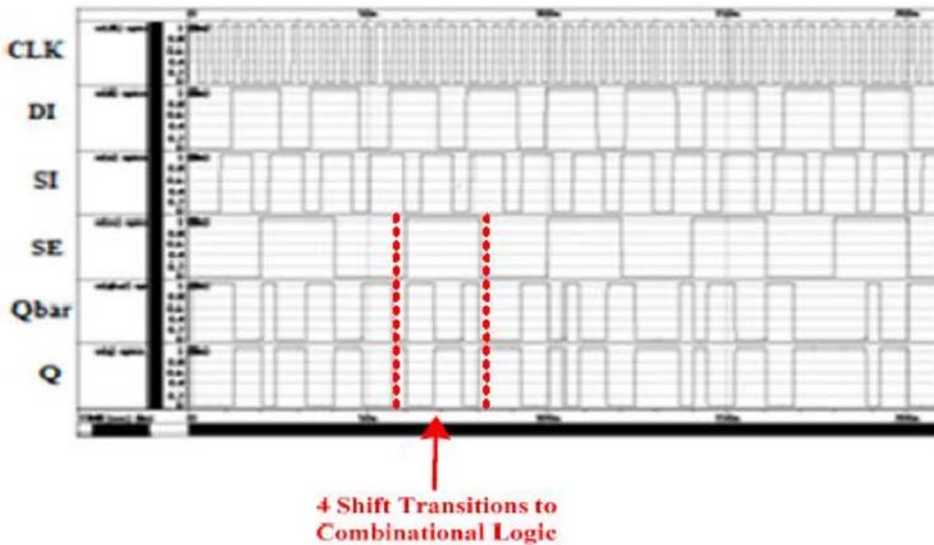


Figure 6. Full-custom layout design for the proposed low power gating scan cell in 32/28 nm CMOS Technology using Laker.

The simulated output waveform of each scan cell to the combinational logic has been shown for the conventional scan cell, proposed gating scan cell, and modified scan cell in Figure 6. It is clearly seen that unlike the conventional scan cell, the proposed gating scan cell and the modified scan cell have no transitions in the combinational logic during the shift session, as the scan cell output “Qnew_Comb” remains the same while the shift enable (SE) is high. Note that, “Qnew_Comb” is the scan cell output connecting to the combinational part.



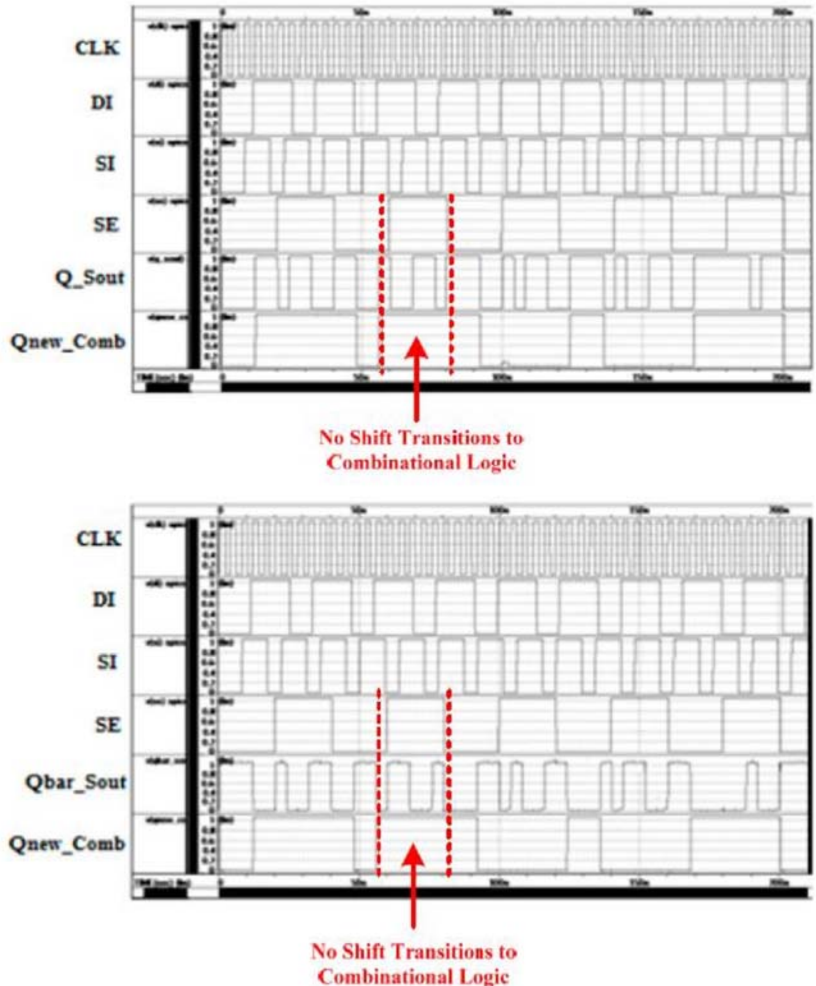


Figure 7. Post-layout simulated output waveform of (a) Conventional Scan Cell; (b) Modified Scan Cell [34]; and (c) Proposed Gating Scan Cell at 250 MHz clock frequency.

Table 1. Comparison of the total power consumption during shift and normal/capture mode.

	Conventional Scan Cell	Proposed Low Power Gating Scan Cell		Modified Scan Cell	
	Power Con. (W)	Power Con. (W)	% Imp.	Power Con. (W)	% Imp.
Ave. Total Power	7.6622×10^{-7}	7.1095×10^{-7}	**7.21**	9.7289×10^{-7}	**−26.97**

Table 2 shows the improvement of power consumption for our proposed scan cell and the modified scan cell over the conventional scan cell in four successive shift cycles. The proposed scan cell outperforms both the conventional scan cell and modified scan cell in all shift cycles. This is because it exploits a shorter shift path with less complexity compared to the other mentioned scan cells

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Table 2. Comparison of the average power consumption during Shift mode.

	Conventional Scan Cell	Proposed Low Power Gating Scan Cell		Modified Scan Cell	
	Power Con. (W)	Power Con. (W)	% Imp.	Power Con. (W)	% Imp.
Shift Cycle #1	8.9381×10^{-7}	7.4193×10^{-7}	16.99	1.0064×10^{-6}	−12.59
Shift Cycle #2	7.4784×10^{-7}	6.6012×10^{-7}	11.72	8.7580×10^{-7}	−17.11
Shift Cycle #3	7.5832×10^{-7}	6.7539×10^{-7}	10.93	1.0704×10^{-6}	−41.15
Shift Cycle #4	7.6638×10^{-7}	6.6542×10^{-7}	13.17	8.9380×10^{-7}	−16.62
Average	7.9158×10^{-7}	6.8571×10^{-7}	**13.37**	9.6160×10^{-7}	**−21.48**

Table 3 shows the percentage of shift power improvements for each benchmark circuit using the proposed low power gating scan cell over the conventional scan cell to form their scan chain.

Table 3. Percentage of shift power improvements for the proposed low power gating scan cell over the Conventional scan cell

	Scan Chain with Conventional Scan Cell		Scan Chain with Proposed Low Power Gating Scan Cell			
	Dynamic Power (W)	Peak Power (W)	Dynamic Power (W)	% Imp.	Peak Power (W)	% Imp.
b14	1.17×10^{-5}	0.4174	4.59×10^{-6}	60.7%	0.1445	65.4%
b15	1.03×10^{-5}	1.4332	5.57×10^{-6}	46.1%	0.2173	84.8%
b18	1.69×10^{-5}	1.8324	7.40×10^{-6}	56.2%	0.3287	82.1%
b21	2.10×10^{-5}	1.5403	9.81×10^{-6}	53.34%	0.2800	81.8%
b22	3.78×10^{-5}	1.4919	1.23×10^{-5}	67.45%	0.4784	67.9%

Future Works:

To evaluate and verify the impact of the proposed low power gating scan cell on the power reduction of the whole circuit during the test (shift) mode of operation in benchmark circuits, a library characterization process will be conducted in order to develop a standard power-aware scan cell based on the proposed low power gating scan cell timing and power characteristics. The exact amount of reduction in test application time therefore will be presented according to static timing analysis (STA) reports.

Conclusion:

One of the less intrusive and effective solutions to reduce shift power significantly, independent of the test set, is scan gating techniques. However, significant delay on signal propagation paths, large area overhead, high switching activity, and finally undesired impacts on peak power all caused by gating logics, has made them less practical for large industrial circuits. Most previous works successfully reduce shift power in combinational logic only, without considering the scan chain as the main source of power consumption during the shifting phase. In this paper, we designed and implemented an area-efficient low power gating scan cell as an integrated solution for shift power reduction in both the scan chain and combinational logic. Since the gating scan cell reduces power consumption inside the scan cell compared with the conventional scan cell, the total power consumption is reduced during the shift (test) mode of operation. The proposed gating scan cell is a modified scan cell augmented by gating and state preserving logics to gate and hold the scan cells' stimulus path while maintaining peak power under a certain threshold. Choosing a new data shift path through a less complex propagation path in the proposed gating scan cell incorporates further

power reduction in the scan chain in addition to improving the critical shift timing and hence, leads to test application time reduction. Compared with the lowest cost gating techniques, the proposed gating scan cell has less DFT overhead with respect to average power, shift, and capture delay. Similar to other gating methods with state hold abilities such as the modified scan cell, the proposed low power gating architecture can be effectively employed in broadside delay fault test applications. Furthermore, it can be applied effectively to both the full gating and partial gating methods. The original fault coverage is not degraded and it does not face routing problems since no additional control signal has been employed. The proposed scheme can efficiently be utilized in both built-in-self test (BIST) and nonBIST architectures. It can also be applied together with other scan-based power optimization methods such as scan chain partitioning and reordering techniques. Low power hardware-based as well as ATPG-based methods can be applied to the proposed structure efficiently for capture average power reduction.

Therefore, these advantages make the proposed approach a potential for all scan-based DFT architectures.

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