COMPARATIVE STUDY OF DELAY & POWER DISSIPATION IN CMOS LOGIC GATES

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Abstract
This work concerns the Comparative study of CMOS Logic Gates by means of Time Delay & Power Dissipation. Dynamic CMOS logic in general and domino logic in particular has a number of advantages to design high speed and low power CMOS circuits. However, the main difficulty with domino logic is that it can implement only non-inverted logic. To implement inverted polarity it is required to duplicate several circuit parts using inverted polarities of inputs and hence increasing area and power dissipation. With static CMOS logic, on the other hand, it is simple to realize gate with both inverted and non-inverted logic unlike dynamic CMOS logic. In this paper, we propose a mixed approach, where it implements both static and dynamic CMOS logic styles in the same circuit eliminating intermediate inverter implementation of domino logic.
Keywords: **In all the categories delay and power consumption at different capacitive loads has been noted in simulation results. To measure the above two parameters the work has been done on S-Edit, L-Edit & T-Spice of EDA Tool Tanner version 12.5 and the simulation results are taken from there. Here 0.5 micron technology at +49 level of modeling used.**
The range of load capacitor which is used in the documennt is in fF, like 1fF, 2.5 fF, 10fF, 100 fF, 200 fF, 400Ff, 600fF, 800fF, 1000fF & 1500fF.

I. INTRODUCTION

In this document mainly two universal gates are considered one in which a NAND Gate and second a NOR Gate operating with different capacitive loads. Considering the above two cases further the work is divided in four categories.

In first category the work is performed on designing Static NAND Gate Schematic with different capacitive loads then prepared layout design of the static NAND Gate and studied under the same capacitive loads values as before.

In second category the work is done on Static NOR Gate Schematic with different capacitive loads then drawn layout design of the schematic of Static NORGate and studied under the same capacitive loads values as before.

In third category the work is performed on designing Domino NAND Gate Schematic with different capacitive loads then prepared layout design of the Domino NAND Gate and studied under the same capacitive loads values as before.

In fourth category the work is done on Domino NOR Gate Schematic with different capacitive loads then drawn layout design of the Domino NOR Gate and studied under the same capacitive loads values as before.

Results & Discussion:

A. Time Delay is an important design constraint in VLSI. Fig-1 shows the SPICE variation of the time delay ratio with effect of various load capacitors (CL) in two logic techniques (static & domino).
Here the blue line shows the effect of load capacitor on time delay in case of schematics of NAND gates in both techniques. In case of

schematics we see up to 10.0 Ff value of load capacitor the delay ratio is minimal which increase gradually up to 800 Ff value of load capacitor. On further increase in the value of load capacitor the delay ratio drastically increase which is not desirable

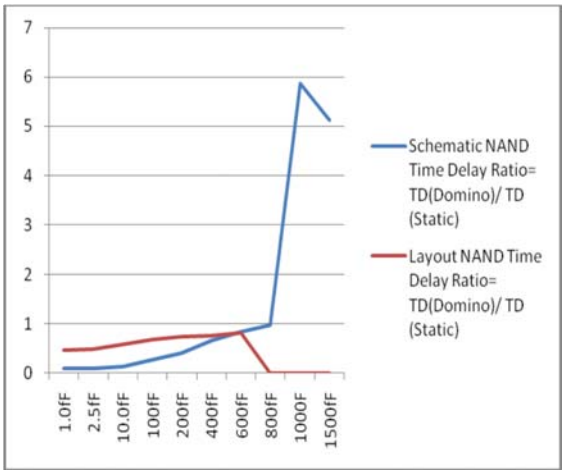

Fig.-1 Nand Gate Time Delay Ratio vs C-apacitive Load

The red curve shown in Fig.1 represented the effect of load capacitor on time delay ratio in case of the layout designs of same NAND gates in both techniques. Due to parasitic capacitors the curve is different from the schematic one but it is more realistic because layout design is more near to the actual implementation of any VLSI circuit.

When we study this curve what we see is although from 1.0Ff value of load capacitor up to600Ff value the time delay ratio is greater than the value obtained in case of schematics but after 600Ff value of load capacitor could not found which shows by
sudden fall of curve. By the curve shown in Fig.1 for NAND gate the optimal value of load capacitor is 600Ff at 3.3v supply voltage.

B. In Fig.-2 shows the SPICE variation of the time delay ratio with effect of various load capacitors (CL) in two logic techniques (static & domino). Here the two curves overlap each other which show that the effect of load capacitor in both the schematic and layout design of NOR gate is same.

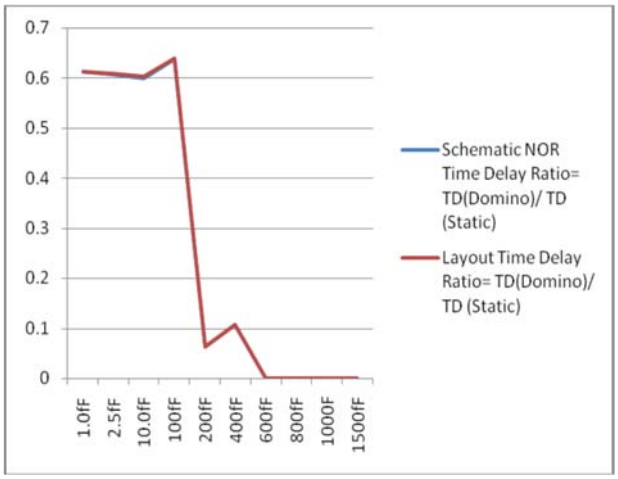

Fig.-2 NOR Gate Time Delay Ratio vs CL

On studying these curves we see that from 1.0Ff up to 10.0Ff the delay ratio slightly reduce where as from 10.0Ff up to 100Ff value of load capacitor the delay ratio increase. Beyond 100Ff value of load capacitor up to 200 Ff curve decrease drastically and shows minimum delay ratio on 200Ff capacitive load. From 200Ff up to 400Ff load capacitor delay ratio further increase but beyond 400Ff could not calculated which shown as sudden fall in curve. Optimal value of load capacitor as shown in Fig.-2 for NOR gate 200Ff at 3.3v supply voltage.

C. Power dissipation is another important design constraint in VLSI. Fig-3 shows the SPICE variation of the power dissipation ratio with effect of various load capacitors (CL) in
two logic techniques (static & domino).

Here the blue line shows that power dissipation ratio is independent of load capacitor in case of schematics of NAND gates in both techniques. The red curve shown in Fig.-3 represented the effect of load capacitor on power dissipation ratio in case of the layout designs of same NAND gates in both techniques.

Due to parasitic capacitors the curve is different from the schematic one but it is more realistic because layout design is more near to the actual implementation of any VLSI circuit. As shown in the curve the power dissipation ratio decreases on differ capacitive loads, also the power dissipation ratio is more at low load capacitor (1.0Ff & 2.5Ff) slightly decrease up to 10.0Ff.

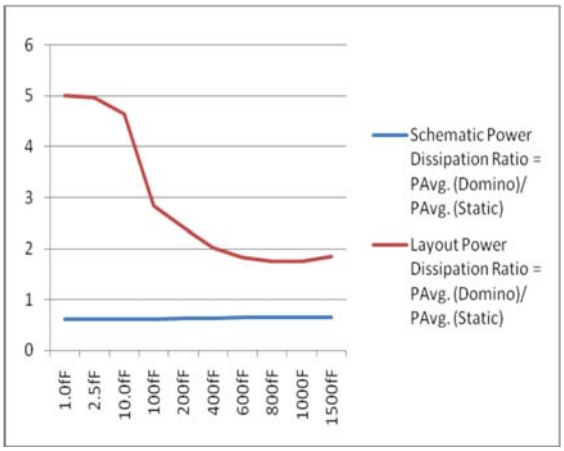

Fig. 3 NandGate: (Static & Domino) Average Power Dissipation Ratio:- PAvg.(Domino/Static) vs CL

From 10.0Ff up to 100Ff value of load capacitor the power dissipation ratio reduced drastically which decreases further on increasing the load capacitor up to 1000Ff. On going beyond 1000Ff up to 1.5Pf again power dissipation ratio starts increasing. By the curves shown in Fig.-3 for NAND gate the optimal value of load capacitor is 800Ff at 3.3v supply voltage.

D. In Fig.-4 shows the SPICE variation of the average power dissipation ratio with effect of various load capacitors (CL) in two logic techniques (static & domino).

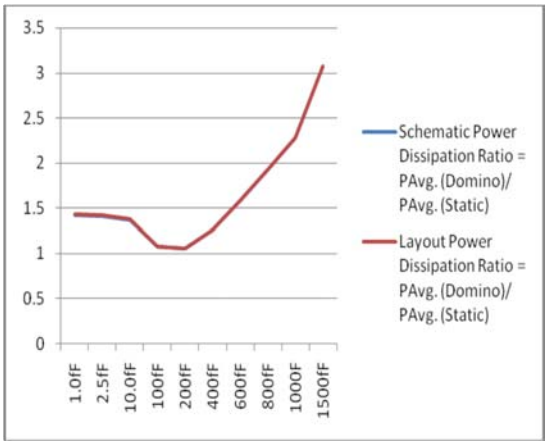

Fig.6.4 NOR Gate: (Static & Domino) Average Power Dissipation Ratio:- PAvg.(Domino/Static) vs CL

Here the two curves overlap each other which show that the effect of load capacitor in both the schematic and layout design of NOR gate is same. On studying these curves we see that 1.0Ff up to 10.0Ff average power dissipation ratio remains almost constant which decreases up to 100Ff and goes up to its minimum value on 200Ff capacitive load. Beyond 200Ff load value average power dissipation ratio starts increasing gradually up to 1000Ff and above 1000Ff up to 1.5Pf increase rapidly as shown in Fig.6.4 which is non desirable. By the curve shown in Fig.6.4 for NOR gate the optimal value of load capacitor is 200Ff at 3.3v supply voltage.

E. Fig-5 shows the SPICE variation of the power delay product ratio with effect of various load capacitors (CL) in two logic techniques (static & domino).

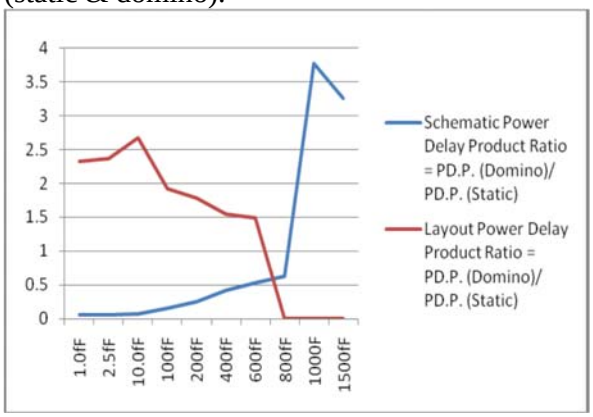

Fig.-5 Nand Gate: (Static & Domino) Power Delay Product Ratio:- P.D.P.(Domino/Static) vs CL

Here the blue line shows that power delay product ratio in schematic of NAND gate. On studying this curve we see that from the 1.0Ff value of load capacitor up to 10.0Ff a very less almost constant power delay product ratio shown which increases gradually up to 800Ff value of load capacitor and rapidly increase beyond 800Ff up to 1000Ff. On further increasing the load capacitor value up to 1.5fF the power delay product starts decreasing.

The red curve shown in Fig.-5 represented the effect of load capacitor on power Delay product ratio in case of the layout designs of same NAND gates in both techniques.

Due to parasitic capacitors the curve is different from the schematic one but it is more realistic because layout design is more near to the actual implementation of any VLSI circuit. As shown in the curve in starting from 1.0Ff to 2.5Ff slight increase observed in power delay product ratio which rapidly increases from 2.5Ff up to 10Ff load capacitor. On increasing the value of load capacitor further beyond 10Ff up to 600Ff the curve shows decrement in power delay product ratio.

After 600Ff the sudden fall of power delay product ratio curve indicate that no result found of power delay product ratio by the EDA tool for the load capacitor greater than the value of 600Ff. By the curves shown in Fig.6.5 for NAND gate the optimal value of load capacitor is 600Ff at 3.3v supply voltage.

F. In Fig.-6 shows the SPICE variation of the power delay product ratio with effect of various load capacitors (CL) in two logic techniques (static & domino). Here the two curves overlap each other which show that the effect of load capacitor in both the schematic and layout design of NOR gate is same.

On studying these curves we see that 1.0Ff up to 100.0Ff the power delay product ratio decreases. From 100Ff up to 200Ff value of load capacitor the power delay product ratio curve rapidly fall which shows the reduction in power delay product ratio. Beyond 200Ff up to 400Ff value of load capacitor power delay product ratio starts increasing after 400Ff then sudden fall of curve shows that no data could be calculated by EDA tool.

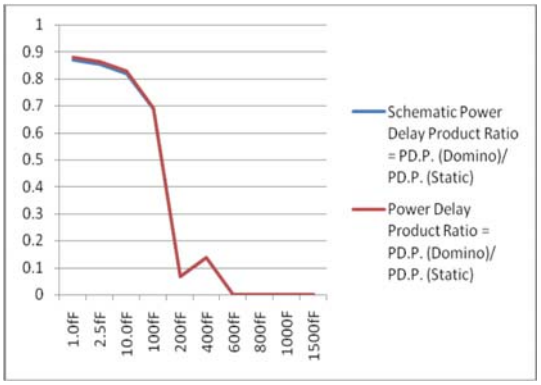

Fig-.6 NOR Gate: (Static & Domino) Power Delay Product Ratio:- P.D.P.(Domino/Static) vs CL

By the curve shown in Fig.-6 for NOR gate the optimal value of load capacitor is 200Ff at 3.3v supply voltage.

G. In Fig.-7 shows the combine SPICE variation (in schematics of static and domino NAND-logic) of the Time delay ratio, Average power dissipation ratio and power delay product ratio with effect of various load capacitors (CL) in two logic techniques (static & domino).

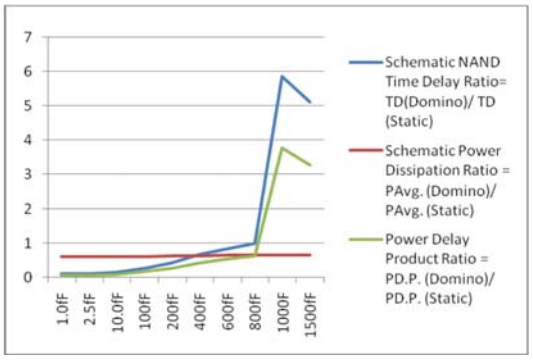

Fig.-7 Schematic Nand Gate All Ratio vs CL

Here the blue line curve shows the effect of load capacitor on time delay ratio which shows a gradual increment in time delay ratio up to 800Ff and on going beyond 800Ff rapid increase in time delay ratio has been observed which is not desirable although after 1000Ff up to 1.5Pf decrement in time delay ratio has been observed. In Fig.-7 Red line curve shows the average power dissipation is independent of load capacitor as we do not see any variant effect of load capacitor on average power dissipation.

In Fig.-7 Green line curve shows the effect of load capacitor on power delay product ratio which is like time delay ratio but less than that. That is power delay product ratio too gradually increase up to 800Ff and on going beyond 800Ff rapid increase in power delay product ratio has been observed which is not desirable although after 1000Ff up to 1.5fF decrement in power delay product ratio has been observed. By the curve shown in Fig.-7 for NAND gate Schematic the optimal value of load capacitor is 400Ff at 3.3v supply voltage.

H. In Fig.-8 shows the combine SPICE variation (in Layouts of static and domino NAND–logic) of the Time delay ratio, Average power dissipation ratio and power delay product ratio with effect of various load capacitors (CL) in two logic techniques (static & domino).

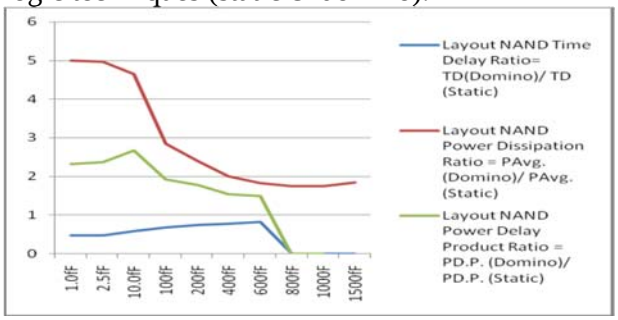

Fig.-8 Layout Nand Gate All Ratio vs CL

Due to parasitic capacitors the curve is different from the schematic one but it is more realistic because layout design is more near to the actual implementation of any VLSI circuit.

Here the blue line curve shows the effect of load capacitor on time delay ratio which shows almost constant time delay ratio from1.0Ff up to 2.5Ff and on going beyond 2.5Ff up to 600Ff value of load capacitor time delay ratio increase gradually.
Rapid fall in time delay ratio has been observed after 600Ff which shows that value could not found by EDA tool.

In Fig.-8 Red line curve shows the average power dissipation is dependent of load capacitor as we see variant effect of load capacitor on average power dissipation.

It is clear from the Fig.-8 that from 1.0Ff up to 1000Ff value of load capacitor the average power dissipation decrease and on further increasing the value of load capacitor up to 1.5fF again it starts increasing.

In Fig.-8 Green line curve shows the effect of load capacitor on power delay product ratio which increases from1.0Ff up to 10.0Ff after then decreases. That is power delay product ratio gradually increase up to 10Ff and on going beyond 10Ff decrease in power delay product ratio has been observed up to 600Ff .Rapid fall in power delay product ratio has been observed after 600Ff which shows that value could not found
by EDA tool. By the curve shown in Fig.-8 for NAND gate Layouts the optimal value of load capacitor is 600Ff at 3.3v supply voltage.

I. In Fig.-9 shows the combine SPICE variation (in schematics of static and domino NOR -logic) of the Time delay ratio, Average power dissipation ratio and power delay product ratio with effect of various load capacitors (CL) in two logic techniques (static & domino).

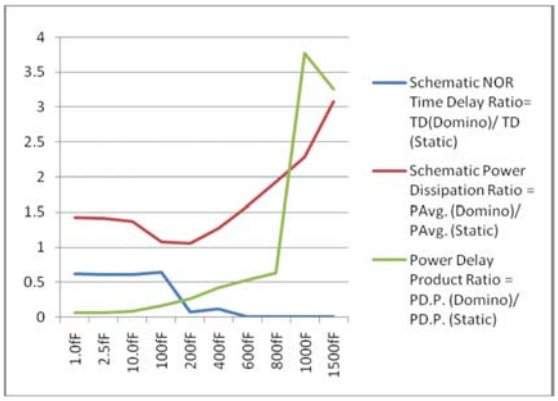

Fig.-9 Schematic NOR Gate All Ratio vs CL

Here the blue line curve shows the effect of load capacitor on time delay ratio which Shows almost constant time delay ratio from 1.0Ff up to 10.0Ff then a negligible increase from 10.0Ff up to 100Ff value of load capacitor. From 100Ff up to 200Ff time delay ratio decreased continuously and give its minimal value on 200Ff. beyond 200Ff up to 400Ff the time delay ratio increase gradually but after 400Ff sudden fall in curve shows that value could not found by the EDA tool.

In Fig.-9 Red line curve shows the average power dissipation is dependent of load capacitor as we see variant effect of load capacitor on average power dissipation. From 1.0Ff up to 10Ff value of load capacitor curve shows almost constant average
power dissipation ratio which starts decreasing from 10Ff up to 200Ff. Beyond the 200Ff load capacitor increment in average power dissipation has been observed which increased rapidly from 1000Ff up to 1.5fF.

In Fig.-9 Green line curve shows the effect of load capacitor on power delay product ratio which is almost constant from 1.0Ff up to 10Ff and increases gradually up to 800Ff.

Above 800Ff a rapid increase in power delay product has been observed up to 1000Ff. Beyond 1000Ff curve starts decreasing further. By the curves shown in Fig.-9 for NOR gate Schematics the optimal value of load capacitor is 200Ff at 3.3v supply voltage.

J. In Fig.-10 shows the combine SPICE variation (in Layouts of static and domino NOR -logic) of the Time delay ratio, Average power dissipation ratio and power delay product ratio with effect of

various load capacitors (CL) in two logic techniques (static & domino).

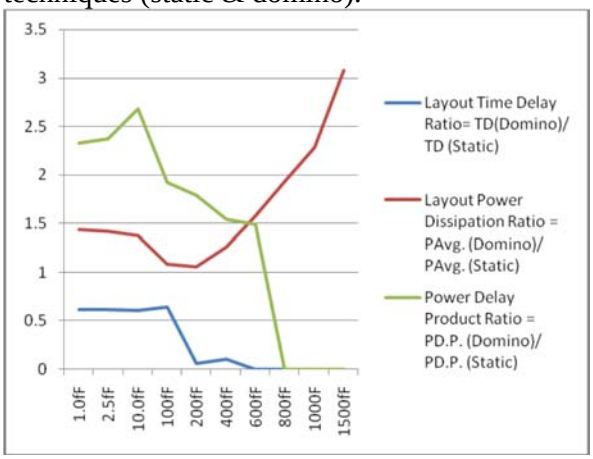

Fig.-10 Layout NOR Gate All Ratio vs CL

Here the blue line curve shows the effect of load capacitor on time delay ratio which Shows almost constant time delay ratio from 1.0Ff up to 10Ff value of load capacitor. After 10Ff up to 100Ff slight increment in time delay ratio has been observed which falls rapidly from 100Ff up to 200Ff. Beyond 200Ff up to 400Ff value of load capacitor the time delay ratio increased gradually. Beyond 400Ff sudden fall in curve shows that value could not found by the EDA tool.

In Fig.-10 Red line curve shows the average power dissipation is dependent of load capacitor as we see variant effect of load capacitor on average power dissipation.
From 1.0Ff up to 10Ff load capacitor value almost constant average power dissipation ratio seen and after 10Ff which decreases up to its minimal value on 200Ff load capacitor. Beyond 200Ff average power dissipation ratio curve shows gradual increment in it up to 1.5Pf.
In Fig.-10 Green line curve shows the effect of load capacitor on power delay product ratio which is gradually increase from 1.0Ff up to 10Ff and further decreases from 10Ff up to 600Ff.Above 600Ff a rapid fall in power delay product has been observed which indicate that value could not found by the EDA tool. By the curves shown in Fig.-10 for NOR gate Layouts the optimal value of load capacitor is 200Ff at 3.3v supply voltage.

K. Conclusion:

Performance comparison of two CMOS logics have been investigated in this document. Domino gates provide high-speed design and dissipate lower power than its static CMOS counterparts[5]. Simple models, simulation, and measurement have shown that high- speed design & substantial power savings can be attained by load capacitor optimization for circuits having short channel devices. The reasons are the
relatively larger parasitic capacitances and the channel velocity saturation effect of submicron CMOS technologies[7].
Experimental results on universal gates (NAND & NOR) in both the techniques (Static & - Domino) the simulation results of optimized load capacitor shows that for a technology
It has been observed that different values of load capacitors for different logic gates.

As in case of NAND gates (Domino v/s Static) optimized value of load capacitor observed 600fF to reduce time delay ratio, average power dissipation ratio and power delay product ratio.
On the other hand in case of NOR gates (Domino v/s Static) optimized value of load capacitor observed 200fF to reduce time delay ratio, average power dissipation ratio and power delay product ratio.
Signal nodes, which toggle several times before reaching a final steady-state condition (referred to as glitching), are relatively common in static logic, but absent in domino designs. This is because once the output of a domino cell rises, no change in the inputs to the cell will cause the output to fall. Only when the clock falls at the end of the evaluation phase will the output of the cell fall. Thus, within a clock period there is the possibility of only one rise and fall at the output of the domino cell[4].

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