FPGA IMPLEMENTATION OF COMPRESSING TECHNIQUE IN VLSI MULTIPLIERS FOR FFT ARCHITECTURES

L.Malathi, M.E.,Ph.D[1], S.Munaf, M.E.,Ph.D[2], Dr.A.Bharahi, Ph.D[3], Dr. A.N.Jayanthi, Ph.D[4]
[1,2,4]Sri Ramakrishna Institute of Technology, Department of ECE, India
[3]Bannari Amman Institute of Technology, Department of ECE, India

ABSTRACT

Compressors are used for less power consumption and high throughput. By analyses the compression techniques the fast and reduced delay were achieved. In the proposed system necessary power was reduced compared to the existing multipliers with an accurate level. The proposed system can be used in digital image processing and communication related applications where compression in multipliers is needed. Nth order compression is used in this proposed.

INDEX TERMS: Nth order compressor, Multiplier.

I. INTRODUCTION

Reduction of partial products takes much time and power in the multiplier. High order compressors provide better results in terms of power and speed. But it consumes more area than low order compressors. Many techniques were proposed to reduce the critical path in the multiplier. Multipliers, shifters and adders are mainly used to accomplish these tasks. Multipliers play a important role in Digital Signal Processors. Digital signal processors take care of convolution, correlation and filtering of digital signal. Multiplier is the most complex one. Multipliers take more time and consume higher power.

The proposed method will produce exact result. But it gives the drawback to optimize the parameters like delay, power and execution time. Of, course every applications need accurate result. Approximate techniques will consumes less power and low complexity. Video processing, Image processing and Multimedia technologies will adapt with an approximate computing and produce acceptable results.

Mostly the techniques which are proposed for multipliers will not produce cent percent accurate without truncation and rounding errors. Most of errors because of most significant bit (MSB) compared to least significant bit (LSB). Result i.e sum value is calculated normally when any one of the operand value of adder is zero. When both operands are one, sum value can be XOR-ed as one from that bit position to least significant bit (LSB).

Approximate XOR/XNOR adder for inexact computing was proposed already [15]. XOR and XNOR gates are required for the proposed system to calculate the output of the adder. Low power imprecise adder were proposed [16] where they optimized transistor count, power consumption and power delay product of the adder. Approximation methodologies were applied in generating the partial product phase [19]. An approximate multiplier is designed by altering the one output combination.

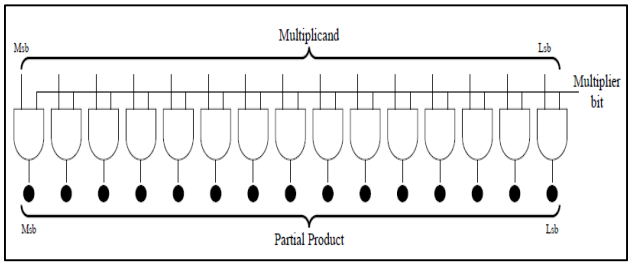

Fig. 1 Partial Product Selection Logic

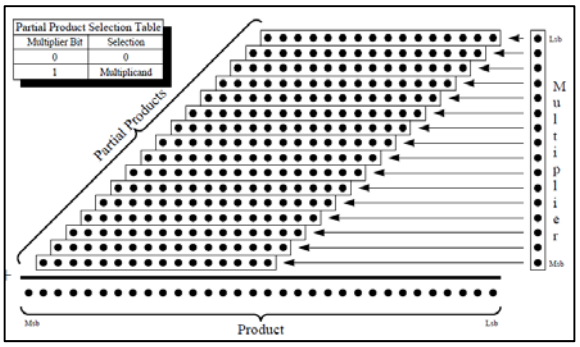

Fig. 2 Partial Product Phase

For n-bit multiplier was implemented by two n/2-bit sub-multipliers. Then, all partial products are accumulated by a Wallace tree. Accurately every techniques having error. To obtain low error and better circuit performance is a challenge always.

II. DESIGN OF COMPRESSORS

A. COMPRESSOR DESIGN WITH TWO SIGNED BITS: DESIGN 1

In full adder take three bits as input and gives out two bits, but in the proposed technique, the only difference is, it deals with negative bits. In this compressor, there can either be one or two negative bits, and accordingly we get the result. Depending on the number of the negative bits the inputs are arranged, and since the compressor deals with negative numbers one of the output.

X and Y are the negative bits and CY is the negative output bit while if there is only one negative bit then Z takes the negative input and SM gives the negative output. When X and Y are positive bits and are high bits, the resulting output is 10 where CY is positive and SM is negative. Similarly, when X and Y bits are high but both of them are negative numbers, the resulting output is 10 but here CY is negative and SM is positive.

The expression is given by,

SM = [Xo •Yo • Z] + [Xo •Y • Zo] + [X • Yo • Zo] + [X •Y • Z]

CY = [Yo • Z] +[X • Yo • Zo] + [X • Y • Z]

B. COMPRESSOR DESIGN WITH TWO SIGNED BITS: DESIGN 2

SM = [C XOR □M] • [X XOR Y] + [Z XOR M]• [X XOR Y]

CY = X •Y • [Z • M] + X • Y • [Z • M] + Y • X • [Z • M] + X • Y • [Z XOR M]

CY = Z • M • [X+Y]

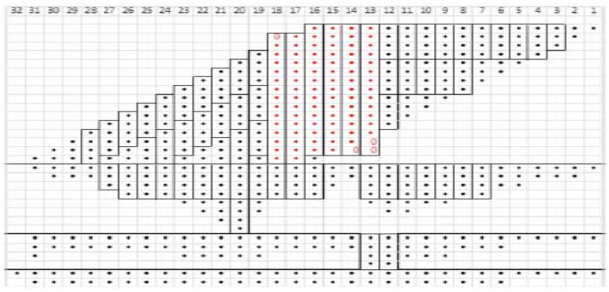

Fig.3 Compressor Design

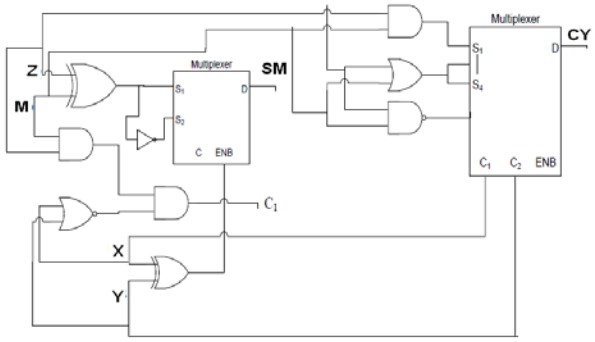

Fig. 4 Compressor Design With Two Signed Bits

C. DESIGN OF TWO'S COMPLEMENT MULTIPLIER: DESIGN 3

In two's complement number representation, the most significant bit (MSB) is weighted negatively. According to the proposed method, In full adders which is separated into four types. In type 0, which represents a normal adder, all three inputs X, Y, Z are weighted positively and the result lies in the range {0,3}. This result is represented by a two-bit binary number CY, SM where CY and SM are also weighted positively. In the other three types there are some signals, indicated by the dots,that are weighted negatively.

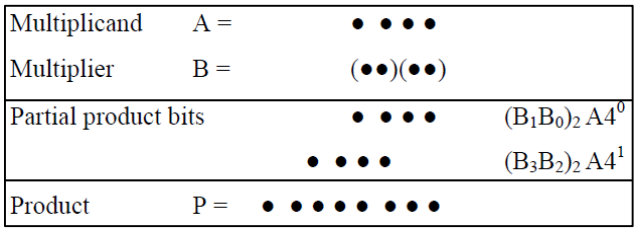

Fig.5 Radix-4 Multiplication in Dot Notation

Input / Output relationships of the four types of generalized full adders.

CY21 + SM20 = X20 + Y20 + Z20

CY21 + (-SM)20 = X20 + Y20 + (-Z)20

(-CY)21 + SM20 = (-X)20 + (-Y)20 + Z20

(-CY)21 + (-SM)20 = (-X)20 + (-Y)20 + (-Z)20

III BUTTERFLY STRUCTURE USING COMPRESSOR

All multipliers are designed by using various signed and unsigned compressors in FFT structure. The signed compressor, some conventional unsigned compressors were used in partial product reduction. Two signed bits are available because the most significant bit of multiplicand produces one signed bit and most significant bit of multiplier produces another signed bit. It is necessary to include signed compressor to add signed bit. In every multiplier, we have chosen correct combination of compressors to reduce the partial product. Signed compressors are used in the multiplier whenever is required. Compressor based multipliers provide better performance than a conventional signed multiplier in terms of speed.

$$
\begin{aligned}
X[k] &= \sum_{n=0}^{N-1} x[n]\, W_N^{kn} \\
&= \sum_{\substack{n=0 \\ n \text{ even} \\ \text{so } n = 2m}}^{N-1} x[n]\, W_N^{kn} + \sum_{\substack{n=0 \\ n \text{ odd} \\ \text{so } n = 2m+1}}^{N-1} x[n]\, W_N^{kn} \\
&= \sum_{m=0}^{N/2-1} x[2m]\, W_N^{k2m} + \sum_{m=0}^{N/2-1} x[2m+1]\, W_N^{k(2m+1)} \\
&= \sum_{m=0}^{N/2-1} s_1[m]\, W_{N/2}^{km} + W_N^k \sum_{m=0}^{N/2-1} s_2[m]\, W_{N/2}^{km} \\
&\qquad \text{by def'n of } s_1[n] \text{ and because of the recursion property } W_N^2 = W_{N/2} \\
&= S_1[k] + W_N^k\, S_2[k]
\end{aligned}
$$

$$
S_1[k] = \sum_{n=0}^{N/2-1} s_1[n]\, W_{N/2}^{kn} \quad \text{and} \quad S_2[k] = \sum_{n=0}^{N/2-1} s_2[n]\, W_{N/2}^{kn}.
$$

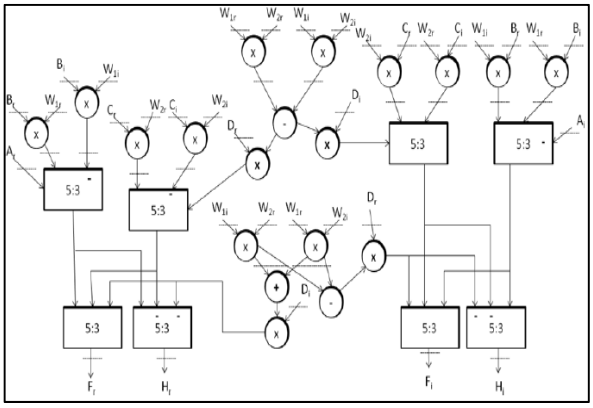

Fig.6 Approximate Modified FFT Architecture Using Compressor

For image compression energy compaction a transform that reduces the signals of interest to a small number of nonzero coefficients. Image compression is often done in blocks. Suppose if select a small block from some natural image. The DFT of the block gives us the values of the discrete Fourier series of the periodic extension of that signal. Suppose the periodic extension has a discontinuity at the block boundaries. Then the DFT coefficients will decay slowly, just like the FT of a square wave (discontinuous) decay as 1/k, whereas those of a triangle wave decay as 1/k2. So any discontinuities in an image, include at the boundary of a block, lead to poor energy compaction of the coefficients.

IV. SIMULATION RESULTS AND DISCUSSION

The function of the proposed design is verified using Xilinx software. FFT structures are described in Verilog HDL. Architectures were synthesized and the results are obtained. Power consumption of this design is considerably low because number of active cells in the critical path is lower than accurate design. The approximate compressor is high among other proposed designs.

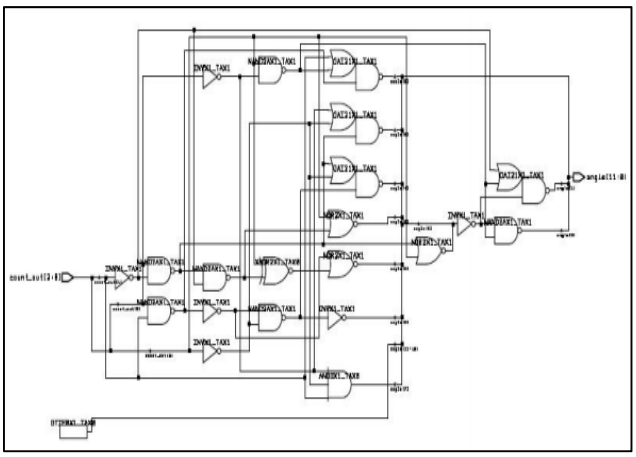

Fig.7 LUT Circuit - FFT

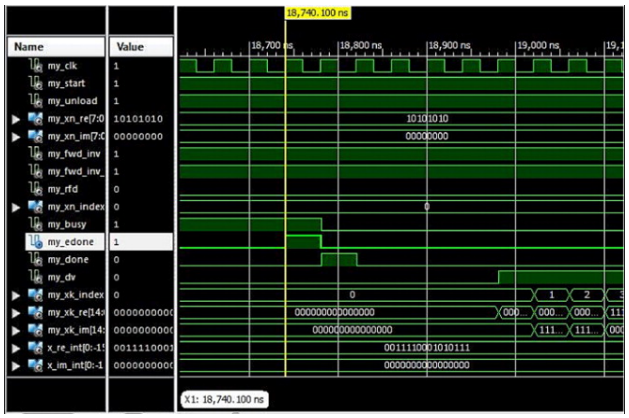

Fig.8 Simulation Result-Two Signed Bit Compressor

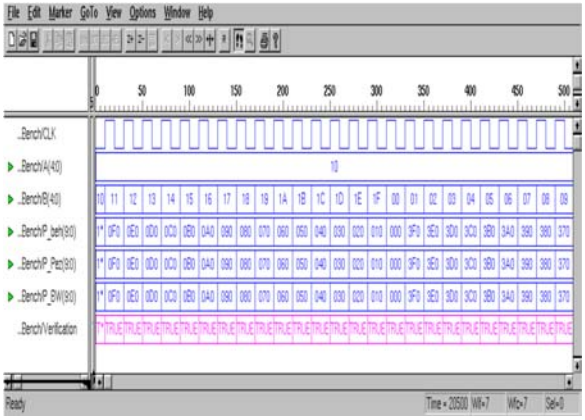

Fig.9 Simulation Result- FFT

V. CONCLUSION

This paper proposes design of compressors with two sign bit. Then signed multiplier is designed with the help of proposed compressor. The proposed design gives reduced delay, low power consumption. Proposed compressor is very small and latency of the multiplier is almost equal as compared to the accurate multipliers. A small amount of extra hardware is required, However the extra hardware requirement is significantly reduced if this method is used in conjunction with the redundant multiplication algorithm. Like the previous methods, direct computation of the low order product bits is avoided in the method. The most significant partial product, which is necessary to guarantee a positive result, is not needed for signed multiplication. All that is required is to sign extend the multiplier to fill out the bits used in selecting the most significant partial product.

ACKNOWLEDGEMENT

The authors would like to thank the authorities of Sri Ramakrishna Institute of Technology – Coimbatore for providing research support grants and environments for carrying out the research works.

REFERENCES

[1] N. Maheshwari, Z. Yang, J. Han, and F. Lombardi, ``A design approach for compressor based approximate multipliers," in Proc. 28th Int. Conf. VLSI Design (VLSID), Jan. 2015, pp. 209_214.

[2] A. Pishvaie, G. Jaberipur, A. Jahanian, " Redesigned CMOS (4; 2) compressor for fast binary multipliers", Canadian Journal of Electrical and Computer Engineering. 36(3), pp.111-115, (2013).

[3] X. Liu, F. Yu, Z.K. Wang, "A pipelined architecture for normal I/O order FFT", Journal of Zhejiang University: Science C. 12(1), pp.76-82, (2011).

[4] R. Shenda, P. Zode, P. Zode, "Efficient design 2k−1 binary to residue converter", International Conference on Devices, Circuits and Systems, Coimbatore, India, pp. 482-485, (ICDCS 2012).

[5] A. Pishvaie, G. Jaberipur, A. Jahanian, "High Performance CMOS (4:2) compressors", International journal of electronics. 101(11), pp. 1511-1525, (2014).

[6] S. Mehrabi, R. F. Mirzaee, S. Zamanzadeh, K. Navi, and O. Hashemipour, ``Design, analysis, and implementation of partial product reduction phase by using wide m:3 (4 _ m _ 10) compressors," Int. J. High Perform. Syst. Archit., vol. 4, no. 4, pp. 231_241, Jan. 2013.

[7] M.B. Fonseca, A. Eduardo, C. Costa, B. Joa˜o, S. Martins, "Design of power efficient butterflies from Radix-2 DIT FFT using adder compressors with a new XOR gate topology", Analog Integrated Circuit Signal Processing. 73(3), pp. 945–954, (2012).

[8] A. Dandapat, S. Ghosal, P. Sarkar, and D. Mukhopadhyay, ``A 1.2-ns 16 _ 16 bit binary multiplier using high speed compressor," Int. J. Elect. Electron. Eng., vol. 4, no. 3, pp. 234_239, 2010.

[9] D. Baran, M. Aktan, and V. G. Oklobdzija, ``Energy ef_cient implementation of parallel CMOS multipliers with improved compressors," in Proc. ACM/IEEE Int. Symp. Low-Power Electron. Design (ISLPED), Aug. 2010, pp. 147_152.

[10] L. Malathi, L. J. Arthiha, R. Kanmani, "FPGA Implementation for Reduced Memory using Scalable Encryption Algorithm" in International Journal for Electronics Communication and Electrical Engineers Vol.4,Issue No.2, 2013, pp-668-670

[11] L.Malathi, Dr.A.Bharahi, Dr. A.N.Jayanthi, S.Munaf, "Design of Fast Integer Pipelined Multipliers for CMOS 64-bit Synchronous and Asynchronous Logic with Adaptable Latency" in International Journal of Recent and Innovation Trends in Computing and Communication, Volume 5, Issue 1, January 2017 99 – 102

[12] S.D. Pezaris, "40- ns 17- bit by 17- bit array multiplier", IEEE Transaction on computers. 20(4), pp.442-447, (1971).
[13] O. Kwon, K. Nowka, E. Swartzlander, Jr., "A 16-Bit by 16-Bit MAC Design Using Fast 5:3 Compressor Cells", Journal of VLSI Signal Processing. 31(2), pp.77–89, (2002).
[14] M. Potkonjak, J. Rabaey, "Pipelining: Just another Transformation. Proceedings of the international conference on Application Specific Array Processors", Western USA. Berkeley, California, pp. 163 – 175, (1992).
[15] J. Cooley, J. Tukey, "An Algorithm for the Machine Calculation of Complex Fourier series", Mathematics of Computations. 19, pp. 297 – 301, (1965).
[16] M. S. K. Lau, K.-V. Ling, and Y.-C. Chu, ``Energy-aware probabilistic multiplier: Design and analysis," in Proc. Int. Conf. Compil., Archit., Synth. Embedded Syst., Oct. 2009, pp. 281_290.
[17] S.A. White, "A Simple FFT Butterfly Arithmetic Unit", IEEE Transactions on Circuits and Systems. 28 (4),pp.352-355, (1981).
[18] K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, 1st ed. Hoboken, NJ, USA: Wiley, 1999.