POWER MANAGEMENT OF LOW-POWER DESIGN_2

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Abstract

Elevated temperatures are a major contributor to lower semiconductor reliability. If heat is not removed at a rate equal to or greater than its rate of generation, junction temperatures will rise. Higher junction temperatures re-duce mean time to failure for the devices. Device reliability has a direct impact on the overall system reliability. Removing heat from these devices is thus a major task facing design engineers of modern electronic power maintenance systems concerned with improving reliability.

Understanding the effect of heat on the reliability of electronic products and the integrity of manufacturing processes is critical if problems are to be avoided. This means the need to understand power management techniques and the need for comprehensive data has never been greater. With passive cooling methods, the chip temperature is determined by the efficacy of heat transfer out of the device.

INTRODUCTION

The increasing demand for high performance, battery-operated, SoC (system —on-chips in communication and computing has shifted the focus from traditional constraints such as area, performance, cost and reliability to power consumption. Just as important, through not so obvious, is the need to power consumption for non-portable systems, such as base stations, where heat dissipation and energy consumption are critical concerns.

There are techniques that have been developed over the past decade to address the continuously aggressive power reduction requirement of most ASIC AND SoC designs. They include clock gating, multi-switching threshold transistors, multi voltage, power gating with or without state retention, dynamic voltage and frequency scaling and substrate biasing.

The use of any of these techniques comes at a and their benefit varies depending on the technique used. In shot they introduce rise to the product development schedule and impact all aspects of ASIC and SoC development, including design, implementation, and verification. Each technique used must be considered with the rest of the system requirements.

For example, designers will have to choose between power gating with or without state retention. Power gating with retention achieves faster wakeup times and preserves state information, but it requires more silicon real estate as well retention flops must be powered up when the rest of the domain gating is the most effective in reducing leakage power. However it is also the technique with the most impact to current design and verification flows and methodologies.

Power gating state retention involves switching off an area of a design when its functionality is not required then restoring power when it is. The areas created by gating are called power blocks .power gating requires the use of retention memory elements to prevent data from being lost in a specific power domain during power down. Retention strategies such as retention flops and latches save information before a power domain switching off and restore it when the power domain is turned back on. As well .Restore protocols must be used to ensure that the power domain returns to a known good state when powered up. Finally, each power domain must be isolated from the rest of. when powered down so that it does not corrupt downstream logic.

Gate level verification poses many issues such as:

Time: gate level simulation are slow.

Debug: debugging at gate level is difficult as the user defined RTL specification has been transformed into implementation through synthesis.

Problem rectification: it takes longer and requires more resources to resolve function problems uncovered at the gate level compared to RTL

For these reasons waiting to perform power aware design verification at gate level is too costly in terms of resources and design cycles.

This paper describes the basic elements of low power design verification and implementation.

Designers have developed various low power techniques to reduce leakage power consumption. These techniques make use of some of sleep operation. Placing power gating structures is a well known technique for reducing power leakage during stand mode, while maintaining high speeds in active mode. During stand by one or more portions of the circuit are switched off and the passage from the source to ground is blocked, eliminating leakage in those areas. One side effect of power gating is that data in storage elements can be lost. As a result, designers use retention memory elements to retain key state data during the sleep .Mode so that it can be restored correctly upon power up this is retention sleep mode.

some designs use a conventional sleep operation in which the power supply of the entire design is cut off when the circuit is not in use such designs do not require data in the registers/latches used in the design. Power down in book computers is an example of such asleep mode. However, even with the conventional sleep operation, function verification of the design is required to ensure that the awake portion of the design function properly while other parts are sleeping and that the system will operate correctly when power is to the sleeping logic blocks.

With retain sleep mode, the operation of a logic circuit is stopped only if that specific work is not in use. Low power devices in portable equipment use retention sleep mode during intermittent operations. These devices preserve the dead during sleep. The sequential cell are blown as retention flip flops .to implement sleep power Management techniques, will defined power management block must be created with specific power control signals and power domains.

POWER MANAGEMENT DESIGN STRUCTURE:

As the power management techniques employ turning off aid various segments of a design, these designs are divided into different power blocks, based on areas of functionality that support common operations or tasks. In other words a

RETENTION MEMORY ELEMENTS:

To maintain the state of registers and latches during sleep mode, retention elements are employed that can retain heir data when in sleep mode alternatively, voltage threshold scaling may be used for retention without requiring a bubble latch to hold the retained value. RFFs and RLAs are affected by the power signals that control the RTL region to which they belong. The registers are corrupted when the power is switched off. Corruption is typically represented by unknown. the register valve is restored after power up if the value was saved successfully before power down and the restore protocol executed successfully. Otherwise, the register value remains unknown until) it is set ,reset, or a new value latched into it. These elements will behave as normal memory elements when the power is switched on and the power control signals are not asserted. The retention flip flop is a clock low retention FF. These types of FFs have one control signal known as ret. A clock low retention FF requires that the clock be gated low during the save and restore operation and most likely during retention as well. When ret is asserted and the clock is low,the restore option is performed. They behave as normal FFs when ret is low.

MOVING LOW POWER SPECIFICATION TO THE RTL:

Power gating requires early verification. Waiting for the gate Izvel netlist is too costly for a number of reasons, rincluding slow simulation time and more difficult power domain constitutes a collection of functionality that can be turned off as a whole, and it runs at the same operating voltage level, having a single set of power control signals. Power control signals are used to control sequential retention cell, isolation cells and the switches that serve as gatekeepers to a blocks power supply.

In addition , every power aware design has at least one primary domain , which is always on. This is known as either the wake-up . debugging and problem resolution. In addition, information at the RTL to validate that low power techniques

are implemented correctly in the early as well as stages of the design flow.

POWER INFORMATION CAN INPUT AT THE RIL IN TWO WAYS:

1 .Directly specified in the RT code

2. Indirectly specified in the file.

By directly integrating the power information in RTL, the corresponding power information is packaged together with the RTL.. Most resister and latches in a RTL design are inferred and not explicitly coded as part of the HDL there is no guarantee that the retention cells will be functionally the new technology library. Similarly power control signal to retention cells and the installation of isolation cell and level shifters within the RTL code create an unnecessarily tight coupling between the design functionality and low power design intent. Finally as significant aspects of the low power design intent is related to the technology implementation, it is usually modified often than the RTL functional specification.

Therefore the two should be; specified separately to facilitate maintenance, changes and verification. For these reasons, it makes sense to provide the power specification in a file. if the low power design intent is specified separately form the RTL code, yet is related to it, then familiar RTI: coding styles can he maintained and relice of the RTL maximized. Thus a means of specifying the low power intent separately from the functionality in RTL is not only very useful but also essential. The low power specification file should provide the information required to overlay the RTL functionality with the power control network and the power aware functionality.

The power specification data provides the low power design intent. The corruption semantics are implied by that intent. Thus the power specification captures the systems power states ;enough information about the power supply network to known how the power supply is distributed and controlled for each state which registers need retention; how isolation and level shifting are handled; and how retention is performed. This information can be used to functionally verify the design at the RTL and ensure that the low power design intent is implemented in the gate level design through synthesis. Synthesis tool can the same information to create an appreciate power aware gate level netlist automatically.

LOW POWER STANDARD FORMAT:

Low power specification are need at each step of the design flow so that correct power management components can be implemented at the RTL ,correctly during synthesis and placed and routed efficiently and accurately in physical design. This requires a single power format accepted by all tools in the flow at any given abstraction level. A single power format case implementation and validation and helps meet design schedules. It must also address reusability, allow early and thorough validation and have built extensibility.

DEFINE SYSTEM POWER STATES AND THE SUPPLY NETWORK:

When designing the low power aspects of an electronic system should start by defining the system power states.. for ex. A system power states may be such that the modem is in sentinel mode, waiting for an incoming call. The information management system is checking for scheduled appointments and the rest of the system is in sleep mode to conserve power. Such a deep sleep state must be defined in terms of the functionality in the system.

The supply network consists of power switches; supply ports that are defined for power blocked and power switches, supply nets that connect supply ports and logic and propagate the supply state and the supply states. Each supply port has one or more supply states defined. The port may drive only one state at any give time. That state is propagated by the supply net connected to the port. The power state table is defined in terms of these states. The supply network to the logic elements in the design based on the semantics defined for specific of supply nets.

STATES		**micro control**	**memory**	**control**	**remark**
	sleep	**Off retain**	**0.8v**	**1.0v slow clock**	**leakage**
	Over drive	**1.3v**	**1.2v**	**0.9v slow clock**	**High perpormance**
	conserve	**1,0v slow clock**	**1.0v**	**0.9v fast clock**	**dynamic**

SPECIFYING POWER BLOCKS:

Power domains enable the automation of supply network connectivity for primary supplies. A power block is a collection of design logic elements that share a primary supply. a primary supply consists of a single power and a single ground supply net pair this definition of a power block enables the- automatic connection of the primary power and ground nets to all logic elements within the block.

THE POWER SIMULATION FLOW:

Power simulation soles the problem of functional verification of power designs It gives designers the ability to functionally their• power management techniques at the RTL, reducing costs significantly both in terms of effort and time.

Power simulation works with normal RTL coding styles. Designers do not need to hand instantiated gate level retention cells for state data the RTL blocks are easily reused without modifying the RTL code, and new reusable blocks can be created independently of the power environment they may be ed within.

The simulator must be :

Identify all sequential elements by the RTL design puling the appropriate cell model behavior.

Dynamically modify the behavior of the design to reflect the specified low power design intent in power down and up situations.

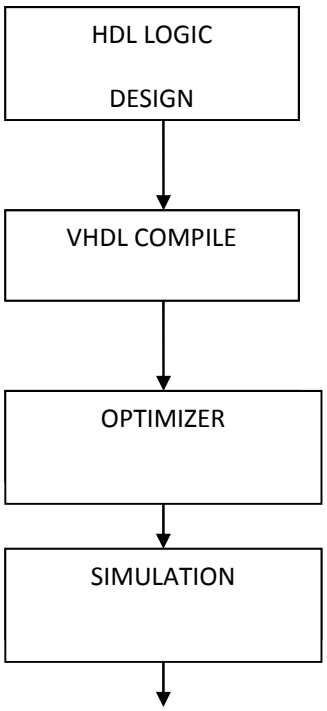
Based on these requirements, simulation is made following steps.

Register/latch recognition from the RTL design.

Identification of power elements and power control signals

Elaboration of the power design

Power simulation.



REGISTEILLATOI AND MEMORY RECOGNITION:

Register, latch, and memory recognition form the RTL is normally associated with the front end of synthesis, which transforms the RTL into a structural netlist containing flip flops ,latches, memories, and combinatorial platform, with the ability to infer sequential elements and recognize memory structures, providing a complete power verification solution.

IDENTIFICATION OF POWER ELEMENTS:

Low power design intent and is processed for the following steps

Power and voltage blocks and power control signals

Mapping of sequential elements

ELOBRATING THE POWER DESIGN:

Elaborating this process, power blocks specified to have state retention in the power configuration file are identified. The sequential elements within these blocks are identified and the power retention behavior mapped to these sequential elements; for ex: power down behavior corruption, state retention, power up behavior and state restoration. All other logic elements within a power block will have their behavior modified such that at power their outputs are corrupted and with power up they resume normal

operation. When a power block is turned off, it goes to an unknown value; in other words, it is corrupt simulation verifies whether the system works properly when the low power design intent is exercised a specified the power models are mainly abstract model of the power retention behaviors. These model typically contain events quiets. The interfaces to models are also predefined. The corruption model simply corrupts at power down and releases at power up. This model is used as a generic corruption model. The retention register can be created with quests power aware.

MODELLING CAPABILITES CAN BE DEVELOPED:

Saving register values Power up and Power down Restoration, of saved values these models work in tandem work in tandem with the RTL when simulated in quests to mimic equivalent power aware behavior after implementation.

POWER AWARE SIMULATION IN ACTION:

The low power design specification with the L functional specification, the power aware is ready to start. The design simulates normally. They can also be used to ensure proper functioning of awake portions of the design in various system power states.

Power aware simulation exposes many functional boos including:

Dependency on output values.

Problems when interacting state machines in different power blocks restore t sates that create deadlock Failure to reset a block upon power on to a known good state for non retentive blocks.

CONCLUSION:

Temperature-dependent design issues are becoming dominant factors in resolving signal- and power-integrity issues in future generations of VLSI chips. There is thus a clear need for effective temperature-aware analysis and optimization tools and design flows that would in turn enable the design of high-performance and reliable IC chips.

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