A NOVEL BIDIRECTIONAL MODEL OF HVDC HYBRID TYPE SUPERCONDUCTINGCIRCUIT BREAKER'S AND ITSPERFORMANCE ANALYSIS FOR LIMITING & BREAKING DC FAULT CURRENT.

G SURESH, P SRINIVAS RAJU, GADA PRAMOD REDDY, 4.PRAVEEN KUMAR
5.C.RAJLINGAM
EEE DEPARTMENT
ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY HYEDERABD TELANGANA INDIA

Abstract—The key obstacle in integrating high-voltage direct current (HVDC) point- to-point networks into meshed multitermi- nal HVDC networks (MTDC) is the absence of dc circuit breakers (DCCBs), which can timely and reliably isolate the faulty HVDC network from the MTDC. In this paper, a novel hybrid-type superconducting DCCB model (SDCCB) is proposed. The SDCCB has a superconducting fault current limiter (SFCL) located in the main line, to limit the fault current until the final trip signal to the SDCCB is given. After the trip signal, insulated-gate bipolar transistor (IGBT) switches located in the main line will commu- tate the fault current into a parallel line, where dc current is forced to zero by combination of IGBTs and surge arresters. DC fault current behavior in MTDC and fundamental requirements of DCCB for MTDC were described, followed by anexplanation of the working principles of the SDCCB. To prove the viability of the a simulation analysis demonstrating SDCCB current interruption performance was done for changing the intensity of dc fault current. It was observed that the passive current lim- iting by SFCL caused significant reduction in fault current in- terruption stress for SDCCB. Furthermore, fundamental design requirements for SFCL, including the effect of SFCL quenching impedance on SFCL voltage rating and energy dissipation capac- ity, were investigated. Finally, advantages and limitations of the SDCCB were highlighted.in Energy Technology of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) under Grant 20154030200730. The work of U. A. Khan was supported

INTRODUCTION

IGH-VOLTAGE direct current (HVDC) systems pro- vide a reliable and cost-effective solution for bridging

long distances for bulk electric power transmission. Recent advances in voltage- source-converter-based HVDC systems (VSC-HVDC) have shown them to be a better alternative than conventional thyristor-based HVDC systems, particularly in developing multiterminal HVDC systems (MTDC) [1]–[4]. MTDCrefers to the HVDC grid formed by integrating two or more HVDC converter stations.

The main component required to develop any electrical grid, whether ac or dc, is the circuit breaker that can quickly and reliably isolate the faulty network from the electrical grid. In

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MTDC, the dc fault current rises rapidly, and its magnitude is very large compared to that in the ac network. Breaking this huge dc fault current is the greatest challenge for MTDC pro- tection system [5]. Due to absence of technology to break the huge dc fault current and isolatre the fault in MTDC, it is still notpossible to develop MTDC, despiteits numerous benefits and many practical applications. HVDC circuit breakers (DCCBs) are needed to selectively isolate a faulty line by quickly and reliably breaking the dc fault current [6], [7].

The superconducting fault current limiter (SFCL), which is an application of superconducrtivity, has been an area of great interest for researchers in the last decade, and several prototypes have been developed and installed in medium- and high-voltage systems [8]–[12]. In this paper, we have proposed a novel hybrid-type superconducting DCCB model (SDCCB), in which a conventional hybrid DCCB (HDCCB) is combined with the SFCL. To prove the visability of the SDCCB, a simulation analysis demonstrating the SDCCB current interruption perfor- mance were done for changing the intensity of dc fault current. Furthermore, fundamental design requirements for the SFCL in the SDCCB were investigated, including the effect of SFCL quenching impedance on the interrupted fault current, SFCL voltage rating, and SFCL energy dissipation capacity. Finally, advantages and limitations of the SDCCB were highlighted.

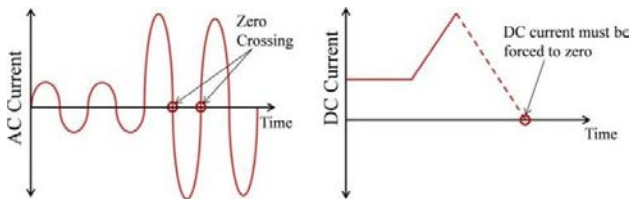


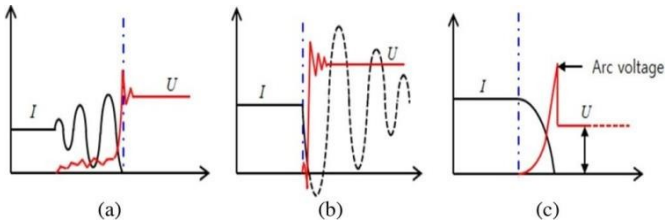
Fig. 1. Differences between ac and dc fault currents

Fig. 2. DC voltage and current waveforms of commonly used methods for dc fault current interruption in dc switchgear. (a) Divergent current oscillation method. (b) Inverse current injection method. (c) Inverse voltage generation method.

I. MTDC FAULT CURRENT AND NEED FOR FAULT CURRENT LIMITING

A. DC Fault Current Interruption Methods

AC circuit breakers interrupt the ac fault current at its natural zero crossing, but there is no zero point in the dc fault current, as shown in Fig. 1. Therefore, DCCBs require an active method for reducing the current to zero level before breaking the circuit. Forcing the huge and rising dc fault current to zero in



HVDC systems requires methods, which are very different fromconventional ac circuit breakers [13].

The three methods commonly used to make zero dc fault current are shown in Fig. 2 and explained as follows [14].

1) Divergent current oscillation method in which the current zero is made by magnifying the amplitude of the high-frequency oscillating dc fault current until it touches the zero point, as shown in Fig. 2(a). Once the current touches the zero point, an ac circuit breaker can be used to open the circuit. This method is highly unstable because it uses large capacitors and inductors to create resonance. In addition, selection of components for its implementation depends mainly on network parameters such as line impedance and load. Therefore, a circuit breaker utilizing this method needs to be modified every time

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if any change in the HVDC system is made. 2) Inverse current injection method creates current zero by superimposing a high-frequency inverse current on dc fault current by discharging a prechargedcapac- itor, as shown in Fig. 2(b). This method results in a complex circuit breaker topology with large number of components and also requires an auxiliary power source to charge the capacitor.

3) Inverse voltage generating method reduces

the current to zero by making the arc voltage higher than the source voltage, as shown in Fig. 2(c). The inverse arc voltage in the circuit breaker ignites the parallel-connected surge arresters, and the network energy is dissipated in these surge arresters, resulting in reducing the dc fault current to zero. The magnitude of reverse voltage and the energy dissipated in the arrester banks

Fig. 3.Three-converter-station MTDC network. After the fault in line 1, normal power flow terminates, and fault currents from all the nodes rush toward the fault point. Current at point B and through line 2 reverses its direction after the fault.are very large. With the latest developments in semiconductor technology and high- voltage valves, this method has been suc- cessfully demonstrated in a conventional HDCCB [15].

B. Large Magnitude of DC Fault Current in MTDC

In MTDC, the dc fault current rises much more rapidly, and it has larger magnitude when compared with that in point-to- point HVDC systems. This is due to multiple power sources and decreased surge impedance in MTDC. Forcing a large dc fault current to zero in a short duration causes enormous voltage and energy stresses for DCCB components [13]. DCCB components capable of enduring these stresses are practically very difficult to develop, due to very large voltage rating, huge energy dissipation requirement, enlarged size, and enormous costs [16]. A fault current limiter can suppress the large dc fault current in MTDC, to breakable values, during the response time of DCCB and significantly reduce the current interruption stress on DCCB components.

C. Necessity of Time Delay for DCCB in MTDC

During a fault in MTDC, all the nodes and their correspond- ing DCCB experience large currents, as normal power flow is terminated and current rushes toward the fault point, as shown in Fig. 3 [17]. At a particular node, it is not possible to identify the faulty line along with the correct DCCB to trip, simply, on the bases of current and voltage at that particular node. A delay is required for the identification of the faulty line among mul- tiple HVDC lines connected with the node. The identification of faulty line may require communication between MTDC con- verter stations located at far distances [16]. During this delay, the fast-rising dc fault current in MTDC could rise to very large values. Fault current limiting would prevent the increasing fault current to reach to unbreakable values during the delay and re- duce the fault current interruption stress on DCCB components.

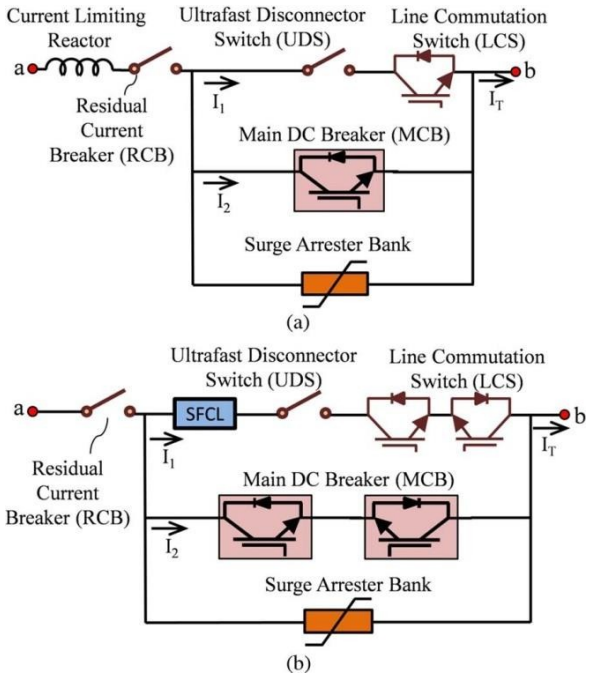

Fig. 4.Single-line diagram of (a) conventional HDCCB and (b) SDCCB.

D. Consideration of Bidirectional Current Flow in MTDC

VSC-HVDCs are the most preferred option to develop MTDC because they have fixed voltage, which makes it easier to integrate them into the nodal structure of MTDC. The outputpower is controlled by changing the current, contrary to conven- tional line-commutated- converter-type HVDC, and therefore, the DCCB in VSC-HVDC must be able to interrupt the current in both the forward and reverse directions [18]. In addition, after the fault in MTDC, the current can suddenly change its direction, as shown in Fig. 3. During the fault, the normal power flow terminates, and currents from all the nodes rush toward the fault point [17]. Hence, the DCCB in MTDC must have bidirectional current breaking capability.

II. SUPERCONDUCTING DC CIRCUIT BREAKER MODEL

The proposed SDCCB is the combination of conventional HDCCB and SFCL. Before explaining the SDCCB, we will brieflyhighlight the working principles andlimitations model. of the conventional HDCCB

A. Limitations of Conventional HDCCB

A prior-art HDCCB is shown in Fig. 4(a) and was pro- posed in [15]. This model works on inverse voltage generation method, as explained in Section II-A. The main components of the HDCCB are shown in Fig. 4(a), and IT is the total current passing through the HDCCB. During normal operation, the ul-

trafastdisconnector switch (UDS), the line commutation switch (LCS), and the residual current breaker (RCB) are closed, and they are conducting the normal dc line current. The main dc breaker (MCB) is opened, and no dc current flows through it. When a dc fault occurs, the MCB is closed, and the LCS opens. Opening the LCS commutates the current to the parallel branch containing the MCB. As the current through the LCS is decreased to a negligible value, the UDS opens with minimumarc and isolates the LCS from any voltage buildup across the HDCCB terminals. Once the trip signal is generated, the MCB

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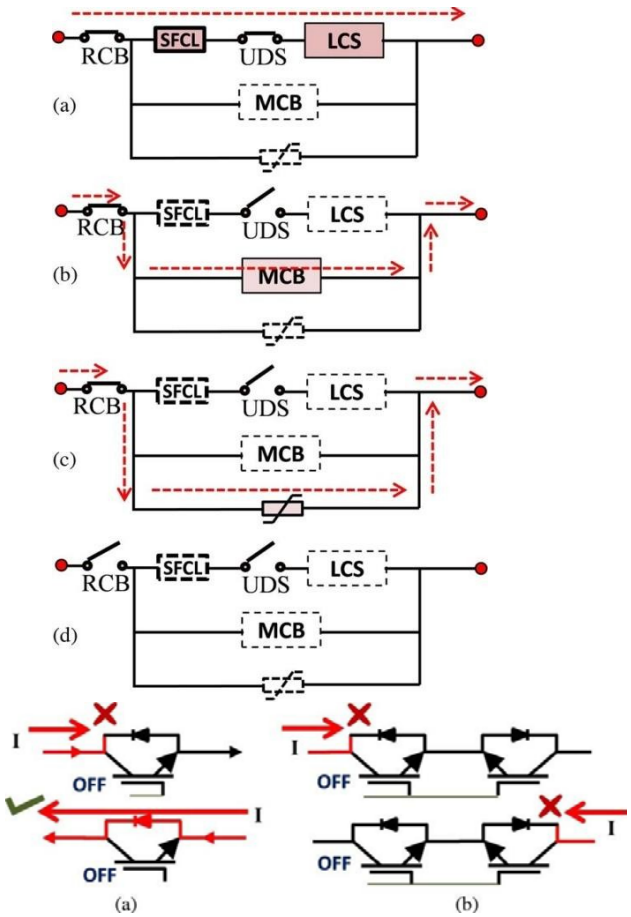

Fig. 5. (a) Single IGBT unable to break current in the reverse direction.

(b) Mirrored pair IGBT configuration breaking current in both directions.

Fig. 6. (a) Fault current is limited by the SFCL as the SDCCB waits for the trip signal. (b) After the trip signal, the MCB is closed, and the LCS opens, causing the fault current to flow through the MCB. Once all the current flows through the MCB, the UDS opens. (c) MCB opens, causing surge arresters to ignite and forcing the fault current to zero. (d) When the current reaches zero, the RCB opens and isolates the HVDC line.

opens, resulting in large inverse voltage buildup across the HDCCB terminals, which ignites the parallel-connected surge arrester bank and forces the dc fault current to zero. Finally, the RCB opens and isolates the HVDC line completely [15].

The HDCCB has a current-limiting reactor in series ofthe normal current path, as shown in Fig. 4(a). The current limiting in the HDCCB is done by pulse- mode operation ofthe MCB, by controlling the voltage drop across the current-limiting reactor to zero [15]. High- power semiconductor valves, such as the MCB in Fig. 4(a), are composed of numerousseries- and parallel-connected semiconductor switches to bearhigh- voltage and high-current stresses.

Repeated switching ofthese high rated valves for current limiting may lead to theirearly failure due to high switching stresses [19]. Active currentlimiting, involving switching of large insulated- gate bipolartransistor (IGBT) valves, is the major limitation of the HDCCB.

Furthermore, the presence of a series current-limiting re- actor causes numerous problems. The reactor energy will be

Fig. 7. (a) SDCCB model developed in MATLAB/Simulink/SimPowerSystems. The controller block controls all the working of SDCCB components.

(b) Control algorithm implemented in the controller module of SDCCB.

discharged during the fault, causing increased dc fault cur- rent. During the current interruption, the reactor will result in large voltage buildup across the HDCCB, due to an inductive kickback effect. In addition, larger inductance in the HVDC network will affect the dynamic response of the system during fast load shifting because of the reactor inductance, which opposes any quick change in current [20].

B. SDCCB

Fig. 4(b) shows the proposed SDCCB, which is the modified HDCCB in Fig. 4(a). Modifications include the following:

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1) the SFCL is placed in series of the main current path (I1);

2) the series reactor has been removed since it is not needed anymore for current limiting; and 3) the single IGBT valve has been replaced by mirrored pair IGBT valves. The single IGBT valves in the HDCCB can only interrupt current in a single di- rection, i.e., from a to b in Fig. 4(a). The reason for this is shownin Fig. 5(a), where a single IGBT, when turned off, can interrupt the current in only the forward direction, whereas a reverse current continues to flow from the IGBT antiparallel diode. Fig. 5(b) shows the mirrored pair configuration of IGBTs. This arrangement of IGBTs, when turned off, will break the current independent of the direction of current flow. Although,Fig. 8. (a) Universal SFCL model developed in MATLAB/Simulink/ SimPowerSystems. (b) Quenching characteristics of SFCL.

SDCCB semiconductor valves, when compared to HDCCB, have doubled and will result in higher cost and larger SDCCB size, this arrangement is inevitable in MTDC as the current in HVDC line can suddenly change its direction during fault, as explained in Section II-D. The SDCCB works as follows. During normal operation, the UDS, LCS, and RCB are closed and conducting, whereas the MCB is opened. After the dc fault, the SFCL quenches and limits the fault current. The SDCCB does not interrupt the current instantaneously, and the decision to trip the SDCCB depends on the following: 1) eliminating the chances of a false trigger due to temporary glitches or spikes;

2) identifying the faulty line and selecting

the correct DCCB among multiple DCCBs on the converter bus; or 3) crossing of safety thermal limit of any of the SDCCB components, including SFCL, LCS, and MCB.

Once the trip signal is given to the SDCCB, the LCS located in the main line opens and commutates the current to the parallel line, where the dc current is made zero by combination of MCB-IGBTs and surge arresters. Finally, the RCB opens and isolates the HVDC line completely. The current interruption method in SDCCB is similar to that in HDCCB, as explained in Section III-A. The interruption time required by the SDCCB after the trip signal is dependent on fault current intensity, as further explained in Section IV-B. Fig. 6 shows the current flow in the SDCCB

during different stages of fault current in- terruption. Fig. 7(a) shows the SDCCB modeled in MATLAB/ Simulink, which was used for simulation analysis in Section IV. Fig. 7(b) shows the control algorithm being used by the SDCCBcontroller in Fig. 7(a).

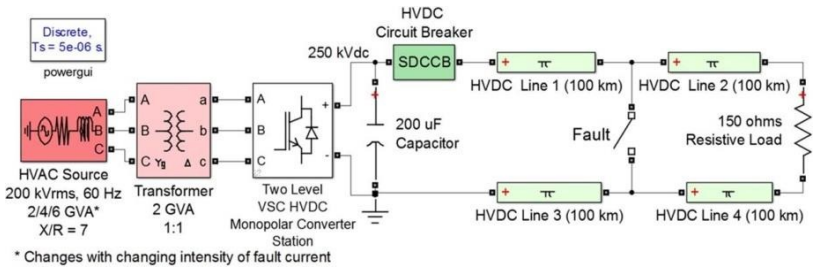

Fig. 9. Test bed model designed in MATLAB/Simulink/SimPowerSystems to perform simulation analysis for SDCCB.

C. SFC L

The main objective of SFCL in SDCCB is to suppress theincreasing dc fault current to alower level and significantlyreduce the current interruption stress on SDCCB components. The SFCL will suppress the dc fault current by inserting additional impedance ZSFCL in the circuit due to its quench- ing. A generic-type dc SFCL was modeled, considering four fundamental parameters of a universal SFCL. These parame- ters and their selected values are as follows: 1) transition or responsetime = 2 ms, 2) minimum impedance = 0.01 Ω,

3) maximum impedance = 20 Ω (also varies as per requirementin Section IV), and 4) triggering current = 3 kA [21]–[23]. Fig. 8(a) shows the SFCL model developed in Simulink/SimPowerSystems, and it works as follows:

1) the SFCL model calculates the sampled value of the passing current and then compares it with the SFCL characteristics table; 2) if the passing current is larger than the triggering current level, the SFCL's impedance increases to the maximum impedance level in a predefined response time; 3) quenching impedance is reflected into the main circuit as a voltage drop generated by the controlled voltage source.

Fig. 8(b) shows the quenching char-acteristics of the SFCL, considering the resistive component of

ZSFCL, during transient simulations in Section

IV. The resistive component of ZSFCL was used in all the transient simulations in Section IV.

Another parameter that is critical for applicability of SFCL in SDCCB is the recovery time of the SFCL. Recovery time is defined as the time required by the SFCL to regain its prefault superconducting state after the fault current through it was reduced below its quenching current value [24]. For SDCCB application in MTDC, the SDCCB SFCLmust have instantaneous fault recovery with very small recovery time. In Fig. 3, we can observe that a fault in MTDC results in large fault current through both the fault-related nodes (nodes N1 and N2) and the unrelated node (node N3) [17]. If the SDCCB in the unrelated node goes into quenching state, it must recover instantaneously once the fault has been cleared. Moreover, short recovery time is also necessary if autoreclosing is needed to be done by SDCCB. However, recovery time is largely dependent on the type of SFCL technology.

A resistive-type SFCL has recovery time in seconds, which is highly undesirable for SDCCB. An inductive-type SFCL with saturated iron core offers almost instantaneous recovery time within 1–2 ms and can be a likely candidate for SDCCB [24], [25]. Our future research work will be focused toward determining the most favorable SFCL technology for SDCCBapplication. Further discussion on the type of SFCL is beyond the scope of the presented work.

III. SIMULATION ANALYSIS AND DISCUSSION

The modeling and simulation analysis of the proposed SDCCB were done in MATLAB/Simulink/SimPowerSystems. It was assumed that the time difference between fault initiation and SDCCB trip signal was 20 ms.The 20-ms delay before interruption was assumed to be caused by the reasons explained in Section II-C. After the trip signal, the SDCCB interrupted the dc fault current and isolated the HVDC line.

A. Test Bed Model

To analyze the working principles and the fault current inter- ruption performance of the SDCCB, a testing setup was mod- eled in Simulink/SimPowerSystems, as shown in Fig.

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9. Table I summarizes the general features of the test bed model. The test bed contains a two-level VSC-HVDC converter station with monopolar HVDC transmission network. Test bed voltage =

250 kV, Load current = 2 kA, and normal power flow =

500 MW. The HVDC transmission line length = 200, and the fault is generated 100 km away from the converter station, as shown in Fig. 9.

The dc fault current intensity in the test bed model is de-pendent on the power rating of the ac system attached withthe VSC-HVDC converter station [26]. Three categories ofac power systems are used, which are denoted as "NormalSystem," "Strong System," and "Very Strong System." The cor-responding fault currents due to these systems are marked as In, Is, and Ivs, respectively. The type of ac systems, their,fault current continued to flow through the IGBT antiparallel diodes, which form an uncontrolled rectifier [6]. The dc fault current in the test bed is composed of three main components:

1) contribution from the ac network; 2) dc-link capacitor dis- charge current; and 3) discharging of the transmission line. These three components are also the dominating factors of dc fault current in real HVDC systems [20].

B. SDCCB

Fault Interruption Performancecurrent intensities when applied in the test bed model in Fig. 9. In, Is, and Ivs represent three fault current in- tensities corresponding to three different ac systems, as shown in Table II. The SFCL quenching impedance (ZSFCL) = 20 Ω, the fault was generated at

60 ms, and the SDCCB limited the fault current up to 80 ms. At 80 ms, the SDCCB was given the trip signal, and it forced the fault current to zero followed by isolating the HVDC line. Fig. 10 shows the prospective fault currents with no SDCCB and the fault currents after application of the SDCCB. The SDCCB has successfully limited and interrupted the dc fault currents. The time required to interrupt the fault current after the trip signal depended on the fault current intensity and varies from 6 ms for In to 12 ms for Ivs. This is due to the fact that, for larger fault current, the SDCCB had to dissipate greater energy in its surge arrester bank and consequently requires more time to

C. SFCL Behavior in SDCCB

The SFCL is an essential component of the SDCCB, and its fundamental design requirements were explored. First, the effect of ZSFCL on the current interruption performance of the SDCCB was investigated, as shown in Fig. 12. The fault current intensity used for this test was selected to be Ivs, as given in Table II. The fault current was limited for 20 ms followed by its interruption. ZSFCL was changed, and its effect on SDCCB current interruption was analyzed. For the smallest value of ZSFCL (5 Ω), the SDCCB had to interrupt the largestfault current. As ZSFCL increased, the fault current interrupted
by the SDCCB decreased with shorter current interruption time. This showed that the large ZSFCL is a needed feature because

TABLE IV PERCENTAGE REDUCTION IN FAULT CURRENT FOR CHANGING ZSFCL

Fig. 13. Comparison of voltage drop across SFCL for changing values of ZSFCL. The larger the ZSFCL, the greater the voltage

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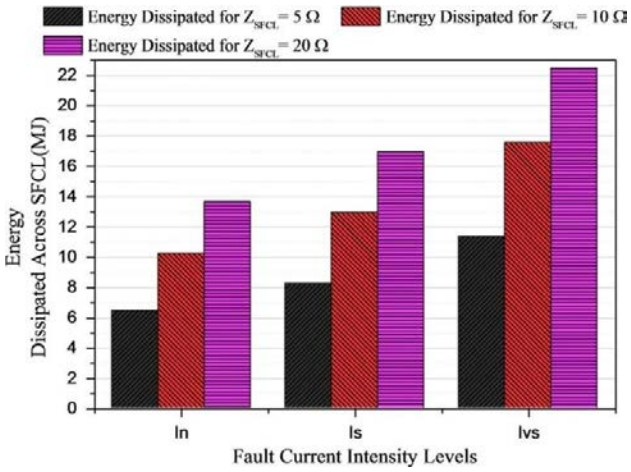


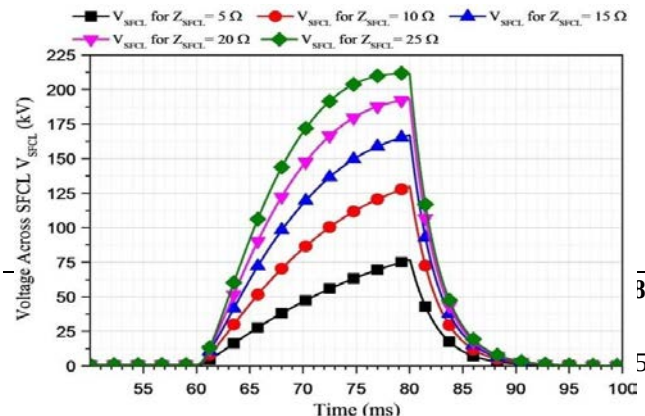
Second, to investigate the effect of ZSFCL on SFCL voltage rating, the voltage drop across the SFCL (VSFCL) during the current interruption in Fig. 12 was measured and shown in Fig. 13. For the smallest value of ZSFCL the SFCL had the lowest VSFCL. As ZSFCL was increased, VSFCL also in- creased, and inevitably, SFCL voltage rating must be frincreased. This effect of ZSFCL is opposite to the effect of ZSFCL on interrupted current intensity, as discussed in Fig. 12. Higher

Fig. 14. Comparison of energy dissipation across the SFCL for changing the intensity of fault current (In, Is, andvIvs, as given in Table II) and ZSFCL. Energy dissipated across the SFCL is directly proportional to the fault

SFCL Quenching Impedance Z_{SFCL}	SDCCB Total Current I_T (kA)	Percentage Reduction (%)
No SFCL	20.5 kA	
5 Ω	16.6 kA	19.0 %
10 Ω	13.7 kA	33.2 %
15 Ω	11.6 kA	43.4 %
20 Ω	9.9 kA	51.7 %
25 Ω	8.4 k A	59.0 %

current intensity and ZSFCL.

VSFCL means larger SFCL voltage rating, which will increase its size and cost. Therefore, ZSFCL needs to be selected care- fully, considering both the SDCCB current interruption abilitym, which is positively



affected by increasing ZSFCL, and the voltage rating of the SFCL, which is negatively affected by in- creasing ZSFCL. Finally, the most critical SFCL parameter was investigated, which is identifying the requirements of energy dissipation across the SFCL. The energy dissipated across the SFCL depends on the following: 1) duration of current limiting;

2) The SDCCB does not require any current-limiting reactor and, thus, does not add any negative effects of increased circuit inductance to the HVDC grid. On the contrary, the HDCCB re- quires a current- limiting reactor, which will affect the transient and dynamic states of the HVDC grid.

3) The SDCCB can interrupt the dc faultdissipated across the SFCL. The SFCL cryogenic system must be capable of removing this energy timely before any permanent damage to the SFCL can occur.

Therefore, SFCL design for SDCCB is dependent on the following: 1) the selected value of ZSFCL, which determines its voltage rating and energy dissipation rating; 2) the maximum value of the prospective fault current in the HVDC network, which depends on the strength of the integrated ac system and the complexity of the MTDC; and 3) the maximum time that the SFCL must limit the fault current in the SDCCB before thetrip signal.

III. ADVANTAGES AND LIMITATIONS

Advantages of the proposed SDCCB model are as follows:

1) The foremost advantage of SDCCB over HDCCB is its passive current limiting ability, which does not require switching of high- voltage IGBT valves. This will significantly increase rthe life of high- voltage IGBT valves. The passive cur- rent limiting is achieved by the SFCL, which has a very quick response time and no conduction losses current in both the forward and reversedirections. The

HDCCB can only interrupt the dc fault current in a single direction.more, fundamental design requirements for SFCL in SDCCB were investigated, including the effect of SFCL quenching impedance on the SFCL voltage rating and energy dissipation capacity. The proposed SDCCB model clearly demonstrated the potential for limiting and breaking dc fault currents in MTDC. Future research will be aimed at investigating the practical problems and proposing solutions for the development of SFCL technology for SDCCB.we can reduce the current interruption stress for SDCCB components and thus significantly reduce their size and cost.

The advantages of the SDCCB over the conventional HDCCB are summarized in Table V. Limitations of the pro- posed SDCCB model are as follows:

1) Enormous energy must be dissipated across the SFCL through the cryogenic environment before any permanent dam- age to SFCL happens. This requires a larger cryogenic systemr with higher power consumption and greater running costs.

2) Although larger ZSFCL is a required feature for SDCCB

to reduce current interruption stress on SDCCB compomnents, it will result in higher voltage drop and greater energy dissi- pation across the SFCL, as shown in Figs. 13 and 14, respec- tively. Therefore, larger ZSFCL increases the SFCL voltage and thermal ratings and consequently increases its size and cost. Special attention is required in desisgning SFCL for SDCCB and in selecting its quenching impedance solution.

IV. CONCLUSION

This paper has explored the possibility of using superconduc- tivity for solving thelong-standing issue of dc current interrup- tion in HVDC networks. We have proposed a novel hybrid-type SDCCB, in which a conventional HDCCB is combined with the SFCL. Working principles of the proposed SDCCB were explained, followed by a simulation analysis demonstrating the SDCCB current interruption ability for changing the intensity of dc fault current. The SDCCB limited the fault current ef- fectively until a predefined time followed by successful cur- rent interruption. The current limiting by the SFCL notably suppressed the dc fault current and significantly reduced the current interruption stress for SDCCB components. Further-

Reference

[1] G. Ding, G. Tang, Z. He, and M. Ding, “New technologies of voltage source converter (VSC) for HVDC transmission system based on VSC,” in Proc. IEEE Power Energy Soc. Gen. Meet., Jul. 2008, pp. 1–8.

[2] J. Pan et al., “AC grid with embedded VSC-HVDC for secure and efficient power delivery,” in Proc. IEEE Energy 2030, Nov. 2008, pp. 1–6.

[3] D. Jacobson, P. Wang, M. Mohaddes,

M. Rashwan, and R. Ostash, “A preliminary look at the feasibility of VSC HVDC in Manitoba,” in Proc. IEEE EPEC, Oct. 2011, pp. 80–85.

[4] D. Jovcic, D. V. Hertem, K. Linden, J. Taisne, and W. Grieshaber, “Feasibility of DC transmission networks,” in Proc. IEEE PES ISGT Eur., Dec. 2011, pp. 1– 8.

[5] R. K. Mallick and R. K. Patnaik, “Fault analysis of voltage-source converter based multi-terminal HVDC transmission links,” in Proc. IEEE ICEAS, Dec. 2011, pp. 1–7.

C. Meyer, M. Kowal, and R. W. De Doncker, "Circuit breaker concepts for future high-power DC-applications," in Proc. 40th IEEE IAS Annu. Meet. Conf., Oct. 2005, vol. 2, pp. 860–866.

[6] M. Noe and M. Steurer, "High- temperature superconductor fault current limiters: Concepts, applications, and development status," Supercond. Sci. Technol., vol. 20, no. 3, p. R15, Jan. 2007.

[7] Y. Xin et al., "Development of 220 kV/300 MVA superconductive fault current limiter," Supercond.Sci. Technol., vol. 25, no. 10, Jan. 2007, Art.ID. 105 011.