HYBRID MODULAR DC TO DC CONVERTER FOR HVDC APPLICATION'S

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Abstract— remarkable progress has been made in the voltage source converter (VSC) based high voltage direct current (HVDC) transmissions. For the upcoming need to interconnect multiple DC transmission lines with different voltage levels, high voltage and large power DC TO DC converters are necessary, This paper investigates bidirectional DC/DC converter which is composed by cascaded half-bridge SMs, series connected diodes. and mechanical This hybrid Popology presents very attractive features such as low cost, high efficiency, and light weight. Operation principle, parameter design, and dedicated control strategies are developed. Simulation of a 150MW, 200kV/300kV DC/DC converter has been performed to verify its performance and evaluate the efficiency. Moreover, a downscaled three-phase prototype rated at 500V/300V 4.5kW has been built and tested. The experimental results further confirm the effectiveness of the proposed DC/DC converter.Index Terms—Bidirectional DC/DC converter, mechanical disconnectors, hybrid topology, energy buffering string, HVDC, diodes, high robustness.

I. INTRODUCTION

The continuous progress in the field of voltage- source- converter (VSC) technology, particularly the development ofmodular multilevel converter (MMC) [1], [2], the VSC-HVDC has been increasingly used for offshore wind power transmission and asynchronous grids interconnection [3].

Recently, VSC-HVDCs in multi-terminal and even the HVDC grids are highly expected in both academia and industry for better integration of large-scale renewable energy sources and strengthening the network stability and reliability [4]. Several multi-terminal HVDCs have already been in operation while one piolet project of a ±500kV/9000MW HVDC grid is currently under construction [5], [6].

However, compared to the mature AC grids, two major technical challenges have to be addressed in future HVDC grids:

1) DC circuit breaker (CB) and 2) DC transformer. Because of the absence of natural current zero in HVDC grids, a DC CB must be able to create an artificial current zero while absorbing the fault energy from DC transmission line plus any added DC inductance. Recent advances of hybrid DC CBs, consisting of mechanical ultrafast disconnector (UFD) and IGBT–based main breaker as well as a load commutation switch, can satisfy the requirements and achieve very short interruption time (2-3 ms) [7], [8]. Many hybrid DC CB topologies have recently

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been proposed and industrial prototypes have also been developed [9]–[11]. On the other hand, DC transformer is required to match the HVDC lines with different voltage levels [12]. Aspossible for DC voltage conversion, power electronics technology must be used. There are plenty ofDC/DC converter topologies in low power applications, but most of these topologies cannot be readily scaled up to hundreds of kilovolts and megawatt power ranges, due to the limitations of losses, cost, dv/dt, filter size, and voltage rating of the semiconductors. To overcome these limitations, several novel HV DC/DC converter topologies based on modular structure have been proposed during the last few years, which utilize series connection of sub modules (SMs) in place of series connection of semiconductors so as to effectively share the voltage stress and improve efficiency [13]. These novel DC/DC topologies can be classified into two categories, according to whether there is galvanic isolation, i.e., isolated types [14]–[18] and non-isolated types [19]–[28]. The common feature of the isolated DC/DC converter topologies is that they are based of and on configuration, which utilizes two full- power DC/AC conversion stages (usually MMC) and an AC transformer. This is a relatively costly solution as each stage must process the full power, resulting in very high components count and high power losses. As a consequence and performance , the isolated topologies are more promoting for applications with a large DC-DC voltage ratio interconnection of HVDC and MVDC systems [18]) or very strict galvanic isolation requirement.

The non-isolated DCtoDC converter topologies, on the other hand, are more suitable for interconnecting HVDC lines with a small voltage ratio. In [19]–[22], the single-stage MMC DC/DC topology is introduced, in which part of the SMs are utilized on both the high-voltage and low-voltage sides, hence it is more efficient than the FTF topologies. However, high magnitude AC voltages and circulating currents need to be injected to exchange power between works the upper level 4 and lower arms, such that the power balance of each SM capacitor can be maintained. Bulky HV filters are therefore required to isolate the injected AC voltages from appearing at the DC terminals. In [23], an additional SM branch was added at the low-voltage DC terminal which actively attenuates the injected AC voltage, but this is at the expense of much higher component count and losses. Besides, the DC/DC auto transformer concept was proposed in [24], in which two MMCs are series connected at the DC terminals whereas parallel connected at the AC terminals through a partial-power AC transformer. In this topology, only part of the total power was transmitted through the AC transformer while the remaining part is transferred directly through the DC path. Thus, capacity of the ACthe Monverter loss can be reduced. Based on this concept, a multiport DC auto transformer topology has been reported [25]. In [26], to avoid the use of the dulky AC trasformer (which suffers higher DC offset and onset voltages stress) in theDC auto transformer, the AC transformer was replaced by a cross-connected SM branch between the upper and lower arms. Meanwhile, in [27] and [28], a novel hybrid cascaded DC/DC converter (HCDC) was proposed, with each phase constructed by two branches of series-connected IGBTs and one branch of cascaded SMs. The cascaded SMs operate as an energy storage element, which connects with one DC side to store a certain amount of energy and then switches to the other side to release the absorbed energy. The poly-phase structure is employed which avoids the DC power flow being interrupted by single- phase switching action. This topology requires few additional components beside several small inductors, hence it shows very small

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footprint. However, the disadvantage of this topologys is that it needs direct indirect series connection of a large number of IGBTs. In brief summary, the existing DC/DC topologies are either technically and manually complex or extensive , which hinders their application and results in the development of HV DC/DCconverter falling far behind the DC CBs.

This paper presents a new hybrid modular DC/DC converter (HMDC) topology for HVDC applications. By incorporating several mechanical disconnections, the topology can achieve efficient bidirectional DC/DC conversion with only limited number of cascaded half-bridge SMs and series connected

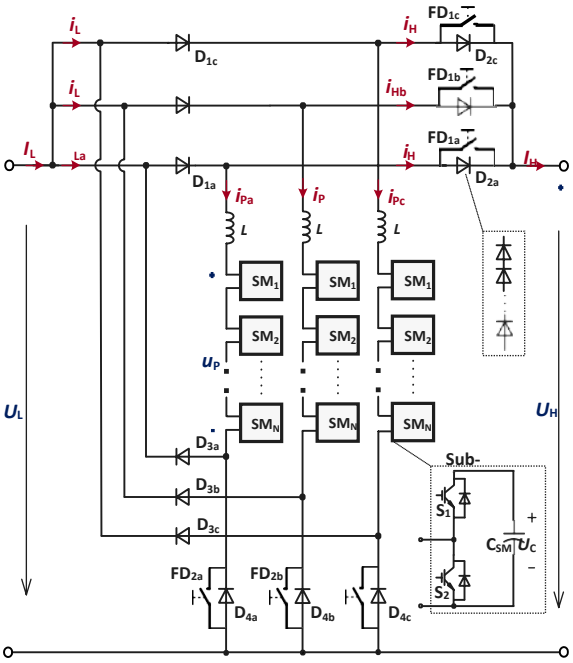

Fig. 1.Configuration of the proposed hybrid modular DC/DC converter (HMDC) topology.

B. Operation Principle of the HMDC Topologydiodes, showing very attractive features of low cost, high efficiency, and simplicity. The circuit configuration as well as its operation principle, parameter design, modulation and control schemes, are presented and verified by simulation results. Moreover, a downscaled prototype has been built and tested to further confirm effectiveness of the proposed topologies.

II. PRINCIPLE OF OPERATION

Circuit configuration of the proposed hybrid modular DC/DC converter It contains three interleaved each phase is formed by four brooches of series connected diodes (D1j, D2j, D3j, and D4j) and one energy buffering string formed by series connected SMs and an inductor L. There are a total of N SMs in each string and each SM is a half-bridge circuit. Particularly, mechanical disconnections FD1j and FD2j are paralleled with D2j and D4j, respectively. FD1j and FD2j are used to achieve bidirectional power transfer capability and they are in complementary operation: FD2j is kept on while FD1j is off when power is transmitted from the low-voltage (LV) side to the high-voltage (HV) side; whereas FD2j is off while FD1j is on when power is transmitted in the opposite direction. The terms UL and IL are the voltage and current of the LV DC side, and UH and IH are the voltage and current of the HV DC side, respectively. iLj and iHj represent the currents of each phase at the LV and HV sides, respectively. UC is the SM capacitor voltage, thus the SM terminal voltage is UC when S1 is on and S2 is off, whereas the SM terminal voltage is 0 when S1 is off and S2 is on. uPj is the sting voltage which is summation of the N SM terminal voltages,andiPj is the string current.

B. Operation Principle of the HMDC Topology

Fig. 2 shows the operation waveforms of the HMDC topology when DC power is transferred from the LV side to the HV side. The energy buffering string alternatively connects with the two DC terminals, to store a certain amount of energy from LV DC side during [0, 0.5Th] and then release the energy to the

HV DC side during [0.5Th, Th], where the string current iPj is controlled as trapezoid waveforms with positive and negative amplitudes of IL and IH, respectively. Hence, the string current would flow through D1j when iPj>0 and D2j when iPj<0, respectively. Meanwhile, the diodes D3j are kept reversely blocked while D4j are bypassed as the disconnectors FD2j are closed. The three-phase waveforms of HMDC are interleaved with 120° electrical angle . Despite the iHj and iLj in one phase of HMDC are discontinuous, the total DC currents iH and iL, given by summation of the three-phase iHj and iLj currents, are ensured to be continuous DC, as a result of the ripple cancellation effect of interleaved waveforms.

The string voltage uPj not only needs to alternatively match the LV and HV DC voltages, but also includes an extra U0 component which is imposed across the inductor to regulate the iPj waveform during the current rising or falling process Tcp. Besides, to avoid generating excessive dv/dt, a staircase shaped waveform is utilized during the rising and falling transitions of uPj, which limits the voltage slew rate by sequentially switching the SMs at an interval of a few microseconds [16].

To withstand hundreds of kilovolt, the diodes in the HMDC must be used in series. With respect to the diode branches D1j and D2j, when power is transferred from the LV to HV sides, they are alternately conducted. Consequently, the maximum voltage stress they need to withstand is the voltage difference between the HV and LV sides. On the other hand, when power is reversed, D2j are bypassed while D1j are reversely blocked which still withstand the voltage difference between the HV and LV sides. Therefore, the required number of series-connected diodes in D1j and D2j is

Compared with the IGBTs employed in [27], diodes exhibit many salient features. For comparison, two commercial devices of similar current rating (5SNA3000K452300 IGBT [29] and 5SDD50N6000 Diode [30]) are compared, as listed in Table I. Diodes have higher voltage ratings, hence the number for series connection as well as the associated cost and complexity, can be reduced. Furthermore, in terms of series connection of IGBTs, both active gate clamping control and passive snubbers are required to achieve static and dynamic voltage sharing. On the contrary, only passive snubbers are necessary with respect to the series connection of diodes. Moreover, diodes present lower on-state voltage drop which means lower power losses.

(9) For instance, the 5SNA3000K452300 IGBT conducting a current of 3000A is expected to have a forward voltage drop ofwhere UB is the rated blocking voltage of each diode and λd is the voltage derating factor in terms of series connection.

Analogously, the diodes D3j and D4j have to withstand the voltage of LV DC side, which yields3.65V, whereas the 5SDD50N6000 conducting the same amount of current only gives an 1.2V voltage drop. Besides, diode has much higher surge current robustness than IGBT. Therefore, by fully developing the current controllability of theenergy buffering strings in the proposed HMDC topology, diodes can be adopted, which reduces the capital cost, losses,

On the other hand, with respect to the current rating, diode D1j only conduct the DC current IL during one third of the operation cycle, because of the 120° waveform interleave among the three phases. Hence, the average current of the diode

C. Fast Mechanical Disconnectors

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In the proposed HMDC, mechanical disconnectors are used to achieve bidirectional power transfer capability. ThemanedchDan,icreaslpdeicsctiovnenly e.ctTohrsusF,Dth1jeaFnDd FDsh2joaurled phaarvaellethleedawbiiltihtyDto2j [31]), fast mechanical switches must be employed. Borrowing from the hybrid HVDC circuit breakers, ultrafast disconnectors (UFD) are available which are capable of opening within several milliseconds (2~3ms) at the nearly zero current condition [7]. In the proposed HMDC topology, thanks to the current controllability of the energy buffering string, FD1j and FD2j can also achieve zero-voltage and zero- current (ZVZC) opening and closing. As a result, there is no technology barrier to employ UFDs in the HMDC and satisfy both normal and emergency power reversal conditions.

TABLE I

CHARACTERISTICS COMPARISON BETWEEN THE IGBT AND DIODE

	IGBT	Diode
Producttype	5SNA3000K452300	5SDD50N6000
Maximumblockingvoltage	4.5kV	6kV
Ratedon-statecurrent	3000A	4210A
Voltage balancing in terms ofseriesconnection	Active di/dt and dv/dt gatecontrolandpassivesnubber	Passivesnubberonly
On-statevoltage	3.65V@I_c=3000A,T_{Vj}=125 ℃	1.2V@I_{FM}=3000AT_{Vj}=125 ℃
Surgecurrentcapability	21000A⁺	71200A⁺⁺

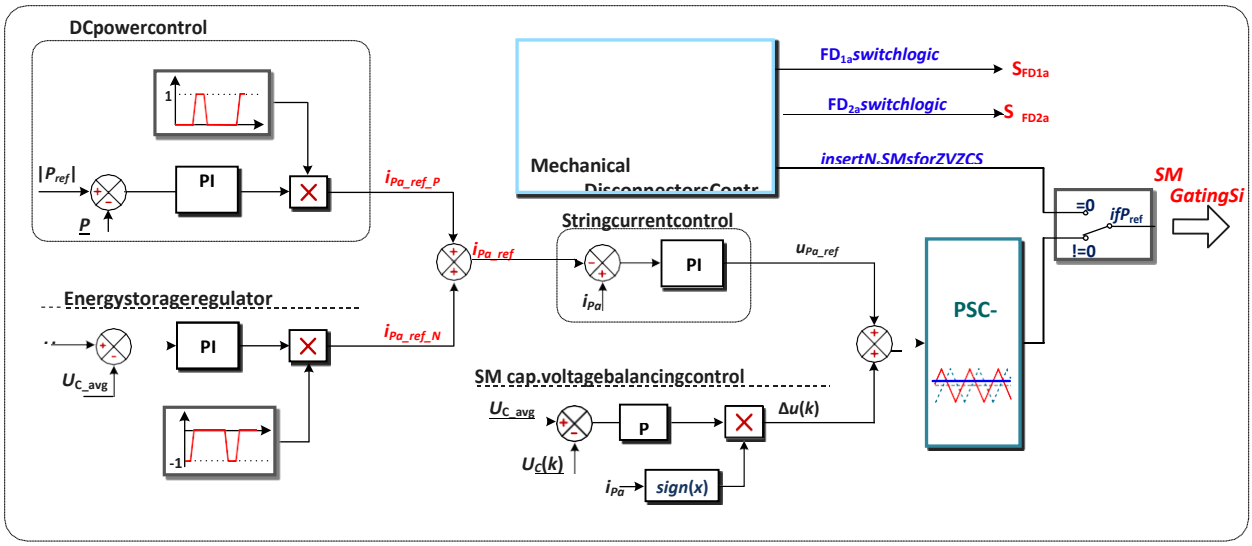

Fig. 4. Control block diagrams for the proposed HMDC converter.

IV. CONTROL SCHEMES

A. General Control

Suitable control schemes are necessary to ensure proper operation of the proposed DC/DC converter. The general architecture of the controller is presented

in Fig. 4, in which phase a is taken as an example. The control system can be divided into six main parts: DC power control, energy storage regulator, string current control, SM capacitor voltage balancing, phase shifted carrier pulse-width modulation (PSC- PWM), and control logics of the disconnectors.

The DC power control manages the transferred power between LV and HV sides. This control block generates the positive amplitude of the string current reference, iPa_ref_P. Then the energy storage regulator compares the average SMenergy in the string) against the nominal value UC_ref and determines the negative amplitude of string current reference, iPa_ref_N, to ensure power balance of the string. Subsequently, the

iPa_ref_P and iPa_ref_N. The string current control further produces the string voltage reference uPa_ref for shaping the desired current waveform. Besides, by limiting the slew rate of the proportional-integral (PI) controller, the rising and falling transitions of the final string voltage waveform uPa can be automatically staircase shaped (i.e., switching the SMs sequentially to avoid generating excessive dv/dt).

generated by disconnector control logics instead of the PSC- PWM generator. At this instance, the string voltage reference uPa_ref is set as UH and then divided by the value of the capacitor voltage to round down to the closest voltage level, Ns. After knowing Ns, the controller inserts Ns SMs to counteract the HV DC side voltage UH. The final voltage of energy buffering string may be slightly smaller than UH, but the difference can be limited less than one capacitor voltage UC (corresponding to the rounding error). As a result, voltage stresses of the disconnectors during both opening and closing are quite low, and in the meantime, currents of the disconnectors are zero since the power is null. This means a ZVZC switching condition has been created by the energy buffering string. The control signals of disconnectors (SFD1a and SFD2a) are then inversed after certain time delays, Tdelay1 and Tdelay2. These delay times are determined by the opening and closing speed of the selected disconnectors. After that, controllers of the PSC-PWM generator and capacitor voltage balancing control are enabled again and the power begins transferring in the opposite direction.

In summary, using mechanical disconnectors, the proposed HMDC topology achieves bidirectional DC/DC power transfer capability. The mechanical disconnectors are basically opened and closed at ZVZC condition, thus they can be made in lightweight [7].

V. SIMULATION STUDY

In order to access validity of the proposed topology and control strategies, simulation of an 150MW HMDC which connects two HVDC systems with voltages of 300kV and 200kV, is performed in MATLAB/Simulink software. In each energy buffering string, there are a total of 180 SMs and each rated SM voltage is 2kV. Detailed parameters of the simulated circuit and operating conditions are listed in Table II.

Fig. 6 displays the key simulation results of the proposed DC/DC converter. As shown in Fig. 6(a), initially, the rated DC power was transferred from the HV side to the LV side. The disconnectors FD1j were kept closed while the disconnectors FD2j were opened, as shown in Fig. 6(b). Then, between 0.3s and 0.5s, the power was ramped from –150MW to 0. After power reached zero, the control logics of FD1j and FD2j were inversed, which reconfigured the

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HMDC topology to transfer power from the LV side to the HV side; afterwards, the power was gradually increased from 0 to 150MW and maintained 150MW after 0.8s, meaning the power flow was completely reversed. Figs. 6(c) and (d) show the voltages (UH and UL) and currents (iH and iL) of the two DC terminals, respectively. Figs. 6(e) and (f) show the voltages and currents of the three-phase energy buffering strings. It is shown that the energy buffering

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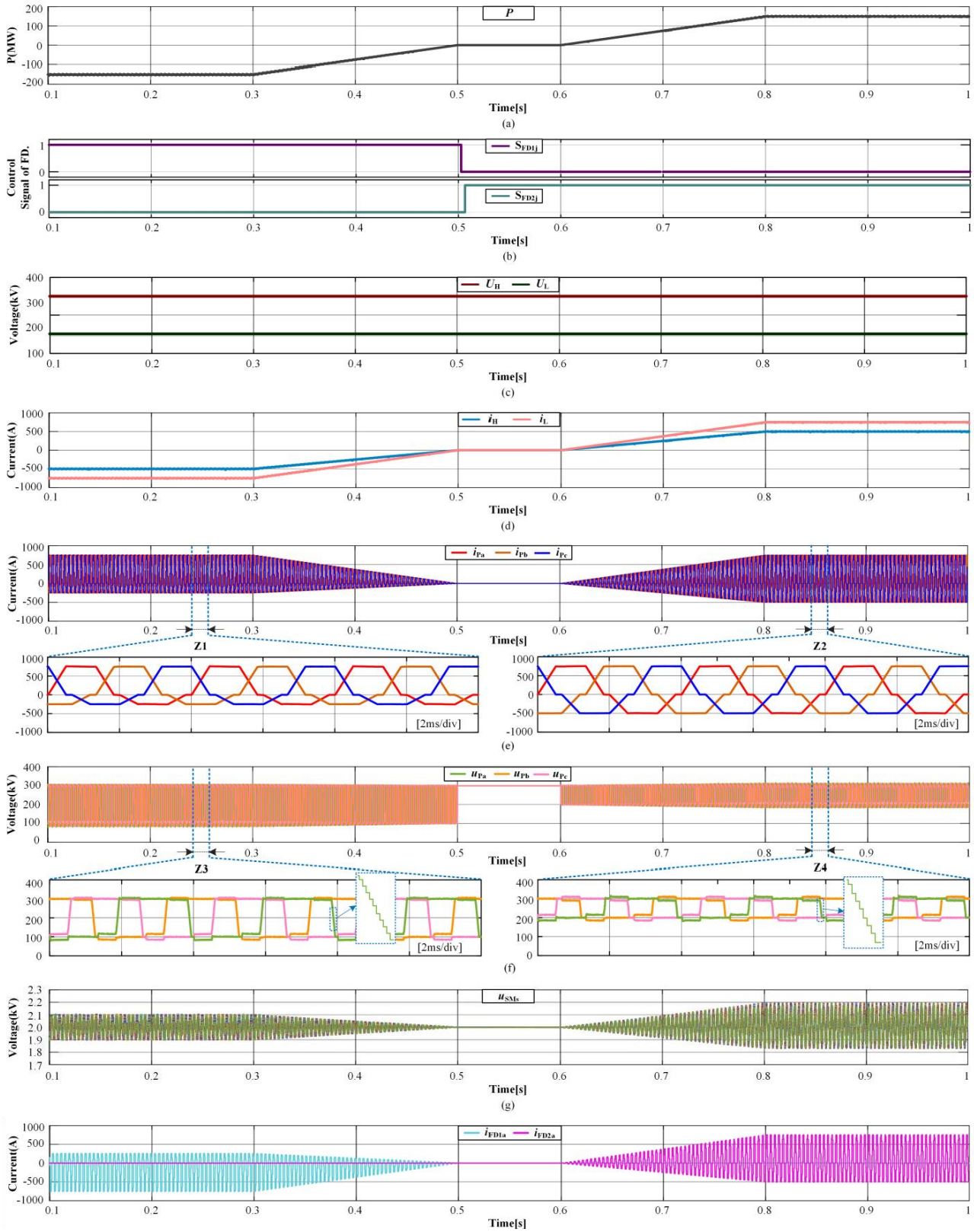

TABLE II SIMULATION PARAMETERS

ConverterParameters	Value
RatedDCpower	P=150MW
HVDC voltage	U_H=300kV
LVDC voltage	U_L=200kV
No. ofSMsineach string	N=180
AverageSMcapacitorvoltage	U_C=2kV
SMcapacitance	C=2mF
SMcapacitorvoltageripple	ε=20%
PSCcarrierfrequency	f_c=580Hz
Operationalternatingfrequency	f_h=250Hz
Arminductance	L=10mH

ControlParameters	Value
Proportionalgainofenergyregulator	0.01A/V
Integralgainofenergyregulator	1A/Vs
Proportionalgainofcurrentcontrol	720V/A
Integralgainofcurrentcontrol	72kV/As

strings operate with 120° electrical angle apart, which can be observed in the zoomed regions of the waveforms. As a result, the identical but interleaved string currents guarantee a continuous and smooth DC current waveform. Besides, the 180 SM capacitor voltages in phase a are shown in Fig. 6(g) which were kept well balanced around the rated voltage of 2kV. Figs. 6(h) and (i) further present the currents (iFD1a, iFD2a) and voltages (uFD1a, uFD2a) of the mechanical disconnectors FD1a and FD2a. These results confirm the effectiveness of the proposed DC/DC converter and the control strategies.

Moreover, Fig. 7 demonstrates the detailed steady-state waveforms of phase a when the power is transferred from the HV side to the LV side. The energy buffering string either inserts between the HV and LV DC sides (uPa around 100kV) or parallels with the HV side (uPa around 300kV). And the diodes D3a and D4a alternatively conducted the string current, as shown in Fig. 7(b), thus the diode voltages uD3a and uD4a would alternatively withstand the LV side voltage UL, as displayed in Fig. 7(c). Observing the voltage of energy buffering string in Fig. 7(d), the zoomed-in view presents a staircase shaped waveform during the falling transition (rising transition is identical), so that the dv/dt stress can be well limited. In Fig. 7(e), the SM capacitor voltages are depicted, which are well balanced.

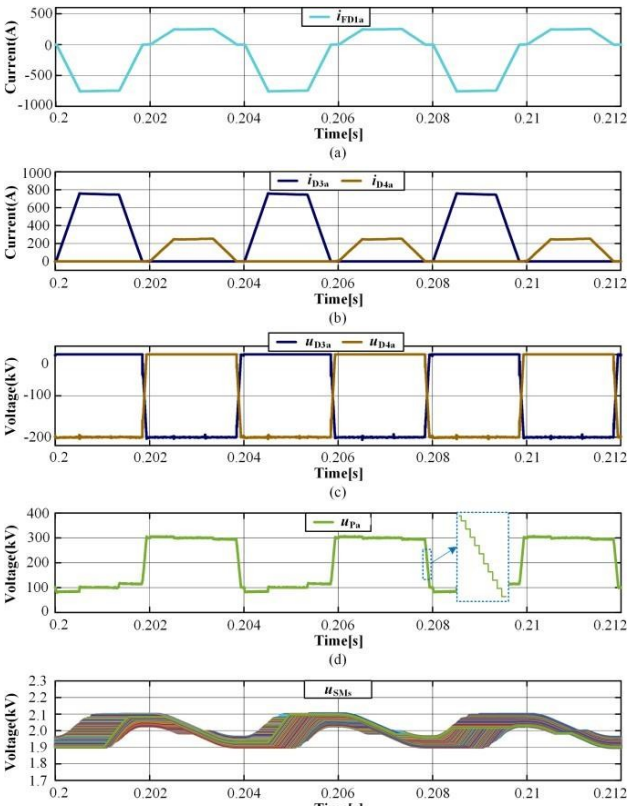

Fig. 7. Detailed waveforms of the proposed DC/DC converter when rated DC power is transmitted from the HV side to the LV side: (a) current of FD1a; (b) currents of D3a and D4a; (c) voltages of D3a and D4a; (d) voltage of energy buffering string; (e) SM capacitor voltages.

Similarly, if the DC power is delivered from the LV side to the HV side, detailed waveforms in phase a under this case are summarized in Fig. 8. Fig. 8(b) and (c) show the current and voltages of D1a and D2a. It is shown the string current iPa was alternatively conducted through these diodes. Notice that, the capacitor voltage fluctuation in Fig. 8(e) is approximately doubled comparing to Fig. 7(e), which can be explained by Eq.

(2) and (5), and the voltage ratio k equals 1.5.

To verify the opening and closing performances of the mechanical disconnectors, waveforms during the power reversal transients are further zoomed in and displayed in Fig.

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9. At 0.5s, the DC power flow was ramped up to zero; and the currents of mechanical disconnectors (iFD1a and iFD2a) both stayed at ZC status, as shown in Fig. 9(c). On the other hand, the energy buffering string inserts appropriate number of SMs to counteract with UH, resulting in almost ZV status for the mechanical disconnectors, as described in Fig. 9(d) and (e). The further zoomed-in view of disconnector voltages uFD1a and uFD2a are displayed in the dotted box in Fig. 9(e). It can be observed there was only a small voltage across FD1a and FD2a. Afterward, the controller inversed the control logics (SFD1j and SFD2j) sequentially at ZVZC conditions, as in Fig. 9(b). In brief summary, thanks to the high controllability of the energy buffering string, ZVZC closing and opening of the mechanical disconnectors can be realized.

VI. EXPERIMENTAL VERIFICATION

A. Experimental Prototype Setup

In order to further verify the validation of the proposed DC/DC converter, a downscaled three-phase prototype rated at 500V/300V, 4.5kW has been built in the authors' laboratory, as shown in Fig. 10. Each energy buffering string contains seven SMs, and each SM is comprised of two IGBTs (Infineon IKW30N60T) and an 1mF capacitor. Two DC voltage sources are connected to the proposed HMDC to emulate two HVDC systems. The diode branches adopt the DD100N16S (Infineon), and the mechanical disconnectors adopt the LC1D09BDC (Schneider Electric). The main circuit parameters are collected in Table III. A digital signal processor TMS320F28335 DSP plus an EP3C25Q240C8 FPGA are employed to realize the control algorithms. Moreover, each SM is controlled by an independent EPM570T100 CPLD.

B. Experimental Results

Fig. 11 presents the experimental results for verifying the bidirectional power transfer capability. In this experiment, the proposed HMDC initially transmitted 4.5kW power flow from the HV side to LV side, and then turned into power reversal process. Eventually, the power flow was transmitted from the LV side to HV side. In this entire process, the DC currents (iH

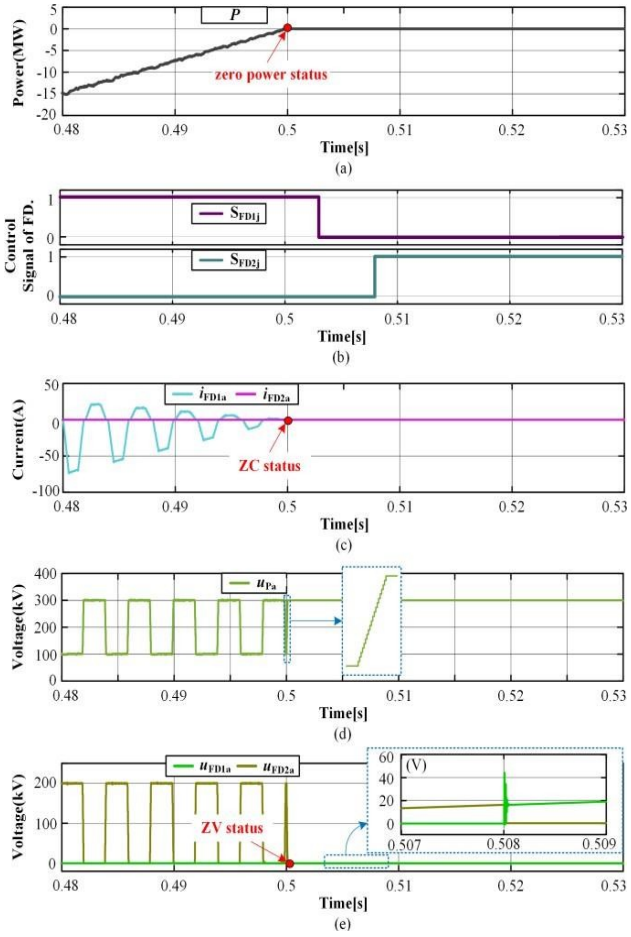

Fig. 9. Zoomed waveforms of the closing and opening processes of FD1a and FD2a: (a) DC power; (b) disconnector control logics; (c) currents of FD1a and FD2a; (d) voltage of energy buffering string; (e) voltages of FD1a and FD2a.

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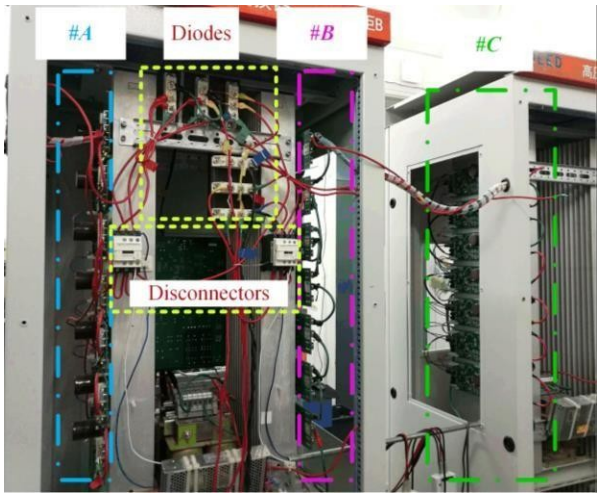
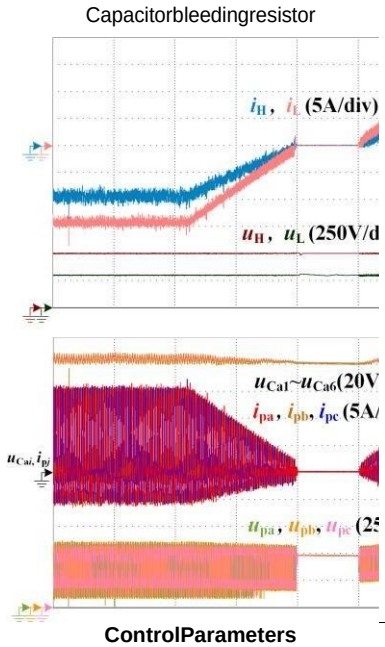


Fig. 10. Photograph of the laboratory prototype.

ANdiL) satisfactorily followed their reference and maintained continuous and smooth, as described in Fig. 11(a). However, some visible harmonics existed and this is due to the limited number of SMs in each string in the experiment, as a result, switching of one SM would cause non-negligible harmonics and influence the current waveform quality. Besides, the SM capacitor voltages remained stable and well balanced during the whole process, as described in Fig. 11(b). These results again

TABLE III EXPERIMENTAL PARAMETERS

ConverterParameters	Value
RatedDCpower	P_{max}=4.5kW
HVDC voltage	U_H=500V
LVDC voltage	U_L=300V
No. ofSMsineach string	N=7
AverageSMcapacitorvoltage	U_C=85V
SMcapacitance	C=1mF
PSCcarrierfrequency	f_c=6kHz
Operationalternatingfrequency	f_h=250Hz
Arminductance	L=1mH



ControlParameters	Value
Proportionalgainofenergycontrol	0.05A/V
Integralgainofenergycontrol	0.5A/Vs
Proportionalgainofcurrentcontrol	5.95V/A
Integralgainofcurrentcontrol	279.60V/As

reversal: (a) voltages and currents of the two DC sides; (b) capacitor voltages of the SMs uCa1~uCa6; voltages and currents of energy buffering string confirmed the effectiveness of the DC/DC topology as well as the proposed control strategies.

The detailed steady-state waveforms of the DC/DC converter, when power was transferred from the HV to the LV side, were given in Fig. 12. In this case, the FD1j was closed to provide bidirectional current path as shown in Fig. 12(c), while the FD2j was opened. It can be observed from Fig. 12(b), the three-phase string current waveforms were almost identical but interleaved with 120° electrical angle, resulting in continuous HV and LV DC currents iH and iL. On the other hand, Fig. 13 shows the steady-state operation waveforms of the proposed DC/DC converter, when power was transmitted from the LV to the HV

side. Control logics of the mechanical disconnectors are inversed compared to Fig. 12, and the DC currents are reversed. Finally, Fig. 14 shows the

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transient performances under power reversal, where the voltages and currents across the mechanical disconnectors (FD1a and FD2a) as well as the corresponding control signals (SFD1a and SFD2a) are displayed. It can be observed in the zoomed region that the disconnector currents iFD1a and iFD2a were controlled to zero as the power ramped down to null. And then, the energy buffering string was forced to withstand the HV side voltage, so as to create almost ZV condition for the disconnectors, as shown in the uFD1a and uFD2a waveforms. These results coincide with the timing diagram as described in Fig. 5. It again confirmed the feasibility of employing mechanical disconnectors to fulfill bidirectional

DC power transfer.

VII. LOSS EVALUATION AND DISCUSSIONS

In attempt to evaluate the losses of the proposed DC/DC converter, a simulation model rated at 300kV/200kV, 150MW is further performed by co-simulation between MATLAB/Simulink and PLECS software. Considering the series connected diodes (D1j, D2j, D3j, and D4j) operate in ZCSmanner and the operation frequency is relatively low (250Hz in this simulation), the grid-commutated rectifier diode 6.8kV/1.59kA D1481N (Infineon, Press-pack, VT0=0.75V) are adopted. And the voltage derating factor λd is set as 0.7. According to (9) and (10), 21 diodes are required in D1j and D2j, and 42 diodes are required in D3j and D4j. The ABB 3.3kV/1.2kA IGBT module 5SNA1200G330100 is employed in the SMs. Other parameters are exactly same as Table II, and the junction temperature of 85℃ are assumed for all the semiconductors in this simulation.

Fig. 15 presents the power loss of each diode in the series branch. Since the diodes operate in ZCS mode, only the conduction losses are considered here. It can be found losses of D2 and D4 are relatively smaller than that of D1 and D3, because their average current are lower according to Eqs. (11)–(14). The loss distribution of each SM are shown in Fig. 16. It can be seen that the switching loss is dominant. Particularly, the loss is higher when power is transferred from LV to HV sides, since the string current amplitude is higher under this case.

Based on the losses of Figs. 15 and 16 and by multiplying their semiconductor numbers, the overall converter loss can be calculated, as shown in Fig. 17. It can be concluded that theoverall converter efficiency is about 99.18% when power was transferred from LV to HV side, and 99.31% in the opposite direction. Thererfore, the proposed DC/DC converter can achieve very high conversion efficiency.

VIII. CONCLUSION

A hybrid modular DC/DC converter (HMDC) is proposed in this paper for future HVDC interconnections. For avoiding series connection of a large amount of IGBTs and achieving efficient power conversion, series connected diodes and mechanical disconnectors are used in combination with the energy buffering strings which are cascaded by half-bridge SMs. The bidirectional DC power transfer capability is realized by fully exploring controllability of the energy buffering strings and using appropriate control logics. The operation principle and control strategies are discussed. Simulation and experimental results have demonstrated the effectiveness and validity of the proposed DC/DC converter. This DC/DC converter shows very attractive features such as low cost, high efficiency, and light weight, which provides an attractive solution for filling in the blank of “DC transformer” in meshed HVDC systems.

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