COMPARATIVE ANALYSIS OF LEAKAGE CURRENT, DELAY AND POWER DISSIPATION FOR DOMINO, DOIND AND ACTIVE BODY BIASED DOIND-ABC1 AT 70NM TECHNOLOGY

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Abstract

In high performance processor and memory device extensively used a dynamic CMOS logic circuits. In comparison of static CMOS it has higher performance due to higher speed so it has less noise immunity and increased leakage power dissipation.

Increase leakage current combine with reduced noise margin results in performance degradation of dynamic circuits. Design of dynamic circuit should be such that reduces leakage current and improve the noise margin.

In this thesis active body biased domino logic is proposed for domino logic which reduces the leakage current with minimum delay penalty. In this thesis different Active body biased technique for DOIND approach namely DOIND-1, DOIND-2, DOIND-3 and DOIND-4 has been used to analyze different parameters.

Proposed DOIND-3 approach has maximum 84% improvement in leakage current among all four proposed technique as compare to domino logic circuit. Proposed DOIND-3 approach also has improvement in most of parameter as compare to all other approaches.In this paper effect of frequency variation in different circuits has been analyzed. All the parameter have been performed at 70 nm technology node using tanner EDA tool with supply voltage 0.9v.

Keywords: Precharge, active body biased, Evaluation, power dissipation, Domino logic.

I.INTRODUCTION

As the semiconductor industry approaches limits of traditional silicon CMOS scaling, the introduction of performance boosters such as novel materials and innovative device structures has become necessary for the future of CMOS scaling [11].

Low leakage current and noise immunity is big challenge for the new researchers. To improve importance of portable systems and less power consumption in very high density VLSI chips result in quick and inventive growth of low power design. Higher power decay reduces the

Battery life in battery operated applications and also reduces the reliability. The leakage Current increases drastically with each new technology inventions. In deep-submicron technologies Leakage power loss is a major problem because it drains the battery even when a circuitry of the system is completely idle. As scaling down the technology node, power supply and threshold voltage also scale down because power supply voltage and threshold voltage of MOS transistor is critical parameters to regulate the performance and switching speed of MOS devices.

In this paper domino logic Active Body Biased DOIND Approach is used to analyze different parameter.

II. RELATED WORK

There are some techniques that is previous design to control leakage current in domino logic circuits. When more than one transistor is turned OFF in series than subthreshold leakage current flowing through a stack of series transistors reduces [1]. This effect is known as stacking

effect. As increases the depth of stack more saving of leakage current is observed. A transistor of width W is replaced by two transistors with width of W/2, this is called forced stacking.

In the Lector Technique [2] two leakages control transistor (one PMOS and one NMOS) is introduce between pull-up and pull-down circuits within standard logic circuits. This arrangement ensures that one of the LCTs always operates in its near cut off region .the basic idea behind LECTOR approach is that "a state with more than one transistor OFF in a path from supply voltage to ground.

INDEP approach [3]is the technique to reduces the leakage current in nanoscale circuit. In this approach to extra inserted transistors between pull up and pull down networks that are input logic dependent.

Leakage biased domino logic circuits [4] regulate the high speed with fine gran leakage reduction. This approach reduces several fold steady state leakage current as compare to low vth domino logic design.

A novel Leakage reduction DOIND Approach [5] for nanoscale Domino logic circuits. It uses Domino logic with clock and input dependent transistors. In this logic two transistors connected between precharge and pull down netwoks. All the body terminal of PMOS transistors connected to Vdd and Body terminal NMOS transistors connected to Gnd.

Dual threshold voltage (DVT) DOIND Logic approach [6] low Vth transistor are chosen in critical path while high vth transistors are chosen in noncritical path . In this technique high Vth and low Vth transistors are used to reduce leakage current in the sleep mode and DOIND transistors used in active and sleep mode.

Sleep switches DVT DOIND logic circuit based buffer approach [7]reduce the subthreshold leakage current in both active and sleep mode of DOMINO Logic circuits. A high vth NMOS sleep switch is connected to dynamic mode and the operation is controlled by extra sleep signal.

III DYNAMIC LOGIC ACTIVE BODY BIASED LOGIC

1) Domino Logic circuits

The General structure of DOMINO logic circuits is shown in fig. 1. The operation of the circuits in this manner When the clock signal is getting low, the domino logic circuit is in precharge phase. In the precharge phase, the node N1 is charged to Vdd thro MP1.Vout of the circuit is low which turn on the keeper transistor (MP2), when the clock signal is getting high, the circuit enters into the evaluation phase. In this phase according to the input combination of pull down network dynamic node N1 is discharged to ground or remain high.

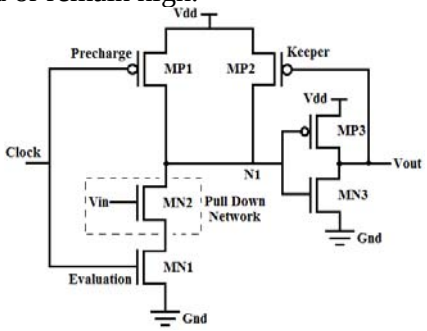

Fig.1: Domino Logic circuit based buffer

The inverter output voltage can also make one transition during the evaluation phase from 0 to 1.

Inverter and week keeper transistor are always used to avoid cascading and charge sharing problem. Performance degrades by adding keeper transistor. Upsizing the keeper transistor improves robustness at the cost of delay and power dissipation and small sized keeper is desired for high speed application. So here is trade off between delay and power to improve noise and leakage immunity.

2) DOIND Logic

In the DOIND (**Do**mino logic with Clock and **IN**put **D**ependent transistors) logic circuit is shown in fig.2. It has two DOIND transistors MP4 (PMOS) and MN4 (NMOS) connected between A and B. Gate terminal of DOIND transistors (MP4 and MN4) are V0 and V1 which are clock and input logic dependent respectively.

Body terminal of all PMOS transistors are connected to Vdd and Body terminal of all NMOS transistors are connected to Gnd. When the clock signal is low, then V0 should be 0 (low) so that MP1 and MP4 is turn on and the DOIND logic circuit comes in precharge phase. During precharge phase, the node N1 is charged to Vdd through MP1and MP4. Vout of the circuit is low which turn on the keeper transistor (MP2). When the clock signal is high, the circuit enters into the evaluation phase. In evaluation phase, when input Vin = 1

(high) then V1 should be 1 so that dynamic node N1 becomes 0 and when input Vin = 0 (low) then V1 should be 0 so that dynamic node N1 becomes 1. Operating status of each transistor is given in table

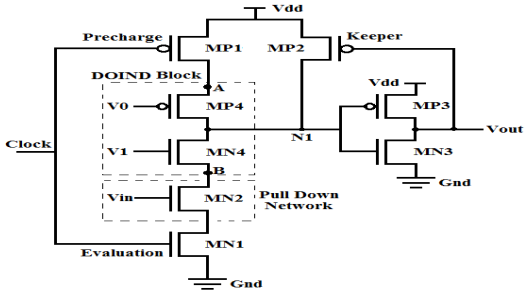

Fig.2: DOIND Logic circuit based buffer

3) Adopting body biasing DOIND logic

In this chapter we proposed DOINDAB (**Do**mino logic with Clock and **IN**put **D**ependent transistor with **A**ctive **B**ody Biasing) ABC1. For the static circuit's body of SOI partially Depleted MOSFET biased to control the threshold dynamically. Operation limited to V_{dd}= 0.7 V. [2].

3.1: DOIND-1 Technique

A standard proposed DOIND-1 logic circuit is shown in fig. 4. It has two DOIND transistors MP4 (PMOS) and MN4 (NMOS) connected between A and B. Gate terminal of DOIND transistors (MP4 and MN4) are V0 and V1 which are clock and input logic dependent respectively. Body biasing MP5 (PMOS) has placed in the transistor MP4(PMOS) and Body Biasing MN5 (NMOS) set to the Transistor MN4(CMOS). Body terminal of all PMOS transistors are connected to Vdd and Body terminal of all NMOS transistors are connected to Gnd.

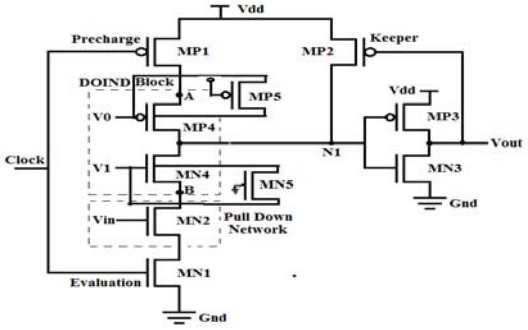

Fig: 4: DOIND-1 Logic circuit

The working operation of DOIND-1 logic circuit is in the following manner .When the clock signal is low, and then V0 should be 0 (low) so that MP1, MP4 and MP5 is turn on and the DOIND logic circuit comes in precharge phase. During precharge phase, the node N1 is charged to Vdd through MP1, MP4 and MP5. Vout of the circuit is low which turn on the keeper transistor (MP2). When the clock signal is high, the circuit enters into the evaluation phase. In evaluation phase, when input Vin = 1 (high) then V1 should be 1 so that dynamic node N1 becomes 0 and when input Vin = 0 (low) then V1 should be 0 so that dynamic node N1 becomes 1. Operating status of each transistor is given in table.

Table: 4.1: Operational Table of DOIND-1 Logic:

Clock	M N1	M P1	Input (Vin)	M N2	MP 2
Logic 0	OF F	ON	Logic 0	OF F	ON
Logic 0	OF F	ON	Logic 1	O N	ON
Logic 1	ON	OFF	Logic 0	OF F	ON
Logic 1	ON	OFF	Logic 1	O N	OF F

(a) Operational Table of DOIND-1 Logic:

Clock	MN4	MP4	Input (Vin)	MN5	MP5
Logic 0	OFF	ON	Logic 0	OFF	ON
Logic 0	OFF	ON	Logic 1	OFF	ON
Logic 1	OFF	OFF	Logic 0	OFF	OFF
Logic 1	ON	OFF	Logic 1	ON	OFF

(b) Operational Table of DOIND-1 Logic

When clock signal going to low with input pulse 0 , PMOS Transistor MP1, MP4, MP5 and keeper transistor MP2 turned ON and transistor NMOS MN1, MN2, MN4 and MN45 going to Evaluation phase . When clock signal getting a logic 0 with input pulse 1 , the transistor MP1 ,MP2, MP3 and MN2 going to ON and Transistor MN1 and MN4 is turned OFF.

4.5.1 Impact on Leakage Current

High leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications.

Relation between leakage current and threshold voltage is given by,

$I_{Leakage} = I_0 \frac{(Vgs-Vth)}{\eta Vt}(1-\exp\frac{-Vds}{Vt})$

Where I_0 is saturation current, Vgs is gate to source voltage, V_t is drain to source voltage and η is subthreshold slope factor.

Table 4.5.impact on leakage current

logic design	Clk =0, Vin =0	Clk =0 Vin =1	Clk =1 Vin =0	Clk =1, Vin =1	Improve In %
Domino	0.307	1.595	2.262	2.126	
DOIND	0.160	0.307	0.127	0.2587	86%
DOIND-B	0.166	0.322	0.322	0.2644	83%
DOIND-1	0.160	0.307	0.306	0.2594	84%

Graph clearly indicate that DOIND logic show better performance approx 86% in compare to

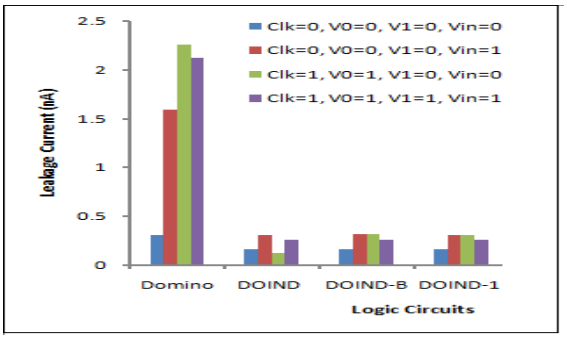

Fig.8: Leakage current for clock=0 and clock=1

Domino Logic but DOIND-1 also give 84% better scaling the leakage current than Domino Logic circuit.

4.5.2 Impact on Static Power

Table 4.6 shows that DOIND logic circuits has better in static power control with different input logic and with both clock=0 and clock=1. DOIND logic 86% better improvement than Domino logic but DOIND-B also 83% better than Domino logic. DOIND-1 achieve 84% gain to control static power than Domino logic circuits.

Table 4.6: static power depends on Clock input and input voltage.

logic design	Clk=0, Vin=0	Clk=0, Vin=1	Clk=1Vin=0	Clk=1 Vin=1	% impr
Domino	0.2763	1.4356	2.036	1.913	
DOIND	0.1448	0.2762	0.115	0.232	86%
DOIND-B	0.1499	0.2901	0.290	0.237	83%
DOIND-1	0.1448	0.2762	0.276	0.233	84%

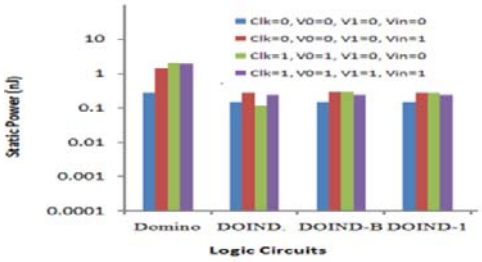

Fig.9: Static power for clock=0 and clock=1

4.5.3 Impact on Static Energy

Static energy element is directly proportional to Vdd so static energy is represented as

$$E_{Static} = I_{Leakage} V_{dd} T_{delay}$$

Where $I_{Leakage}$ is leakage current and T_{delay} is circuit delay.

DOIND-1 control the static Energy at 50MHz, 5MHz, 500KHz and 50KHz approximate 38%, 98%, 98% and 97% than Domino logic circuits.

4.5.4 Impact on Static PDP

Static power delay product (PDP) is given by

$$PDP_{static} = E_{static} \times T_{delay}$$

DOIND logic have79% better performance at the 50MHz but on remaining frequency at 5MHz, 500KHz and 50KHz DOIND-1 98%, 98% and 97% better than other all logic circuits.

4.5.6 Impact on Delay

In most designs there will be many logic paths that do not require any conscious effort when it comes to speed. However, usually there will be a number of paths, called the critical paths that require attention to timing details. These can be recognized by experience or timing simulation, but most designers use a timing analyzer, which is a design tool that automatically finds the slowest paths in a logic design.

Table; 4.10: Delay at different clock frequency

Logic design	Clock frequency			
	50MHZ	**% improve**	**5MHZ**	**% improve**
Domino	**65.68**		**111.6905**	
DOIND.	99.5	-51%	102.5	8%
DOIND-B	137.87	-110%	138.037	-24%
DOIND-1	245.787	-274%	10.78	90%
Logic design	Clock frequency			
	500KHZ	% improve	50KHZ	% improve
Domino	111.6905		110	
DOIND.	104.4	7%	104.5	5%
DOIND-B	127.1756	-14%	127.592	-16%
DOIND-1	10.65	90%	20	82%

All the logic have poor performance at the 50MHz frequency, at the remaining frequencies 5MHz, 500KHz and 50Khz DOIND-1 gives a 90%, 90%, and 82% better improvement than Domino logic

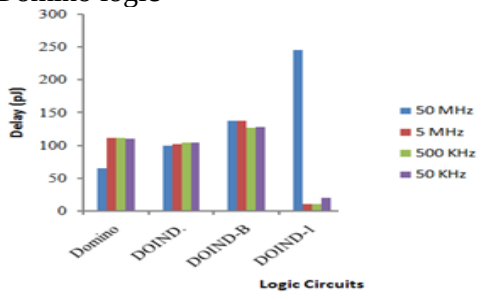

Fig.10: Delay at different clock frequency

IV.SIMULATION RESULT

The EDA tanner is used for study of different parameter for domino logic, DOIND, DOIND-B and DOIND-1 approach with supply voltage 0.9V.

V.CONCLUSION AND FUTURE SCOPE

At lower technology node in VLSI design, Leakage power dissipation becomes major concern. Leakage current drain out the battery of portable device even when the circuit is in idle mode and in reset unnecessary power consumption without operating the device. This chapter present the contribution of the work and future scope of the technology.

This paper work focus mainly towards different adoptive body biased technology for DOIND approach. Proposed DOIND-1 has maximum average improvement in leakage current of 84% among all other circuits. All the circuits have been analyzed at four different clock frequency 50MHz, 5MHz, 500 KHz and 50 KHz respectively.

Static Energy, static power delay product (PDP) , dynamic power, dynamic EDP and dynamic PDP of all the circuits are analyzed at all four frequencies.

Many parameters proposed adoptive body biased DOIND approach has been analyzed but some future work can also be done. Future aspects are given as follows:-

(a) All the simulation is performed at 70nm technology node. Simulation of all the circuits at other technology node can be done and check the performance of the circuit. Effect of the temperature variation can also be analyzed for the circuits.

(b) Layout of the circuits can also be calculated.

(c) Unity Noise gain and figure of merit can also calculated for the circuits so that novelty of the circuit can be analyze.

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