COMPARATIVE ANALYSIS OF CAPACITOR CLAMPED MULTILEVEL INVERTER WITH AND WITHOUT FILTER USING THREE LEVEL SPACE VECTOR PULSE WIDTH MODULATION

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Abstract
Multilevel inverters are the preferred choice in industry for the application in high voltage and high power applications. Multilevel inverters has advantages over two level inverters like minimum harmonic distortion, reduced EMI/RFI generation, and operation on several voltage levels. This paper presents the analysis and comparison of a conventional three level Capacitor Clamped (CCM) multilevel inverter using three level Space Vector Pulse Width Modulation (SVPWM) and Sinusoidal Pulse Width Modulation (SPWM). For the two switching techniques simulations are carried out with and without filter. FFT analysis has been conducted to obtain the Total Harmonic Distortion (THD) for both SVPWM and SPWM outputs. The simulations are performed using MATLAB/SIMULINK software and the results are presented.

Keywords: Capacitor Clamped Multilevel Inverter CCI, Space Vector Pulse Width Modulation, Sinusoidal Pulse Width Modulation, Total Harmonic Distortion.

1. INTRODUCTION

When ac loads are fed through inverters it required that the output voltage of desired magnitude and frequency be achieved. A variable output voltage can be obtained by varying the input dc voltage and maintaining the gain of the inverter constant. If the dc input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse-width-modulation (PWM) control within the inverter [1].

The inverter which produce an output voltage oftwo levels areknown as two level inverters. In high-power and high-voltage applications these two-level inverters however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and a machine drive for sinusoidal and trapezoidal current applications. This is where multilevel inverters are advantageous. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices can increase power rating [2]. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronizedswitching devices. The harmonic content of the output voltage waveform decreases significantly.

2. CAPACITOR CLAMPED MULTILEVEL INVERTER

The structure of this inverter is similar to that of the diode clamped inverter. Instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the capacitor clamped multilevel inverter is shown in Figure 1. This topology has a ladder structure of DC side capacitors. The voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. One advantage of the capacitor clamped multilevel based inverter is that it has

redundancies for inner voltage levels [2]-[5]. Unlike the diode clamped inverter, the capacitor clamped multilevel inverter does not require all of the switches that are ON (conducting) in a consecutive series. Moreover, the capacitor clamped multilevel inverter has phase redundancies, whereas the diode clamped inverter has only line-line redundancies. These redundancies allow a choice of charging and discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states which make up the level S_a.= 1. Considering the direction of the a-phase capacitor clamped multilevel current i_{ac1} for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. In Table 1, the current i_{adc} is the a-phase component of the dc current [6]. The total dc current can be calculated by summing the components for all phases. As with the three-level capacitor clamped multilevel inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states that both capacitors can be regulated to their ideal voltages [7]-[9].

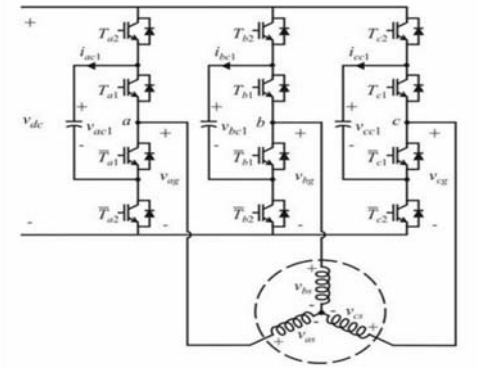

Fig.1 Three level capacitor clamped multilevel inverter.

S_a	T_{a2}	T_{a1}	V_{ag}	Iac1	Iadc1
0	0	0	0	0	0
1	0	1	Vac1	$-I_{as}$	0
1	1	0	Vdc –Vac1	I_{as}	I_{as}
2	1	1	V_{dc}	0	I_{as}

Table 1 Switching of one leg of FCI

3. THREE LEVEL SVPWM

Space vector pulse width modulation is quite different from the other PWM methods. With PWMs, the inverter can be thought of as three separate push-pull driver stages which create each phase waveform independently. SVM however treats the inverter as a single unit. Specifically the inverter can be driven to eight unique states. Modulation is accomplished by switching the state of inverter [8]-[10].

In α-β coordinate axis, the space vectors corresponding to the 27 working states are shown in Fig.3. Due to the redundancy states the 27 switching states are really corresponding to 19 different space vectors. And they separate Fig.2 into 6 sectors A, B, C, D, E, F with 4 equilateral triangles in each sector. Fig.3 shows that through the calculations of the amplitude and phase angle, where the referred vectors locate can be decided [11]-[13]. For their symmetry, here only gives an example of sector A to describe how the referred ones integrated by basic vectors. No matter where

*V*ref is, it can be expressed by

$$Vref\ Ts=(T_1V_1+T_2V_2+T_3V_3) \quad (1)$$

$$T_1+T_2+T_3=T_s \quad (2)$$

where

V_1, V_2, V_3 - vectors that define the triangle region in which Vref is located.

T_1,T_2,T_3 – corresponding vector durations.

Ts - sampling time.

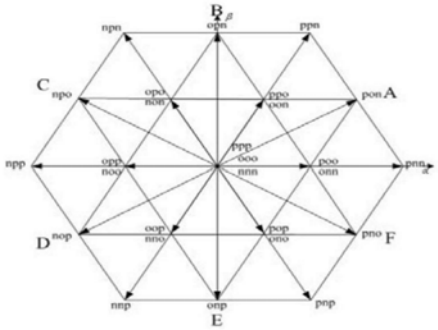

Fig.2 The space vectors corresponding to the 27 working state

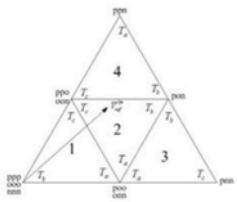

Fig.3 The integration of *V*ref

Of all the 19 basic space vectors, there is one phase connected with zero curves at least except

long vectors, and forms the closed circuit with the plus or minus. As a result, the capacitors charge and discharge frequently, which causes the ripple of the neutral voltage. To make sure that the three-level circuit working under the normal condition, it is necessary to control the neutral voltage ripples acceptable. So it needs to consider about the influences reacting on it. The redundant small vectors separately exert plus and minus offset on the neutral voltage. For this reason, their acting time can be adjusted to keep the balance of the neutral voltages [14]-[16].

4. SINUSOIDAL PWM

This is a very simple technique for harmonic reduction. In this technique pulse magnitude will be constant and only pulse width can be changed. In this pure sine wave is compared with carrier wave and producing gate pulses.

Sine wave has fundamental frequency and carrier wave can be taken morethan fundamental frequency Fig 4 shows Sinusoidal Pulse Width Modulation.Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave [17].

In the modulation techniques, there are two important parameters: frequency ratio,P = ω_c/ω_m modulation index $M_a = A_m/A_c$ where ω_c- reference frequency ω_m - carrier frequency A_m - reference signal amplitude A_C - carrier signal amplitude.
In this method of modulation, several pulses per half-cycle are used. Instead of maintaining the width of all pulses, the width of each pulse is varied proportional to the amplitude of a sin-wave evaluated at the centre of the same pulse [18]. By comparing a sinusoidal reference signal with a triangular carrier wave, the gating signals are generated.

The frequency of reference signal determine the inverter output frequency and its peak amplitude, controls the modulation index, M, and then in turn the RMS output voltage the more common carrier technique, the conventional sinusoidal pulse width Modulation technique, which is based on the principle of comparing a triangular carrier signal with a sinusoidal reference waveform (natural sampling).The Fig.4 below shows the sinusoidal pulse width modulation for three level inverter [19].

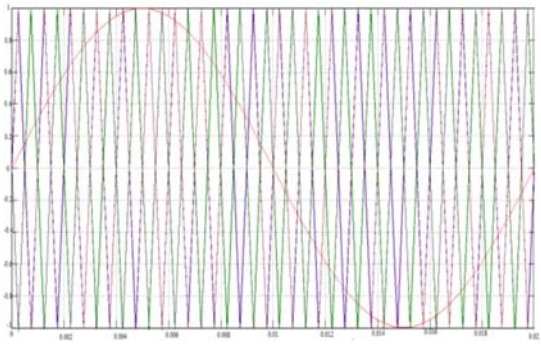

Fig. 4 Sinusoidal Pulse Width Modulation for three level inverter

5. FILTER DESIGN

A filter is required to obtain an approximate sine wave for the load, since the output of multilevel inverter is not sinusoidal. The filter is designed as per the equation:

$fc=\sqrt{fr.fs}$ (3)

f_c- corner frequency f_r-reference frequency
f_s-switching frequency

$fc=\frac{1}{2\pi\sqrt{LC}}$ (4)

6. RESULTS AND DISCUSSIONS

Comparison of SVPWM and SPWM fed three level capacitor clamped multilevel inverter with and without filter has been done using MATLAB/SIMULINK. The input for inverter is taken as 500 V. The switching of inverter was done by using both SVPWM and SPWM and total harmonic distortion was taken for both output voltage. Table 2 shows the simulation parameters.

Parameters	Value
V_{dc}	500V
Switching Frequency	10kHz
R_{load}	1Ω
Lload	1mH
Cfilter	10 μF
Lfilter	5mH

Table 2 Simulation parameters

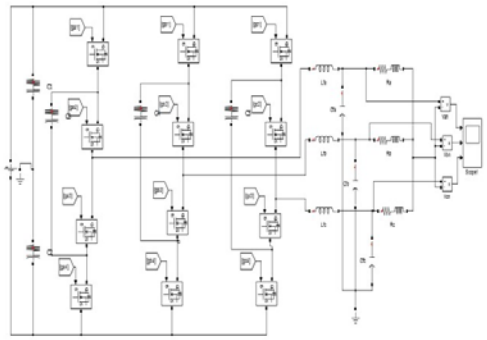

Fig 5 SPWM fed CCM

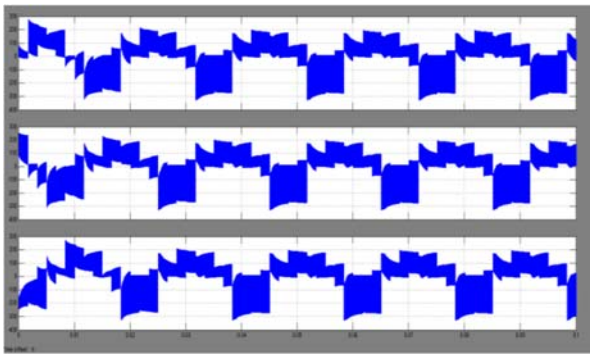

Fig. 6 SPWM fed inverter output phase voltage without filter

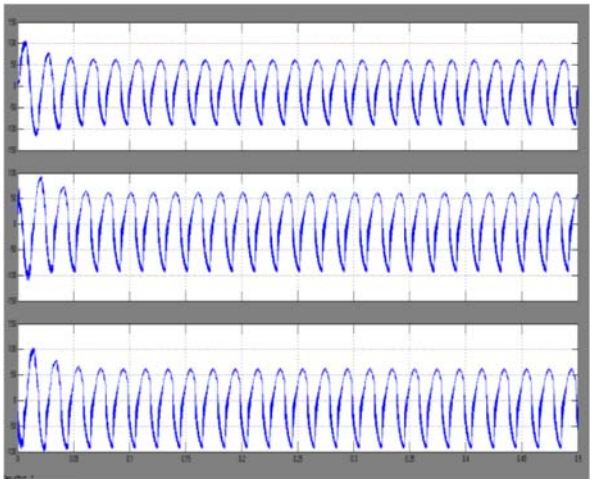

Fig. 7 SPWM fed inverter output phase voltage with filter

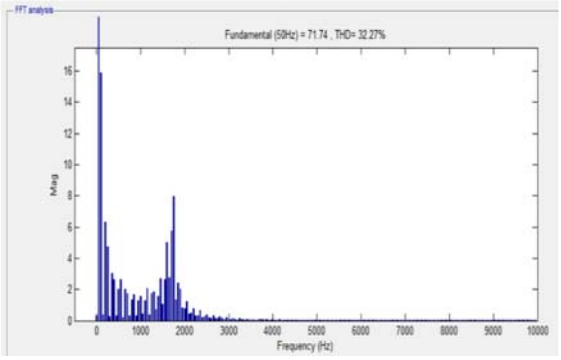

Fig. 8 FFT analysis of SPWM fed CCM output phase voltage

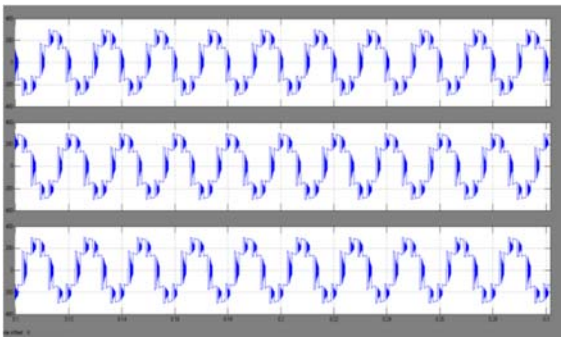

Fig. 9 SVPWM fed inverter output phase voltage without filter

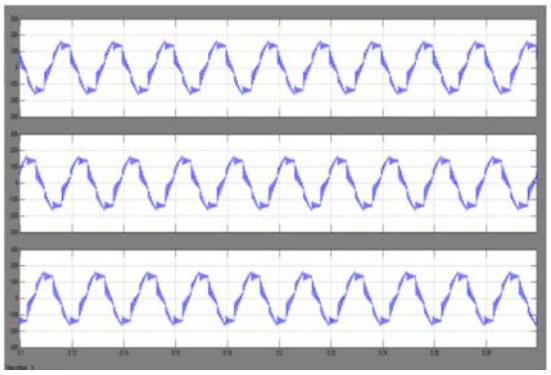

Fig. 10 SVPWM fed inverter output phase voltage with filter

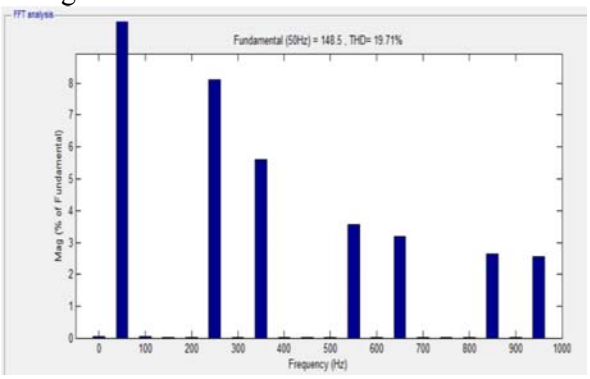

Fig. 11 FFT analysis of SVPWM fed CCM output phase voltage

The Fig.5 shows the Simulation of CCM. Fig.6 shows the output phase voltage of SPWM fed CCM inverter without filter and Fig.7 shows the output phase voltage of SPWM fed CCM inverter with filter. Fig.8 shows the FFT analysis of SPWM fed CCM inverter and from this it is clear that a THD of 32.27% and Fig.9 shows the output phase voltage of SVPWM fed FCI inverter without filter and Fig.10 shows the output phase voltage of SVPWM fed CCM inverter with filter.Fig.11 shows the FFT analysis of SVPWM fed CCM inverter and it shows THD as 19.71%.

REFERENCES

[1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevelvoltage-source-converter topologies for industrial medium-voltage drives", *IEEE Transactions on Industrial Electronics,* vol. 54, no. 6, pp.29302945,July 2007.

[2] Akhila. A, Manju Ann Mathews, Nisha G .K, "Comparative Analysis of Capacitor clamped multilevel and Diode Clamped Multilevel Inverters Using SPWM," *International Journal of Innovative Science, Engineering and Technology(IJISET),* vol. 3, no.8, pp.387393,August 2016.

[3] Y. Zhang, Z. Zhao, "Study on capacitor voltage balance for multilevelinverter based on a fast SVM algorithm", Proceeding of the CSEE(inChinese), vol. 26, no. 18, pp. 71-76, May 2006.

[4] G. K. Nisha, S. Ushakumari and Z. V. Lakaparampil "CFT Based Optimal PWM Strategy for Three Phase Inverter," *IEEE International conference on Power, Control and Embedded Systems (ICPCES'12),* Allahabad, India,pp. 1-6, 17-19 December 2012.

[5] A Gupta, A. M. Khambadkone, "A space vector PWM scheme formultilevel inverters based on two-level space vector PWM*", IEEE Transactions on Industrial Electronics,* vol. 53, no. 5, pp. 1631–1639, February 2006.

[6] G. K. Nisha, S. Ushakumari and Z. V. Lakaparampil "Online Harmonic Elimination of SVPWM for Three Phase Inverter and a Systematic Method for Practical Implementation," *IAENG International Journal of Computer Science,* vol. 39, no. 2, pp. 220-230, May 2012

[7] . A. Sapin, P. K. Steamer, J. J. Simond, " Modeling simulation and test of a three-level voltage-sourceinverter with output LC filter and directtorque control", *IEEE Transactions on Industry Applications,* vol. 43, no. 2, pp.469-475,April 2007.

[8] G. K. Nisha, S. Ushakumari and Z. V. Lakaparampil "Harmonic Elimination of Space Vector Modulated Three Phase Inverter," *Lecture Notes in Engineering and Computer Science: Proceedings of the International Multi-conference of Engineers and Computer Scientists, (IMECS 2012),* Hong Kong, pp.1109-1115, 14-16 March 2012.

[9] L. Dalessandro, S. D. Round, J. W. Kolar,"Center-point voltagebalancing of hysteresis current controlled threelevel PWM rectifiers",*IEEE Transactions on Power Electronics,* vol. 23, no. 5, pp. 2477-2488, September 2008.

[10] Akhila.A, Lekshmi.K.R, Nisha .G.K, "Analysis and Comparison of Capacitor clamped multilevel and Modular Multilevel Converters Using SPWM,"International Journal of Innovative Research and AdvancedStudies (IJIRAS),vol.3, no.8, pp.352-357,July. 2016.

[11] G. K. Nisha, Z. V. Lakaparampil and S. Ushakumari, "Performance Study of Field Oriented Controlled Induction Machine in Field Weakening using SPWM and SVM fed Inverters," *International Review of Modeling and Simulations,* vol. 6, no. 3, pp. 741-752, June 2013.

[12] Jih-Sheng Lai, Fang Zheng Peng, "Multilevel Converters a New Breed of Power Converters," *IEEE Transaction on Industrial Applications,* vol. 32, no. 3, pp. 509-517,May/June 1996.

[13] Jose Rodriguez, Leopoldo.G. Franquelo, Samir Kouro, Jose.I .Leon, Ramon .C.Portil "Multilevel Converters an Enabling Technology for High power Applications,"*IEEE Transaction on Industrial Applications,* vol. 97, no. 11, pp. 1786-1816, November 2009.

[14] G. K. Nisha, Z. V. Lakaparampil and S. Ushakumari, " FFT Analysis for Field Oriented Control of SPWM and SVPWM Inverter fed Induction Machine with and without Sensor," *International journal of Advanced Electrical Engineering,* vol. 2, no. 4, pp. 151-160, June 2013.

[15] G. K. Nisha, S. Ushakumari and Z. V. Lakaparampil "Method to Eliminate Harmonics in PWM: A Study for Single Phase and Three Phase," *International conference on Emerging Technology, Trends on Advanced Engineering Research,* Kollam, India, pp. 598-604, 20-21 February 2012.

[16] Kalle Ilves, Antonios Antonopoulos, Staffan Norrga, Hans-Peter Nee, "A New

Modulation method for the Modular Multilevel Converter Allowing Fundamental Switching frequency," *IEEE Transaction on Industrial Applications,* vol. 27, no. 8, pp. 3482-3494,August 2012.

[17] G. K. Nisha, Z. V. Lakaparampil and S. Ushakumari, "FFT Analysis for Field Oriented Control of SPWM and SVPWM Inverter fed Induction Machine with and without Sensor," *International conference on Advance Engineering Technology(ICAET'13),* Mysore, India, pp. 34-43, 27 January 2013.

[18] Akhila A, Nisha G .K, "Comparative Analysis of Capacitor clamped multilevel and Cascaded Multilevel Inverters Using SPWM," *International Journal of Engineering Trends and Technology,*vol.4,.no.1,pp.610,October 2016.

[19] Tolbert. L. M and Pend. F. Z, "Multilevel Converter as a Utility Interface for Renewable Energy Systems," IEEE Power Engineering Society Meeting, vol. 2, pp. 1271-1274, March 2000.

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