DESIGN & PERFORMANCE ANALYSIS OF 16 BIT RAM USING QCA TECHNOLOGY

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Abstract
Quantum dot Cellular Automata (QCA) is a smart technology to implement computing architectures at nano scale. QCA circuits require low power for their working along with the potential for high density and reliability. By following a set of simple design rules, capricious circuits can be made using QCA cells. The enthusiasm behind this paper is to design and simulate a novel 16 bits random access memory architecture having real volatile nature. This paper proposes a 16 bit random access memory (RAM) using QCA technology. The RAM is implemented using five and seven input majority gate in QCA Designer v2.3.0. In addition, the problem of overwriting the data in all memory cells by the selection of individual single memory cell is also solved in this paper by applying erasure feature in the predesigned circuit. The result shows that the proposed 16 bit RAM have number of advantages in terms of latency, area needs for circuit (size of integrating circuit), power consumption and complexity level to a traditional RAM in uses.

Keywords: Quantum dot cellular automata (QCA), Nanotechnology, QCA cell, RAM, Memory cell, Majority gate

I. Introduction

Using CMOS technology, memory was designed traditionally which gave the need of an approach to increase the capacity of memory. CMOS technology will approach to physical limit in next ten decade. So power consumption will be main problem in CMOS technology. To remove this problem QCA is used. QCA is a technology with low power consumption, very high density and fast operational speed, and also offers a new method of computation and information transfer. Interconnections for signal transferring are used for logic computation [2].

In QCA logic states are not stored as voltage levels, but rather the position of individual electrons. The basic elements of QCA are QCA cell, Majority gate and inverter. A QCA cell can be viewed as a set of four “dots” that are positioned at the corners of a square [7]. A quantum dot is a site in a cell in which a charge can be localized. The cell contains two extra mobile electrons that can quantum mechanically and tunnel between dots, but not cells. QCA cell works on columbic interaction of electronics between the cells [10]. The locations of the electrons determine the binary states. Fig.1 (a), Fig.1 (b) and Fig.1 (c) shows the QCA cell diagrams.

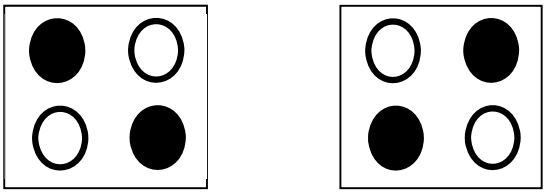

Fig. 1- (a) QCA cell with polarization"-1" for the binary “0” logic level; (b) QCA cell with polarization "+1" for the binary “1” logic level

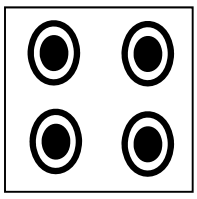

Fig.1(c): QCA cell with polarization "0"; for the binary “0” logic level

Memory has been designed in QCA owing to the advantages of latency, complexity as compared to CMOS technology.

Various memories in QCA have unique characteristics due to their architectural structure. In this paper, memory is designed using five and seven input majority gate to remove the problem of volatile nature of already designed memory. This new QCA memories exploit the features of the memory-in motion paradigm. The paper is organized as follows: Section II provides a literature survey on QCA memories, while Section III provides the proposed memory cell. Section IV introduces a novel design 16 bit RAM approach that utilizes a new clocking scheme for compact and efficient design of serial and parallel memories. Finally in section V a comparative analysis is pursued; the different architectures are analyzed using various figures of merit as well as the desired application requirements. Conclusions are also drawn.

II. LITERATURE SURVEY

A Quantum Cellular Automaton (QCA) is a nanotechnology which is an attractive alternative for transistor based technologies in the near future. Arithmetic structures based on quantum cellular automata (QCA) was discussed in paper[8]. A new five and seven input majority gate in quantum dot cellular automata is designed. To reduce cell count, latency and complexity four inputs AND gate and OR gate in only two clock phases 3 using seven input majority gate [8]. By applying these kinds of gates QCA circuits could be simplified and optimized.

Various authors have worked on QCA memory. In 2003 memory was designed using QCA technology in which each memory cell consists of 158 cell. Since the design consists of a simple two dimentional grid structure, an n-bit memory would have O(n) cells. Spacing of QCA cells was taken 10nm, then the design has a storage capacity. Ottavi and other authors have implemented a memory with parallel read/serial write in 2005. This architecture combines the advantage of reduced area of a serial memory with the reduced latency in the read operation of a parallel memory [3].

Vankamamidi has given a novel parallel memory architecture in 2006 which is amenable to QCA implementation and it uses Line Based Memory. Line based memory is the memory cell in which storage is achieved by moving data back and forth along a line of QCA cells [4]. This architecture results in substantial savings in the number of clock zones and underlying circuitry's complexity for clocking the QCA memory [4].

In 2008, a memory was designed in which clocking zones are shared between memory cells and the length of the QCA line of a clocking zone which is independent of the word size [5]. QCA circuits for address decoding and input/output for simplification of the Read/Write operations were also discussed. An comparison of this memory architecture and previous QCA serial memories was discussed in terms of latency, timing, clocking requirements, and hardware complexity.

In 2012, two types of memory were designed. One is parallel memory and other is serial memory cell. Parallel memory was designed using multiplexer, AND logic gates. In serial memory, number of clock zones is four times the number of cells used in feedback loops [6].

In 2012, a memory was designed in which each memory cell has minimum number of cells and designed with five logic operations and act as a pipeline[1].

All work proposed by different researches consider three input majority gate, none were taken five and seven input majority gate. Therefore this paper consider the five and seven input majority gates to compared its performance with the following objectives

1. To reduce latency
2. Miniaturization size
3. Reduce complexity

III. PROPOSED MEMORY CELL

Memory cell is a collection of storage cells together with the necessary circuits to transfer information to and from them.

Here the previous memory cell and its problem also is discussed that was designed in paper [1]. This architecture of memory has different features, such as number of bits stored in a loop, access type (serial or parallel) and cell arrangement for the memory bank. The parallel architecture is similar to CMOS based memory architecture and it is a conventional memory cell in this paper. It is unit memory cell to store 1-bit data only. The data bit is stored in a loop, until the WR/RD control signal is low. When Read

bar/Write is raised high, then the input bit is stored in the loop and data is written in the memory cell. When Read bar/ Write are low then the previous written data is read from the memory cell. The loop must be implemented using all zones of the four phase adiabatic switching technique for the clock, thus allowing the 'motion' of the stored bit. The right AND gate A3 is called an enable gate and operates independently from the remaining gate of the circuit. To read or write mode, the enable gate outputs the stored value when EN is '1'. This shows that the memory cell is selected to be read. Otherwise, when EN is '0', the output is '0', which means that the memory cell is not selected to be read. The basic memory cell (conventional) of this architecture is shown in

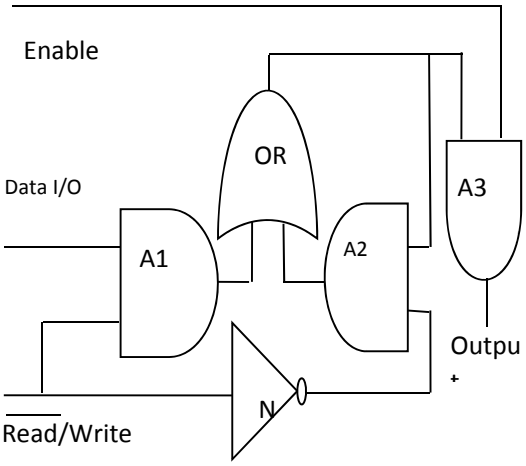

Fig.2- Basic conventional memory cell

It has four logic gates in which three AND gate, one OR gate and one inverter gate are used. And it has been designed in QCA designer with three input majority gate. It faces one problem, when we read the memory in next cycle after the enable "0" then output should be zero but output will be the previous data written in the memory. Other problem is created when 16 bit RAM designed with this memory cell. This problem is overwriting the data in all memory cell even when selection of one memory cell.

To remove the above discussed problem in the memory, the following memory is proposed.

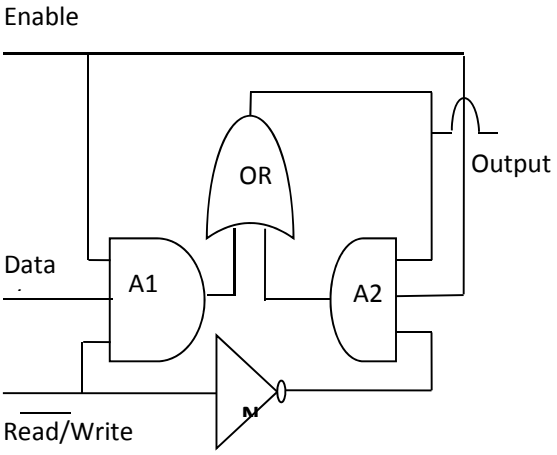

Fig. 3-Proposed memory cell

As shown in Fig. 3 it has four logical gates as two AND logic, one OR logic and one inverter. Here one logical AND gate is reduced so latency and complexity will be reduced. This proposed memory is designed in QCA Designer with new five input majority gate.

To read/write mode operation enable should be '1' otherwise output will be always zero. When the Read bar/write is high then data is written in the memory cell. And when Read bar/write is low then data is read out from the memory. In 16 bit RAM eight AND logic gates are reduced so latency will be reduced. Implementation and simulation of proposed memory cell are shown in Fig.4 and Fig.5.

A. Implementation of Proposed Memory cell

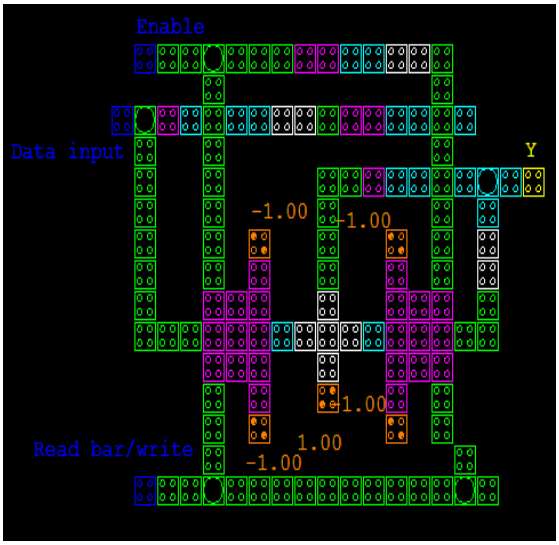

Fig.4. Implementation of Proposed Memory cell

A. *Simulation Result of Proposed Memory Cell*

Fig. 5- Simulation result of proposed memory cell

Table 1-Comparison table between conventional & proposed memory cell operation

Enable	Read/ Write	Data	Output of Conventional memory	Output Proposed Memory
0	x	x	0	0
1	1	D1	D1	D1
1	0	x	D1	D1
0	x	x	0	0
1	0	x	D1	0

Table1 shows the comparison between the read/write operation of conventional and proposed memory cell.

IV. SIXTEEN BITS RAM

In this section, to design 16 bit RAM the unit memory cells are arranged in a 16 bits array. To select any memory cell, output of decoder is connected to enable as shown in Figure 6. To activate any memory cell output of decoder should be one.

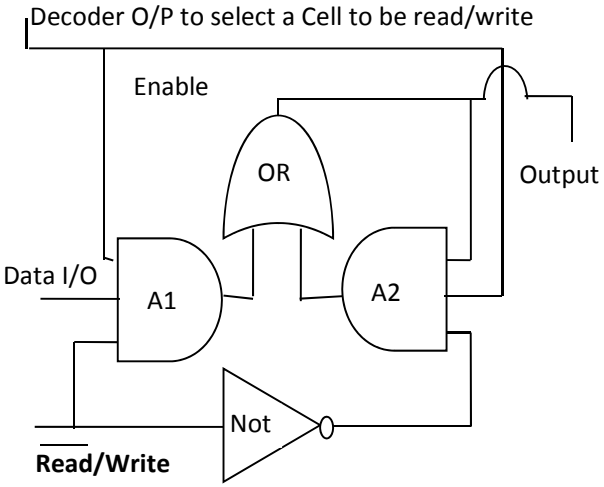

Fig.6. Selection of one memory cell through decoder

In Fig 7, the vertical decoder rails in extreme left column and row decoder rails are used to select the memory cell. The horizontal arrows represent the data input rails; the read/write enable rails and the OR chain rails [1].

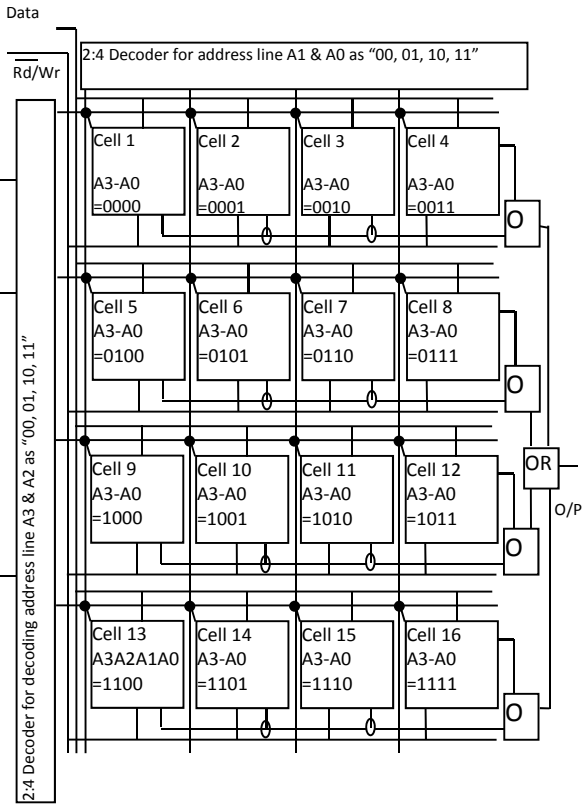

Fig.7- 16 bit RAM blocks representation using proposed memory cell

The 2-to-4 decoder in the first-stage uses eight 2-input AND gates in both column and row

decoders. One row and one column decoder is used to select any unit memory cell with minimum delay. The total latency from when the initial decoded address begins to when the output appears is seven clock cycles. At the bottom right of the RAM, there is the output of the RAM. It is the OR of the enabled outputs of all sixteen memory cells. The decoder ensures that only one memory cell is enabled. Thus, the output of the entire RAM is equal to the value stored in the enabled cell. Read/ write operation is shown in table 2.

Table 2- Read/write operation of 16 bit RAM using proposed memory cell

Address	W/R	Data input	Output
XXXX	1	D	D
XXXX	0	X	D
$X_1X_2X_3X_4$	1	D_1	D_1
$X_1X_2X_3X_5$	1	D_2	D_2
$X_1X_2X_3X_4$	0	X	0

But when we designed the 16- bit RAM with this proposed memory cell. Then there will some problem in the 16-bit memory as shown in above table of read/write operation. That problem is when write the data in one memory cell the data will be zero in all other memory cell. After that if we read any memory cell then the read data will be zero rather than the previous data written in memory cell. So when working on one memory cell using decoder then there should be no change in any other memory cell.

To remove the above discussed problem Read/Write is controlled by the decoder and one more Feature added in this memory which is Erasing signal as shown in Fig 8. Erasing signal is used to clear all memory cells. Using this signal RAM can be check whether it is empty or not

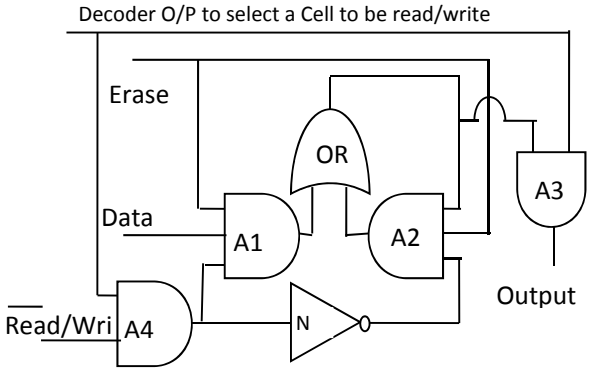

Fig. 8- 16 bit RAM blocks representation

Read/ write operation works till the Erase signal is one. Here four AND gate, one OR and one NOT gate are used. In QCA implementation two AND logic are designed with Five input majority gate and all other logic operations are designed with three input majority gate.

Now design of 16 bit RAM is shown in Figure 9 using above discussed memory cell which have volatile nature

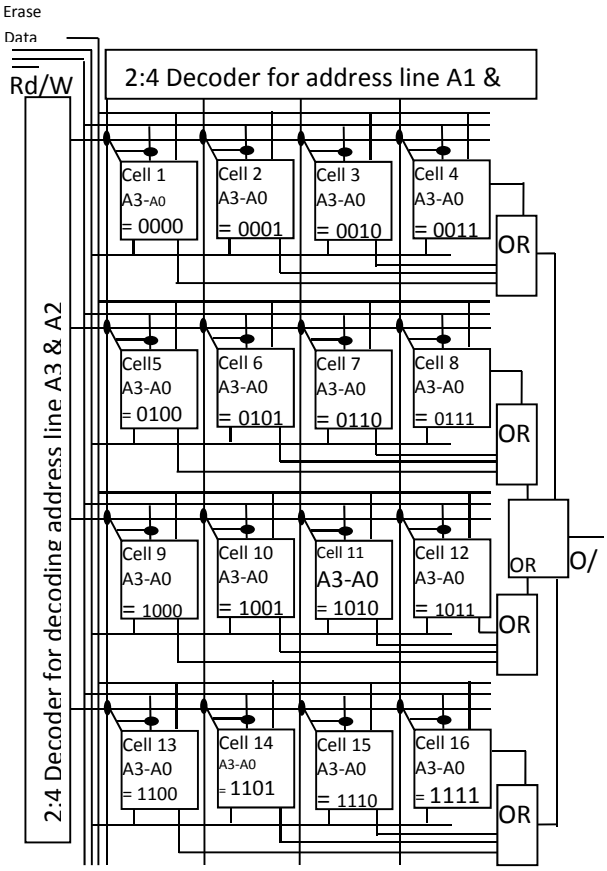

Fig.9. Block representation of 16 bit RAM memory having real volatile nature

Read/write operation of 16 bit RAM having volatile nature is shown in table3.

Table3-.Read/write operation of 16 Bit RAM having volatile nature

Address	Erase	W/R	Data input	Output
XXXX	0	X	X	0
XXXX	1	1	D	D
XXXX	1	0	X	D
$X_1X_2X_3X_4$	1	1	D_1	D_1
$X_1X_2X_3X_5$	1	1	D_2	D_2
$X_1X_2X_3X_4$	1	0	X	D_1

A. *Implementation of 16 bit RAM using Proposed modified conventional Memory cell*

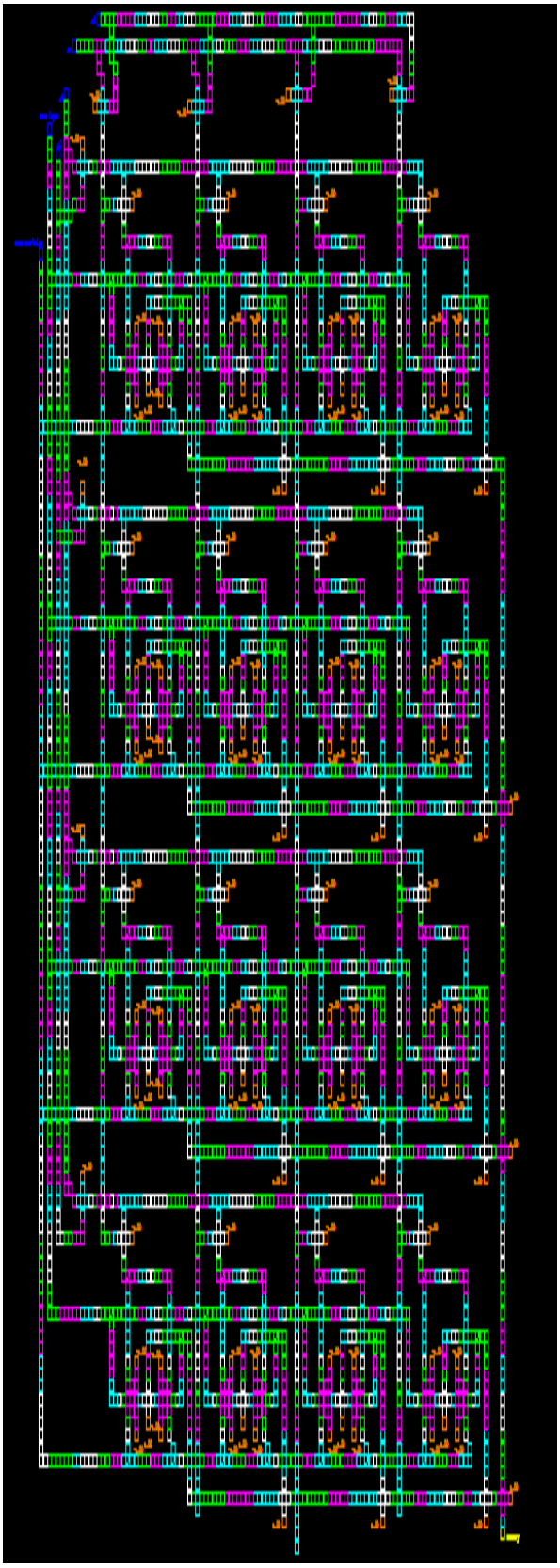

Fig. 10 -16 bit RAM memory implementation using proposed & modified memory cell

B. Implementation of 16 bit RAM using Proposed Memory cell Having volatile nature

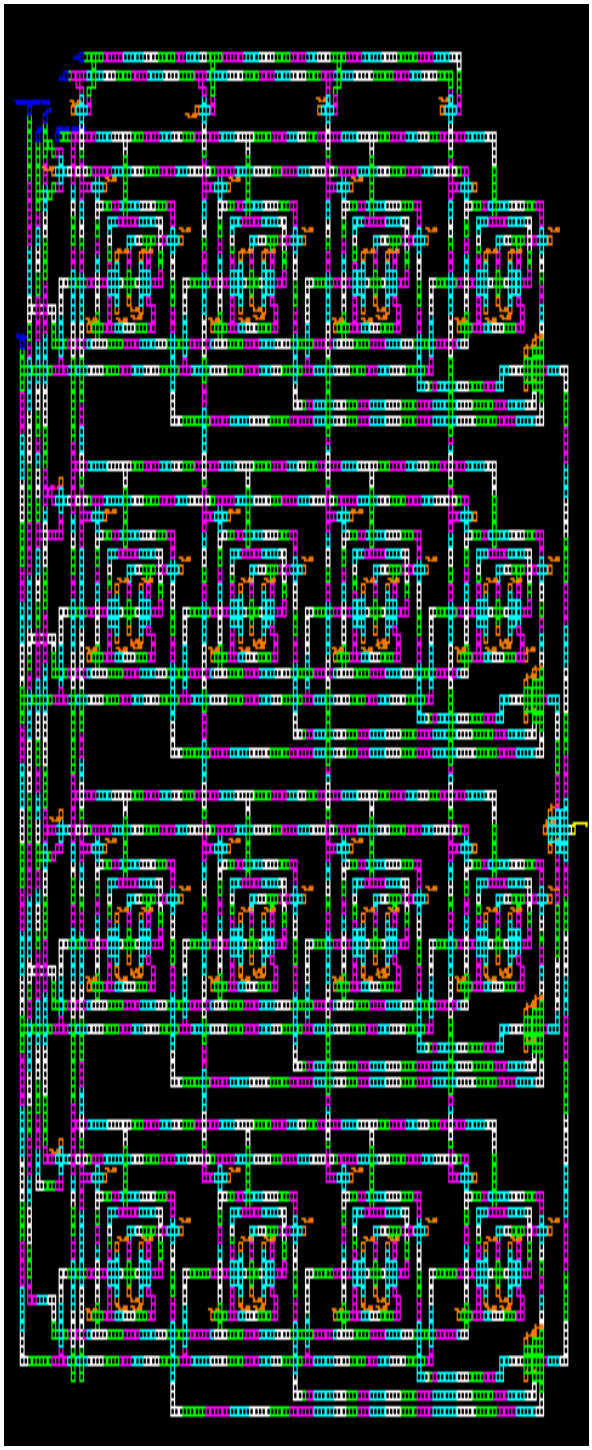

Fig.11. 16 bit RAM memory implementation using proposed & modified memory cell having erase feature

V. SIMULATION RESULTS

To implement and simulate the proposed 16 bit RAM, the software is QCA designer 2.0.3. Simulation parameters for one of the simulation method bistable approximation are given in table 4.

Table 4- Simulation parameters

Parameter	Value
Cell size	18nm
Temperature	1.000000k
Relaxation time	$1.000000e^{-015}$s
Time step	$1.000000e^{-016}$s
Total simulation	18s
Clock height	$9.800000e^{-022}$J
Clock low	$3.800000e^{-23}$J
Clock shift	$0.000000e^{000}$
Clock amplitude factor	2.000000
Radius of a factor	65.000000nm
Relative permittivity	12.900000
Layer separation	11.500000nm

Simulation results of 16 bit RAM using proposed memory and also having volatile nature of cell are shown in figures 12 and 13.

1. *Simulation result of 16 Bit RAM using Proposed Memory cell*

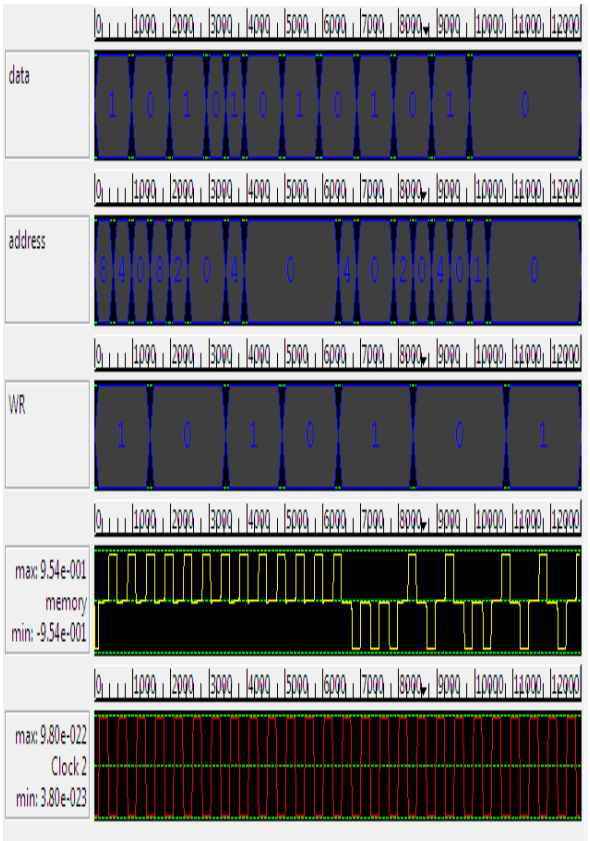

Fig. 12- Simulation of 16 bit RAM memory using proposed memory cell

2. *Simulation result of 16 Bit RAM using Proposed Memory cell having volatile nature*

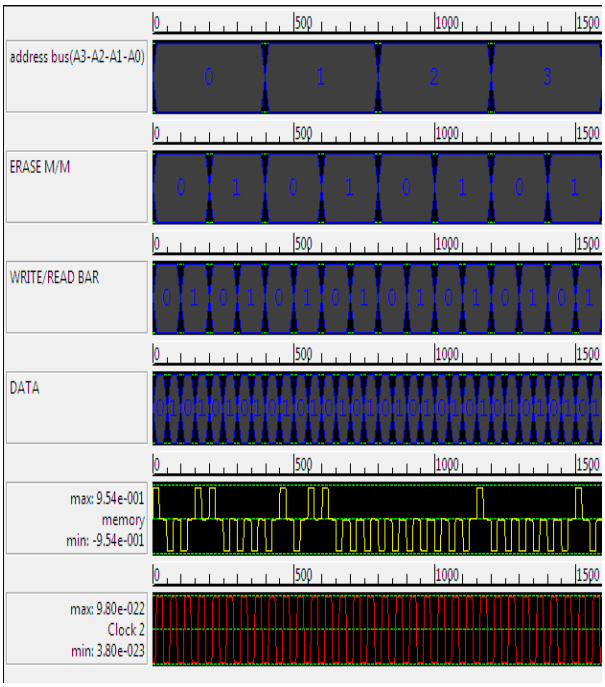

Fig.13. Simulation result of 16 bit RAM memory using proposed memory cell having volatile nature

A comparison among various parameter related to architecture and advantages-disadvantages of conventional 16 bit RAM and both proposed 16 bit RAM is shown in table 5.

Table.5. Comparison between the parameters of conventional and proposed 16 bit RAM

Type of Majority gate	Latency	Number of Cells	Complexity	Required Majority gate
Conventional 16 bit RAM	31 Clock cycle	445	High	88-three input Majority gate
16 Bit RAM with proposed memory cell	23 Clock cycle	4421	Low	32-five input,39-three input Majority gate
16Bit RAM with advanced proposed memory cell	27 Clock cycle	5980	Medium	5-seven,32-Five and 56-three input

VI. CONCLUSION

16 bits RAM designing is so easy now because of the five and seven input majority gate used in this paper. Overall latency, area and complexity of the circuit is reduces with less number of majority gates. Proposed memory architecture can be designed only in 27 clock zones even with additional feature of erasing signal. Further memory capacity can be increased as per requirement with promoting nine input majority gate.

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