REDUCED INTRICACY WALLACE MULTIPLIER USING ENERGY PROFICIENT FUSION CMOS FULL ADDER

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Abstract

A multiplier is one of the important hardware blocks in most digital and high performance systems such as microprocessors, FIR filter and digital signal processors etc. With improving in technology, many researchers have tried and are trying to design multipliers which offer high speed, low power consumption and less area. However area and speed are two most important constraints. So improving speed results always in larger area. So here we try to find out the best solution among the both of them. Wallace Tree Multiplier (WTM) is the fastest multiplier used in number of data-processing processors to perform fastest arithmetic function. From the structure of the RCWM Reduced Complexity Wallace Tree Multiplier, it is clear that there is scope of reducing the power consumption and area. This work uses an efficient and simple gate-level modification to significantly reduce the power and area of RWTM. Conventional WTM is still area-consuming due to the CMOS switching structure. The logic operations involved in conventional RCWM and WTM are analyzed to study the data dependence and to identify redundant logic operations. Reduced Complexity Wallace multiplier (RCWM) will have fewer adders than Standard Wallace multiplier (SWM) A Reduced Complexity Wallace multiplier presented in this paper is having the same delay as that of Standard Wallace multipliers. In both multipliers, at the last stage Carry Propagating Adder (CPA) is used. This paper proposes use of Energy Efficient HYBRID CMOS full adder in reduced complexity Wallace Multiplier at the place of Full adder of standard Wallace Multiplier in order to reduce Area, Power and improvement in speed. The Reduced complexity reduction method smartly reduces the number of half adders with 70-80% reduction in an area of half adders than standard Wallace multipliers.

Keywords: Energy Efficient HYBRID CMOS full adders, Wallace Multiplier, High speed multiplier, Reduced Complexity Wallace Tree Multiplier

I. INTRODUCTION

Multipliers are one the most important component of many systems. In high speed digital signal processing (DSP) and image processing multiplier play an vital role. In image processing fast Fourier transform (FFT) is one of the most important transform often used. A computational process of fast Fourier transform requires large number of multiplication and addition operation. The execution of these algorithms requires dedicated MAC and Arithmetic and Logic Unit (ALU) architectures. Multipliers and adders are the key element of these arithmetic units as they lie in the critical path. With the recent advances in technology, many researchers have tried to implement increasingly efficient multiplier. They aim at offering low power consumption, high speed and reduced delay. One such multiplier is Standard Wallace Multiplier (SWM) . SWM is fully parallel version of the multiplier, the carry save adders used in SWM are conventional full adders whose carries are not connected, so that three inputs are taken and two words are out. SWM also uses half adders in reduction phase. Reduced complexity Wallace multiplier (RCWM) reduced number of half adders used in SWM with a slight increase in full adders to reduce the

number of gates. Both the multipliers SWM and RCWM have same number of stages and delay is also same. This paper proposes use of Energy Efficient HYBRID CMOS full adder in reduced complexity Wallace multiplier at the place of carry propagating adder in order to reduce power and improvement in speed.

II. TRADITIONAL METHOD

A. Wallace Multiplier

A Wallace Multiplier is an easily hardware EFF multiplies two integers, proposed by an Australian Computer Scientist Chris Wallace. For unsigned multiplication, up to n shifted copies of the multiplicand are added to form the result. The entire procedure is carried out into three steps: partial product (PP) generation, partial product grouping & reduction, and final addition. The principle of Wallace tree multiplication . For an n x n multiplication there are n^2 partial products that have to be summed. The 1st step in the algorithm involves grouping the partial products into sets of 3. For example, if there are *n'* rows of partial products, 3*[n/3] rows are grouped and the remaining n mod 3 rows are passed to the next stage. Therefore three rows of partial products are grouped together in stage 1, These 3 rows are then sum using full adders and if there are 2 dots in particular column half adders are used. The resulting sum and carry signals from the half and full adders are passed to the next stage. The process is repeated till the entire n partial products are summed. The resulting sum and carry out of the last stage is added using a fast carry propagation adder at the final stage.

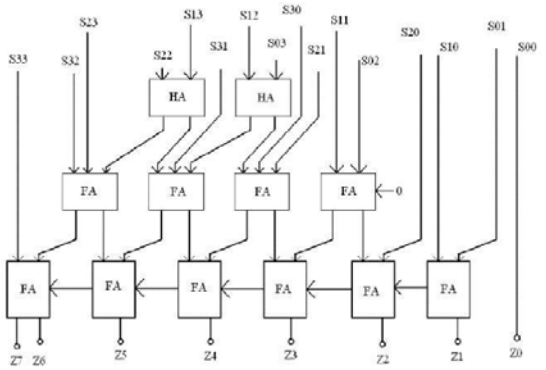

FIG: WALLACE MULTIPLIER

B. Reduced Complexcity Wallace Multiplier

Reduced complexity Wallace Multiplier (RCWM) is the modified version of Standard Wallace Multiplier (SWM). In SWM they use full adder and half adder in their reduction phase, but half adder do not reduced the number of partial bit therefore RCWM reduced the number of half adder used in the SWM with slightly increase in full adder . The partial products are formed by N^2 AND gates. The partial products are arranged in a Tree structure format. The modified Wallace reduction method divides the matrix into three row groups. Full adders are use for each group of three bits in a column like the Standard Wallace reduction. A two bits group in a column is not processed, so it is passed on to the next stage (in contrast to Standard Wallace method). Single bits are passed on to the next stage as in the Standard Wallace reduction. The only time half adders are used is to ensure that the number of stages does not exceed that of a Standard Wallace multiplier. For some cases, half adders are used in the final stage of reduction. In RCWM they use carry propagating adder (CPA) . One possible carry propagating adder for RCWM is a hybrid adder consisting of S+1 ripple carry half adder.

III. ENERGY EFFICIENT HYBRID CMOS FULL ADDER

A. Alternative logic Structure For a Full Adder

An Energy Efficient CMOS Full adder design using alternative logic scheme gives low power delay product (PDP), in terms of speed, power consumption and reduced Area in the cmos full adder logic.

Proposed full-adder is scrutinized by the full adder's truth table, it can be seen that sum signal can be generated as follows

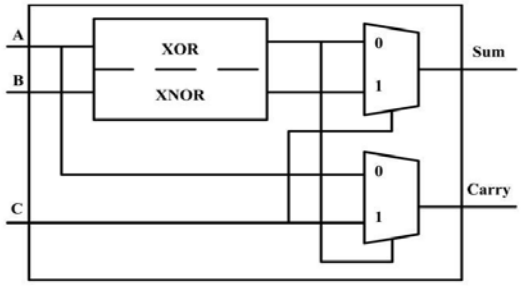

FIG:ENERGY EFFICIENT HYBRID CMOS FULL ADDER

And carry signal can be generated as signals, we use DPL logic style that helps to achieve the full voltage swings and better driving capabilities at internal nodes. The DPL style makes use of both parallel connections of NMOS, PMOS logic

networks. DPL provides the XOR and XNOR signals simultaneously thus intermediate signals can be generated with higher speeds. Two separate multiplexers are used to generate the sum and carry signals as shown in Figure 1. The multiplexer circuit used to generate the sum signal will be controlled by input signal C. The other multiplexer is controlled by the intermediate signals and will generate the carry signal. Each of this multiplexer functionality is achieved by using the transmission gate style as shown in Figure 2. The advantage of designing a multiplexer with transmission gate is that it can drive the large capacitive loads easily and can gain the complete voltage swings.An alternative logic scheme to design a full adder ce ll can be formed by a logic block to obtain the A+B and A + B signals , another block can be obtain the A × B and A + B signals, and two Multiplexers driven by the C input to generate S0 and C0 outputs as shown in fig 1. Full adder design using swing restore complementary Pass -Transistor logic (SR-CPL) style [4] build the AND/OR gates And XOR/XNOR gates, and multiplexer based on pass transistor to obtain S0 and C0 outputgroundless pass-transistor logic.Double-pass transistor logic eliminates some of the inverter stages required for complementary pass transistor logic by using both N and P transistors, with dual logic paths for every function. While it has high speed due to low input capacitance, it has only limited capacity to drive a load.

IV. PROPOSED SYSTEM

Proposed architecture has same stages as RCW Multiplier. At the stage where conventional full adder is present, Energy Efficient HYBRID CMOS Full Adder is used as shown in Fig 2. Our proposed architecture aims to reduced overall power consumption and leads to increase speed. The design makes use of Energy Efficient HYBRID CMOS Full Adder in Place of conventional full adder. Let two numbers multiply using RCW Multiplier as shown below. The RCW Multiplier has three steps. Multiply (that is - AND) eachbit of one of the arguments, by each bit of the other, giving n2results. Depending on position of the multiplied bits, thewires carry different weights , for example wire of bit carrying result of a2 b3 is 32. Fig 3 shows the multiplication of two 4-bit numbers. The numbers are denoted by A and B where a0 , a1, a2, a3 represents the bits of multiplicand A with as its least significant bit and significant bit b0, b1, b2, b3 represents the bits of multiplier B with as its least significant bit and as its most significant bit. The Multiplication of two 4-bit numbers giving partial product, which arrange these partial product bit in tree format and reduced the group two bit using Half adder shown in first stage, and reduced the group of three bit using full adder shown in second stage of Fig 4. Then final adder add all the result of second stage give final product, which is of 8-bit .

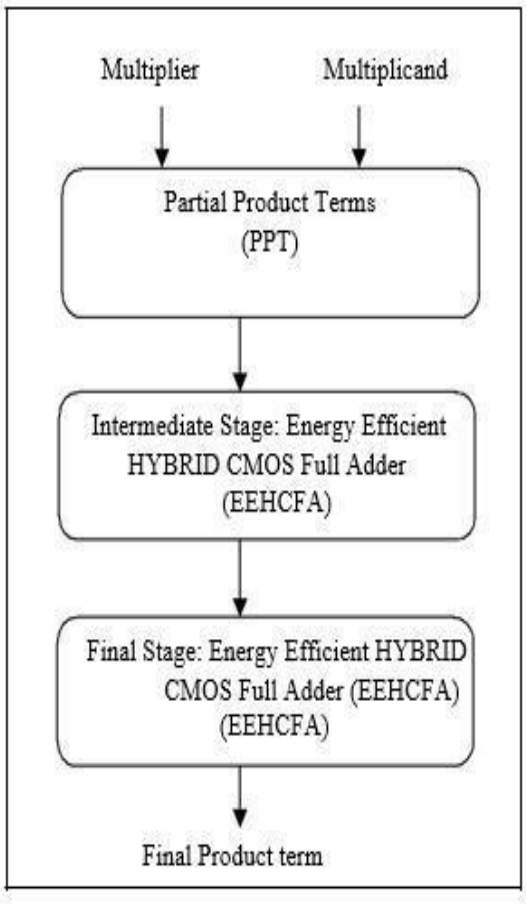

FIG: PROPOSED MODEL FOR WALLACE MULTIPLIER

V.AREA OPTIMISATION

Table I shows the complexity reduction. As seen from the table the total gate count for proposed multiplier is reduced as compare to other multiplier. Number of gate count for full adder is 8 and foe half adder is 6. Table II below shows the comparison between conventional full adders i.e. carry propagate adder and proposed full adder . From the below table it is seen that total fate count in carry propagating adder is 32 and in conventional full adder it reduced to 26 because of this total gate count for multiplier is reduced

COMPLEXITY OF REDUCTION

Proposed Wallace Tree Multiplier Using EECFA					
Number of bits	8	16	24	32	64
Number of stages	4	6	7	8	10
Full Adders	39	201	490	907	3853
Half Adders	3	9	16	23	53
Total Gates	324	1644	3984	7348	31036

TABLE 1:BITS OF WALLACE

parameter	existing	proposed
area	448	416
power	5.550e	5.2806 e
delay	1.55 e	1.0117 e

TABLE 2:COMPARISION

VI. SIMULATION RESULTS AND ANALYSIS

A. Schematic diagram of EEHCFA

Below shows a schematic for Energy Efficient HYBRID CMOS full adder using XOR/XNOR and two 2:1 MUX by using transmission gate

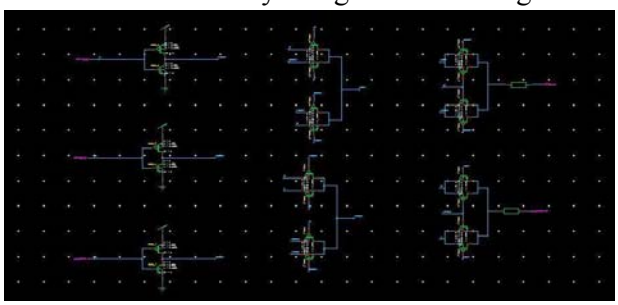

FIG:SCHEMATIC OF EEHCFA

B. Schematic Diagram For Result

This section analyzes the Result of energy efficient hybrid CMOS full adder

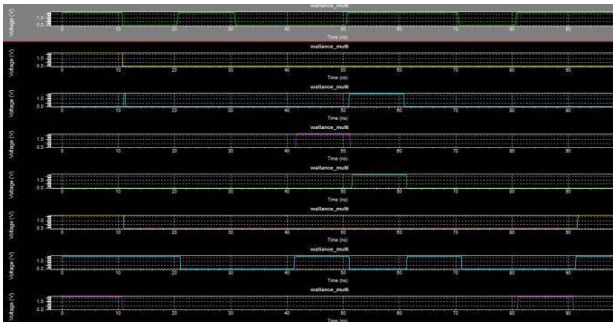

FIG:OUTPUT WAVE FORM

VII. CONCLUSION

The description of the multiplier circuits turned out well, all multipliers and helper circuits were easily made generic with respect to the number of bits in the inputs. This paper proposed modified reduced complexity Wallace Multiplier with reduced power consumption and area by using Energy Efficient HYBRIDCMOS Full Adder at the place of conventional Full adder. From the literature view it can be notify that proposed multiplier reduced power and total number of gate count i.e. reduced area.

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