ANALYSIS OF NEW TECHNIQUE FOR DIGITAL DIFFERENTIAL PROTECTION OF TRANSFORMER

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Abstract

The protection of power transformer is carried out by using unit Digital differential relaying scheme. This protective scheme should operate only for internal faults in the transformer but not for the external faults. Also this protective scheme should not operate for the inrush current in the transformer which occurs while energizing the transformer under no load condition. These currents are high in magnitude and remains for milliseconds. These current causes protective relay mal -operation and reduces power quality on the system. The protective scheme should differentiate between inrush current and fault current. For this purpose, Fast Fourier transform based logic technique is used for the analysis of type of incoming current in the transformer. Satisfactory operation of Digital differential relay is evaluated by simulation using Matlab software. Different cases of operating hazards have been analyzed by simulation and the stable operating status of the differential relay is observed. The outages of the power transmission line are reduced and the energy saving is achieved by introducing new technique of digital transformer protection.

Keywords: digital protection; differential protection; digital differential relay

I. INTRODUCTION

Transformer is the static device which is very important element in the power system. So, the protection of transformer is very important. Hence, it is carried out with the help of digital protection in which digital relay is used. This relay is fast and accurate as it is based on the software. Digital relay have many advantages over electromechanical relay and static relay. They require the hardware consisting of anti-aliasing filters, sample and hold circuits, multiplexer and analog to digital converters. These make the relay fast and accurate. Differential protection scheme is used for the protection of power transformer which is based on terminal quantities of transformer; the power input to the transformer under normal conditions is equal to the power output [1].Online condition monitoring of transformers can give early warning of electric failure and could prevent catastrophic failures and losses. Hence a powerful method based on signal analysis should be used in monitoring. The method should discriminate between normal and abnormal operating conditions that occur in power system related to transformers such as external faults, internal faults, magnetizing inrush, load changes, arcing, etc.

A new type of relays using the principle of harmonic restraint presented by Hayward's in his paper [3] ,which describe the difference between internal fault current and magnetizing-inrush current by their difference in the waveform shape. A new digital algorithm to detect winding faults in single-phase and three-phase transformers is presented by Sachdev, Sidhu and Wood [4]. Yabe [5] described a new method to discriminate internal fault current from inrush current by the sum of active power flowing into transformers from each terminal.

II. DIGITAL SOLUTIONS OF PERCENTAGE DIFFERENTIAL PROTECTION PROBLEMS

The proposed technique is tested on a 3Ø, 2-kVA, 230/100V,60Hz,Δ/Y, core-type power transformer. The simulated model is shown in Fig.1.Three identical current transformer (CTs) are connected in Y on the primary Δ connected side, and another three identical CTs are connected in Δ on the secondary Y connected side of the power transformer. The power transformer is connected to a small power system consisting of a three phase power generator feeds 0.5kW load through this transformer between two circuit breakers CB_1 and CB_2. These two CB_s are included in the system to examine the switching effect on the digital relay.

The proposed digital differential relay is designed using a simulation technique .The design is implemented to protect the power transformer against internal faults and prevent interruption due to inrush currents.

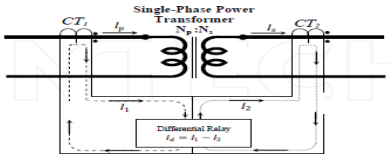

Fig. 1 Differential Protection of transformer

This algorithm is built on the principle of harmonic current restraint, where the magnetizing-inrush current is characterized by large harmonic components content that are not noticeably present in fault currents. Due to the saturated condition of the transformer iron, the waveforms of the inrush current are highly distorted. The amplitude of the harmonics, compared with the fundamental is somewhere between 30% to 60f % and the third harmonics are progressively less [3] [6].

Fig2 illustrates the flow chart of logic technique algorithm. In this algorithm the output currents of the CTs undergo over two analysis processes, amplitude comparison process and harmonic content calculation process. The amplitude comparison between the RMS values of the CTs output current ($|I_{d1} - I_{d2}|$) is in the left hand side of the flowchart, and the harmonic calculation is in the right hand side of the flowchart. The software is implemented according to the following steps:

1) Step one: Reading data from the CTs.

2) Step two: Data calculation, which is given as follows;

a) For the amplitude calculation, if the absolute difference ($|I_{d1} - I_{d2}|$) between the CTs output currents is greater than zero the logic (1) takes place, which indicates the case of an irush current or an internal fault. Otherwise the logic (0) takes place, which indicates detection of an external fault

3) Step three: Taking the final dicision:

a) If the logic cases received from both cases (a & b) in step two are both (1), that indicates a detection of an internal fault. Then a trip signal is released to stop the simulation.

b) For the other logic options of (0,1) means an external fault, (1,0) means an inrush current, or (0,0) indicate an occurrence of an inrush current or an external fault, and the simulation goes back to step two to start the calculation again for the next sample.

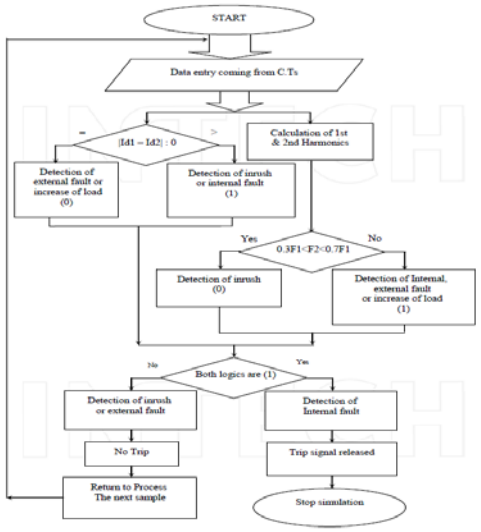

Fig.2. Flow chart of Digital Differential Relay Scheme

III. THE RESULTS AND DISCUSSIONS:

The results will be given for different cases:

Case 1: magnetizing inrush current,
Case 2: magnetizing inrush with adding load,
Case 3: Three phase to ground fault at loaded transformer,
Case4: Phase A to ground external fault at loaded transformer

Other cases of different types of faults and inrush currents such as single line to ground fault, line to line to ground fault and

three phase fault in both cases loaded and unloaded transformer are illustrated.

Case 1: Magnetizing inrush current:

In this section of simulation, when the primary side CB_1 is closed at 0.1 sec, only the inrush current flows in the primary circuit of the power transformer and no current passes through the power transformer to the secondary side as shown in fig. 3. The harmonic comparator shows in fig.4 that the value of the 2nd harmonic is higher than 0.3 of the fundamental component.

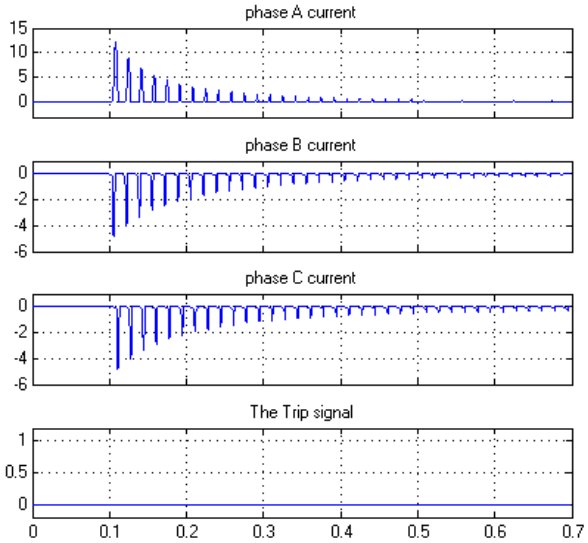

Fig. 3.Inrush currents waveforms of the three phases at the primary side of the power transformer

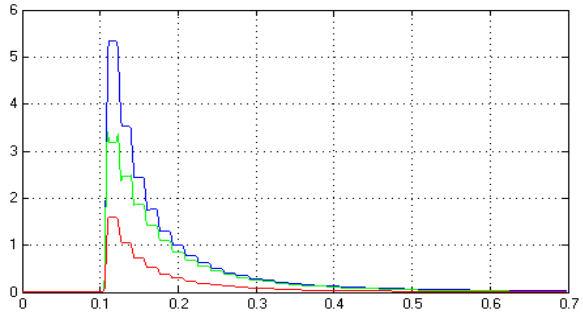

Fig. 4 Harmonic comparator result: the 2nd harmonic and the fundamental component for the 1st case

In this case the harmonic calculation part released logic (0) but the amplitude comparator shows in fig. 5 that the differential current is equal to the inrush current, where both curves are drown over each other, then the amplitude comparator release logic (1). For this logic coordination (0,1) no trip signal is released.

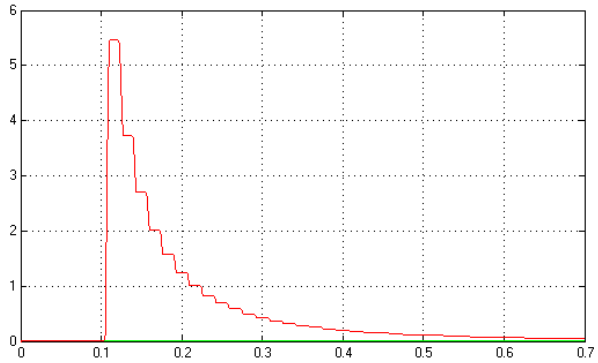

Fig. 5
Amplitude comparator results for the 1st case

Case 2: Magnetizing inrush with adding load:

This test is carried out after the energization of the power transformer by switching ON the CB_1 at 0.1sec and CB_2 at 0.3sec from the beginning of the simulation to see the effect of load excursion on the accuracy of the designed approach. Therefore, a 500W resistive load is added to the system at 0.3 sec. Consequently, the inrush current disappeared and load current started to flow in the primary and secondary circuits of the transformer according to the transformation ratio of the power transformer as shown in fig. 6. However, the output currents of the primary and secondary CTs are equal due to the proper selection of the transformation ratio of the primary and secondary CTs, which can obviously noticed in fig. 8. Where, before the time 0.3 sec the differential current was equal to the inrush current, but after the swathing ON of the load the differential current went to zero and the primary and secondary currents become equal.

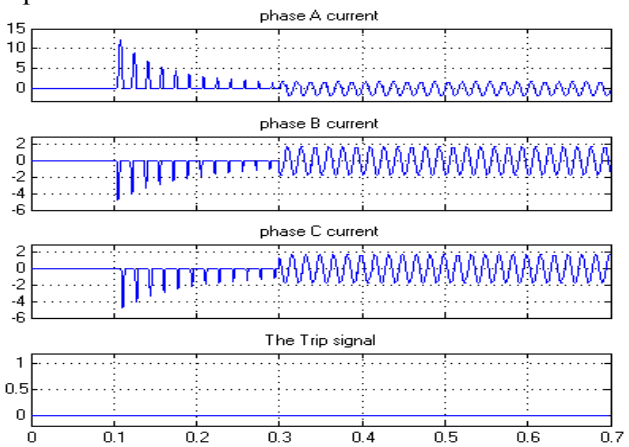

Fig.6 Normal load current starts flowing at 0.3sec

As shown in Fig.7, after the switching of CB_2, the value of the 2nd harmonic become lower than 0.3 of the fundamental component. Accordingly, the harmonic calculation part released logic (1) but the amplitude comparator released logic (0). Consequently, for this logic coordination (1,0) no trip signal is released.

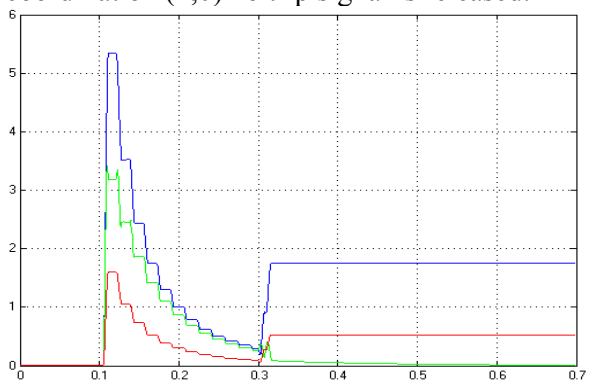

Fig.7 2nd harmonic and the fundamental component for the 2nd case

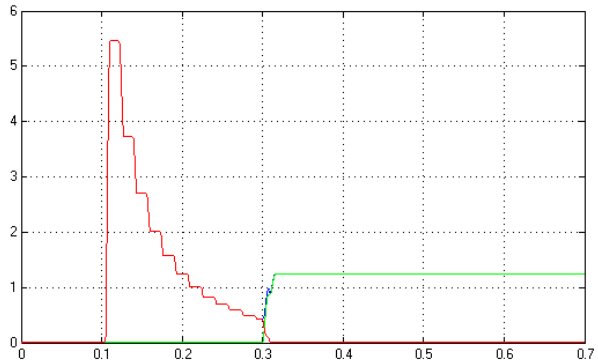

Fig. 8 Amplitude comparator results for the 2nd case

Case 3: Three phase to ground fault at loaded transformer:

In this section, a three phase to ground fault is created to test the security of the algorithm. After the switching of CB_1 at 0.1 sec, an internal fault is created at 0.5 sec at the secondary side of the power transformer by connecting the three phases A, B and C of the secondary side of the power transformer to the ground. In this case, a significant increase of the primary current takes place due to the fault occurrence inside the protected zone at 0.5 sec as shown in fig. 9. The relay detected this increase using the harmonic and amplitude comparators and realized it as an internal fault. Consequently the transformer is isolated from the grid. Also it is obvious from fig. 10 that the relay has released a trip signal after 0.57 m. sec. after the occurrence of the fault, which can be considered as a very good speed to isolate the transformer.

As shown in fig. 11, after the occurrence of the fault at time 0.5 sec, the value of the 2nd harmonic increased during the transient time and the decreased rapidly to a value lower than 0.3 of the fundamental component once the steady state is achieved. Accordingly, the harmonic calculation part released logic (1). Also from fig.12 which shows the result of the amplitude comparator the value of the differential current is no longer equal to zero. Accordingly the amplitude comparator released logic (1). Therefore, for this logic coordination (1, 1) a trip signal is released in order to isolate the power transformer from the grid.

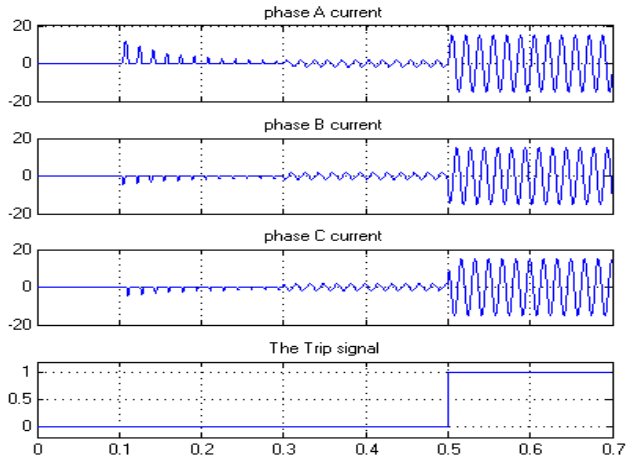

Fig. 9 Increase of phase A, B, & C currents due to the occurrence of the fault at 0.5 sec for loaded transformer

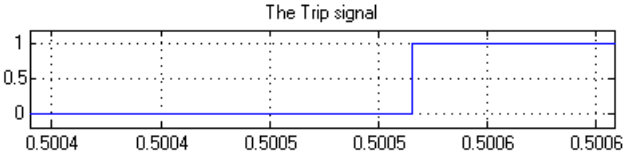

Fig. 10 Zoomed trip signal, trip time is around 0.57m.sec

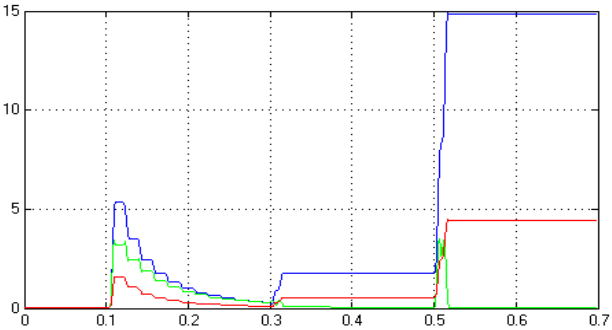

Fig. 11
2nd harmonic and the fundamental component for the case of three phases to ground fault at loaded transformer

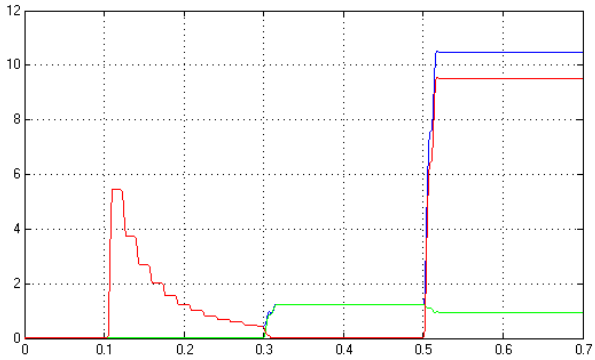

Fig. 12 Amplitude comparator result for the 3rd case

Case 4: Phase A to ground external fault at loaded transformer

This case is similar to case 2, where the occurrence of the fault current outside the protected zone leaded to the increase of fault currents in both sides of the power transformer. Therefore the relay considered this case as a sever increase in load currents. Figure 13 shows the increase in load currents. Figure 13 shows the increase in phase A current and no trip signal is released

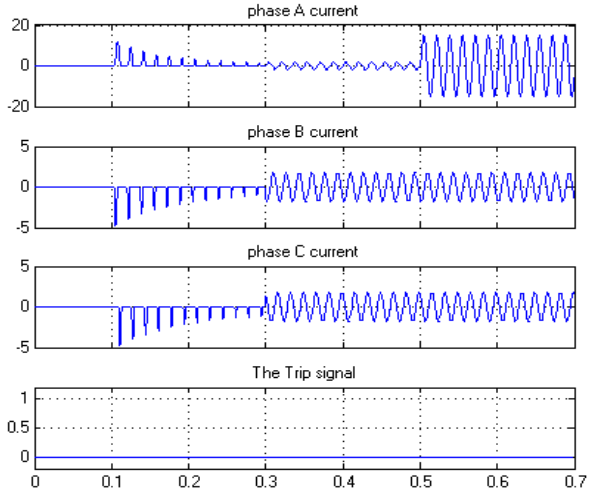

Fig. 13 Increase of phase A current due to the occurrence of the fault at 0.5 sec for loaded transformer

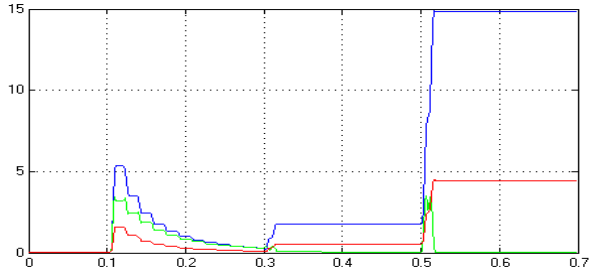

Fig. 14
2nd harmonic and the fundamental component for the case for the 4th case

As illustrated in fig.14, after the occurrence of the external fault at 0.5 sec, the value of the 2nd harmonic decreased to a value less than 0.3 of the fundamental component. Accordingly, the harmonic calculation part released logic (1) but the amplitude comparator released logic (0) because the differential current is almost zero as it can be seen from figure 15. Consequently, for this logic coordination (1, 0) no trip signal is released.

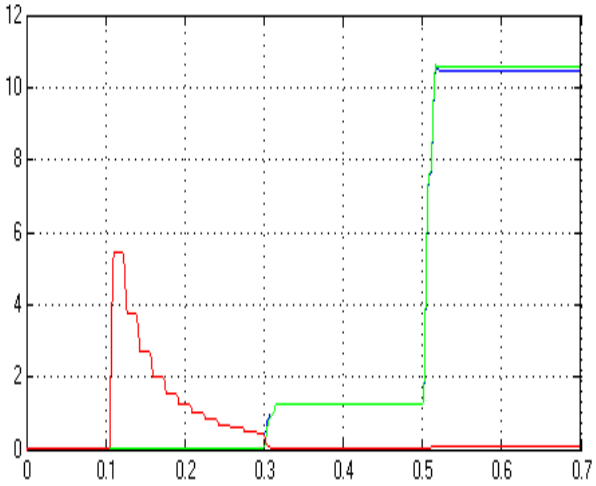

Fig. 15 Amplitude comparator result for the 4th case

Similarly, the relay is tested for all other cases of different types of fault such as single line to ground, line to line, line to line to ground and three phase faults in both cases loaded and unloaded transformer. In all cases the relay has successfully released a trip signal in each case. The results of some of these different types of faults are shown in figures (16 – 20).

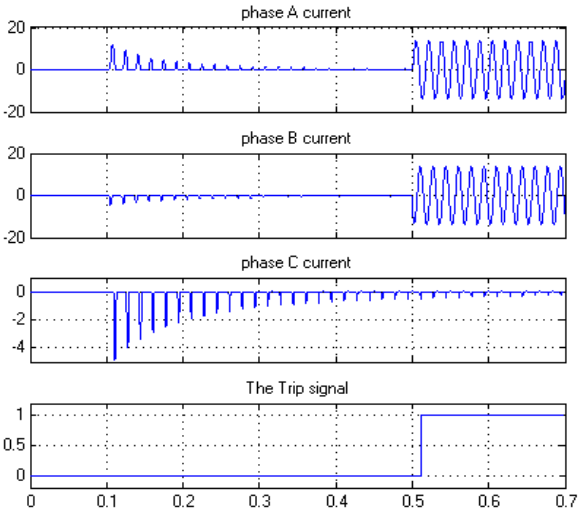

Fig. 16 Increase of phase A & B currents due to the occurrence of the fault at 0.5 sec, for unloaded transformer

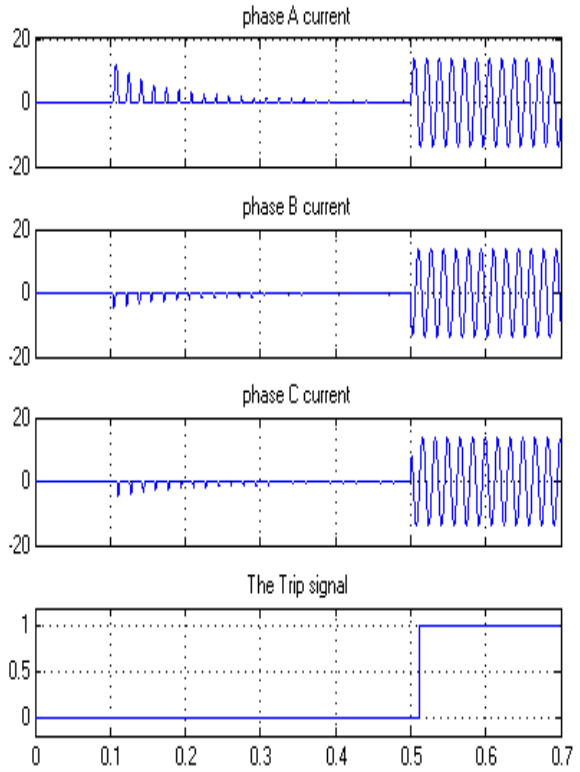

Fig. 17 Increase of phase A, B & C currents due to the occurrence of the fault at 0.5 sec, for unloaded transformer

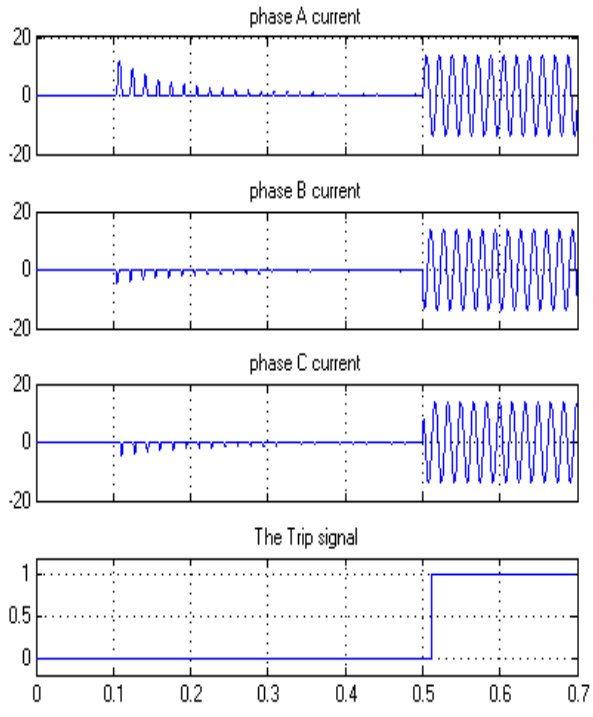

Fig. 18 Increase of phase A current due to the occurrence of the fault at 0.5 sec for loaded transformer

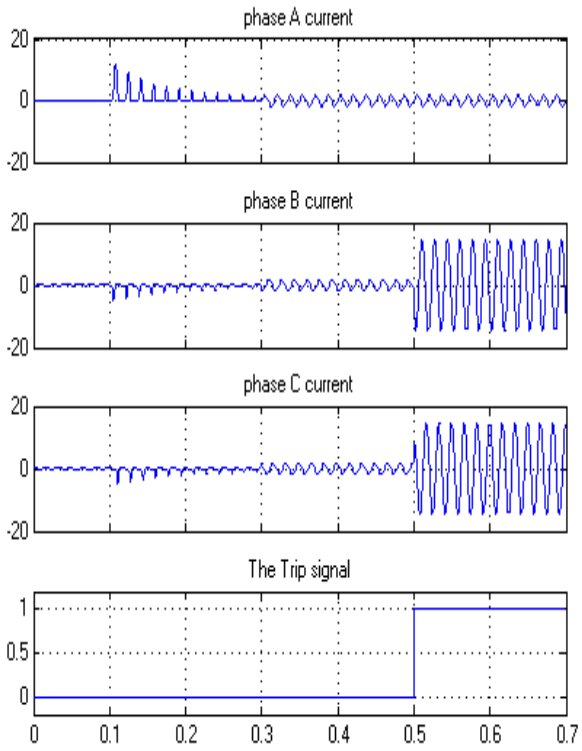

Fig. 19 Increase of phase B & C currents due to the occurrence of the fault at 0.5 sec for loaded transformer

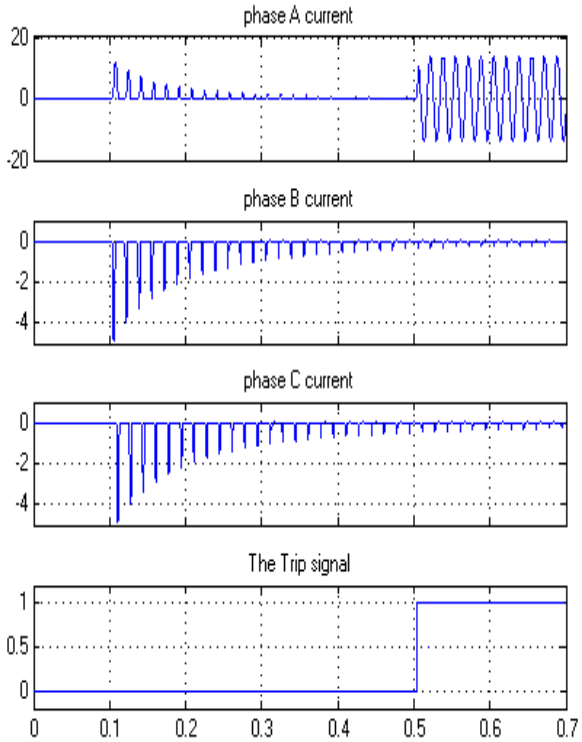

Fig. 20 Increase of phase A current due to the occurrence of the fault at 0.5 sec, for unloaded transformer

IV SIMULATION OUTCOME

Table No. 1 Performance of relay under various cases

Sr. No.	Type of Cases	Unloaded Time Trip Status (m Sec)	Loaded Time Trip Status (m Sec)	Functioning of Relay
1	Phase A to Ground Fault	4.7	1.7	Trip
2	Phase B to Ground Fault	12	0.6	Trip
3	Phase C to Ground Fault	15	0.6	Trip
4	Phase A to Phase B Fault	1 2.2	0.8	Trip
5	Phase B to Phase C Fault	14.6	0.6	Trip
6	Phase A to Phase C Fault	12	1.3	Trip
7	Phase A to Phase B to Ground Fault	12	0.6	Trip
8	Phase B to Phase C to Ground Fault	13.2	0.6	Trip
9	Phase A to Phase C to Ground Fault	0.57	0.6	Trip
10	Three phase Fault	12	0.6	Trip
11	Load Current	No Trip		Restrain
12	Inrush Current	No Trip		Restrain
13	Earth Fault	No Trip		Restrain

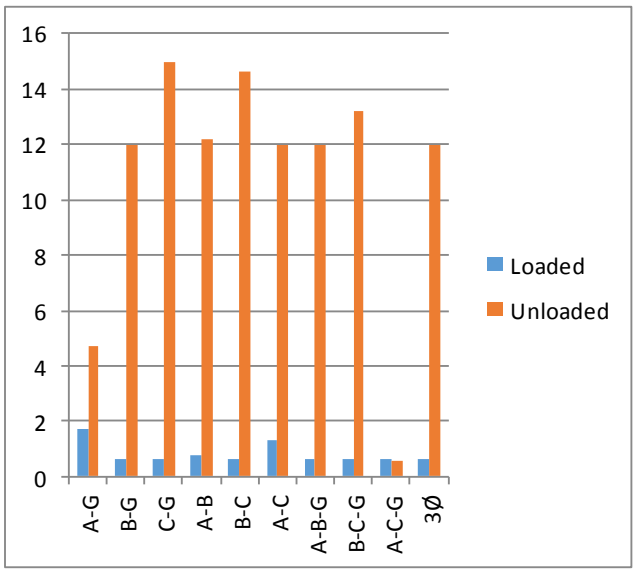

Fig. 21

Simulation Outcomes

CONCLUSIONS

A Matlab simulation of a power transformer under various cases is presented in this paper. The results in this simulation are tested for many cases and for all cases it gave satisfactory results. It is found that the fastest trip time was around 0.57 m.sec in the case of phase A – phase C - ground fault and the slowest trip time was 15 m.sec for phase C to ground fault when the transformer is unloaded. Further after loading the transformer the fasted time 0.6 m sec is observed. This trip time is satisfactory in order to to ensure that the algorithm will give a proper decision to discriminate between a fault current and an inrush current. On the other hand the relay is restrained in the cases of inrush current, normal load current or the external fault current and the performance indicated that energy saving is achieved due to restraining the unwanted outages on the power transmission lines due to this new method.

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