DESIGNS, IMPLEMENTATION METHODS AND ANALYSIS FOR SRAM

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Abstract

Power consumption, delay, and leakage current are the major design concern of CMOS Technology. Especially for short channel devices, the problem of leakage power is more pronounced. In addition to that, as the technology compresses, the leakage current also increases very fast. Therefore, numerous low power techniques have been evolving to reduce the leakage current in CMOS technology. Due to technology advancements, SRAM cell size is decreasing, the leakage current and power become the significant components to deal with. In this paper, we are proposing various SRAM design techniques for 6T, 8T and 10T models; one is by considering technology variations. For that, conventional SRAM cell is designed using 120 and 90nm technologies and compared their parametric variations. The other design aspect of SRAM is, using logic design techniques such as Pass Transistors logic, Transmission gate logic and adiabatic logic. The performance of each SRAM design is compared with conventional SRAM in terms of delay, power and area. We observed that for low power applications one could prefer adiabatic logic to CMOS logic. The Transmission gate SRAM suitable for low leakage current applications, Pass Transistor Logic is suitable for the designs where critical path and area are to be low.

Index Terms: 6T, 8T and 10T SRAM configurations, parametric variations, logic design techniques, delay, power, leakage current, Pass Transistors logic, Transmission gate logic and adiabatic logic.

I. INTRODUCTION

According to International Technology Roadmap for Semiconductor (ITRS) reports the present size of 6T SRAM cell 0.096 μm^2 may become 0.003 μm^2 by the end of 2028 on the silicon area with an average size reduction of 38.8% for every two years [1]. This shows a rising demand for more chips area for embedded memory with a commitment for low power, standby data retention, stability, and less cell area. SRAM plays a critical role in modern microprocessor system, portable devices like PDA, cellular phones, portable multimedia devices and in SoC's. SRAM based cache memories are commonly used to achieve higher speed processor. The trend of scaling of device brings several challenges like power dissipation, sub threshold leakage, reverse diode leakage, and stability. From few years, CMOS devices are scaled down to reach the better performance in terms of speed, size and reliability, power dissipation.

Reduction in the threshold voltage and the gate oxide thickness are the root cause for the evolution of many advanced research developments of SRAM designs. The likely parameters that show impact on performance of SRAM memory considered are intrinsic parameter fluctuation, random dopants fluctuation, oxides thickness fluctuation, and line edge roughness degrade the stability of SRAM cells. Since the conventional 6T SRAM suffers from stability problems, an effort is being made to solve using Schmitt trigger based SRAM design in [2] shows that much less power than the existing, but at the cost of increased

number of transistors. However, this method reduces power dissipation along with stability improvements. There are other methods [3] such as modified design for charge sharing in which read discharge power is reused in order to reduce low swing on read and write lines to target reduction in power dissipation. Using less number of transistors at the same time good read stability is achieved by implementing the 7T SRAM design [4], which reduces area and power. Charge sharing technique is introduced in implementing 8T [5, 6], 10T SRAM to reduce power consumption, with less number of transistors [7, 8], which results in reduction of power. In [9], different SRAM designs such as 6T, 8T, and 10T were addressed based on different logics to improve stability with low power and area as major concerns. power and area. It is observed that for low power applications one can prefer adiabatic logic to CMOS logic. The Transmission gate SRAM suitable for low leakage current applications, Pass Transistor Logic is suitable for the designs where critical path and area are to be low. The proposed designs were implemented in Microwind 3.1. The rest of the paper is organized as follows: Different SRAM cell configurations i.e. 6T, 8T, and 10T are discussed in section II. Section III gives the details of proposed work. Section IV provides performance comparison in terms of power dissipation and maximum current area and delay for various types of SRAM configurations against the technology variations and based on logic design. Conclusions and future work are provided in section V.

II. REVIEW ON RELATED WORK

A. Review Stage

The most usually used configurations in SRAM design are 6T[1], 8T[5] and 10T[7]. Poor stability, small hold, and read static noise margins are the commonly seen problems in 6T. Especially in read operation, the vulnerability in stability will occur and is mainly due to the voltage division between access and driver transistor. This problem was addressed by using 8T structure in which the data holding element and data output element were separately taken. As a result read '1' value due to not having any discharge path. However, the problem is with read current flow to ground. Invention of 10T eliminates this problem by using two more transistors in the decoupled read path. Instead of draining the read current to ground, the read path is connected to BL & BLB through these 2 transistors.

III. PROPOSED WORK

The proposed work is intended to reach design of low power SRAM. Dynamic power varies as VDD2. So reducing the supply voltage reduces power dissipation [10]. Selective frequency reduction technique and multi- threshold voltage techniques are few, which reduces dynamic power as well as leakage power at system level. Transistor resizing can be used to speed-up circuit and decreases power. Using this technique, SRAM is designed in 120nm and 90nm with reduction of voltage. However, observed that resizing of transistor with reduced supply voltage affects circuit speed and is the major deficiency of this approach. Hence, instead of technological solutions, logic design as a solution is implemented that encountered the problem of circuit performance degradation introduced by reduction of voltage. Some of the logic techniques used as low power designs are sleep transistors to reduce standby power, parallelism and pipelining in system architecture, clock disabling, power-down of selected logic blocks, adiabatic computing. In the proposed work, SRAM is designed using Transmission gate, pass transistor and adiabatic logic. Results are captured for each design and the performance of SRAM is compared in terms of critical path delay, power dissipation, maximum current and area.

A. Transmission gate logic (TG)

A transmission gate is a switch comprised of a pMOS transistor and nMOS transistor, which will selectively obstruct or surpass a signal level from the input to the output. The biased control gates are used to maintain both the transistors are in either on or off.

i. SRAM 6T cell design using TG logic

The conventional SRAM is implemented using TG logic and the resulting 6TG SRAM cell is shown in Fig. 1. Transmission gates are used

in the place of two cross-coupled inverters. Two more TG cells are used in the place of access transistors. The control signal, denoted by WL, is connected to the Access TG cells, so that, the data can be written or read from bit lines similar to conventional SRAM cell.

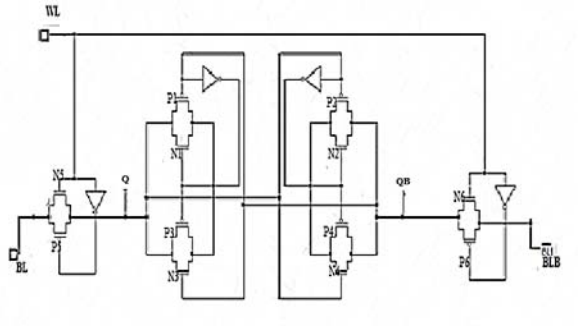

Fig 1. TG based 6TSRAM cell design

ii. SRAM 8T cell design using Transmission gate logic

The circuit design for 8T SRAM using TG logic is shown in Fig.2. It follows 6TG SRAM structure, in addition read decoupled path consisting of two transmission gates. The write and read operations are same as discussed in conventional 8T SRAM design.

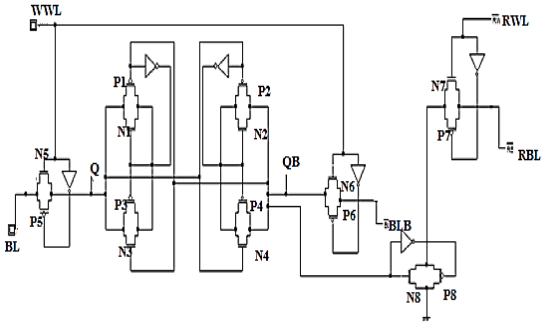

Fig.2 TG based 8T SRAM cell design

iii. SRAM 10T cell design using Transmission gate logic

The architecture of the 10TG SRAM cell is shown in Fig. 3 is similar to the single ended 8TG SRAM cell. In addition to the 8 transmission gates, 2 transmission gates are added in the decoupled read path and instead of draining the read current to ground, the read path is connected to BL & BLB through these 2 transmission gates. The write and read operations are same as discussed in conventional 10T SRAM design. Corresponding simulation results are shown in Fig.4 & 5.

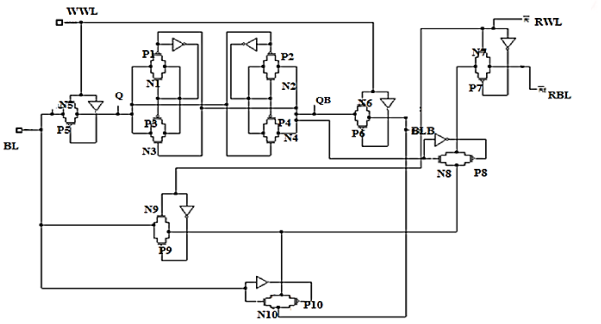

Fig.3 TG based 10T SRAM cell design

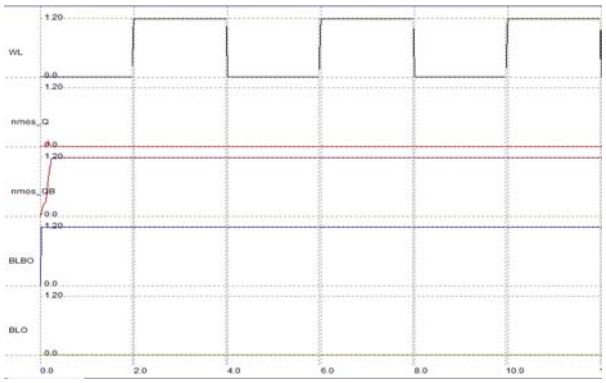

Fig.4 Simulation results for TG based 6T SRAM cell design for Write '0' operation

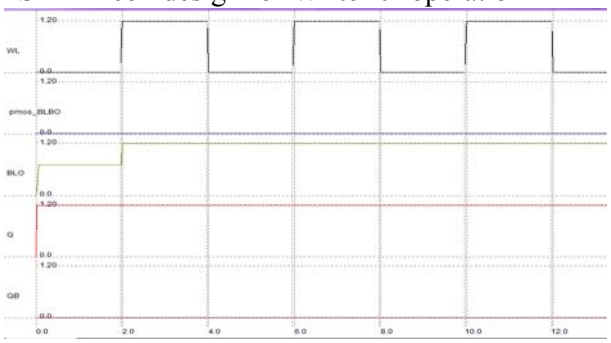

Fig.5 Simulation results for TG based 6T SRAM cell design for Read '1' operation

B. Pass Transistor Logic (PTL)

Pass transistor network realizations of logic functions in general result in area savings and higher operating speed when compared with the corresponding gate logic realizations. It acts like a switch. NMOS pass transistor logic using the NMOS transistor as a pass element has a substantial area savings, speed improvements and less power dissipation compared to gate logic implementations.

i. SRAM 6T cell design using PTL logic

The circuit shown in Fig.6 consists of two

cross-coupled inverters connected back to back were made up of 2 NMOS transistors and as usual two more NMOS transistors are used as access transistors. Structural design is same as conventional design except the pull-up PMOS transistors. Write and read operations are same as conventional 6T SRAM design.

ii. SRAM 8T cell design using PTL logic

The circuit design shown in Fig.7 is same as 8T SRAM cell but is designed only by NMOS pass transistors. The operation of the circuit is same as conventional 8T SRAM cell. The additional NMOS pass transistors are needed to separate the data-holding element and the data output element. This will lead to a read disturb free operation. Read and write operations are same as we discussed in conventional 8T SRAM cell design.

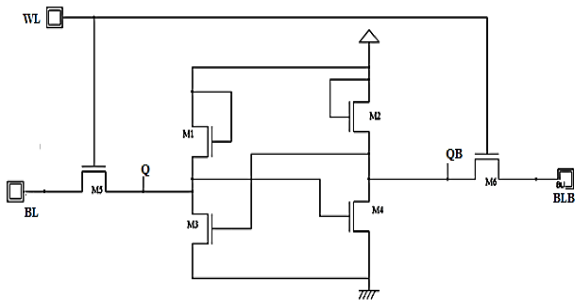

Fig.6 PTL based 6T SRAM design

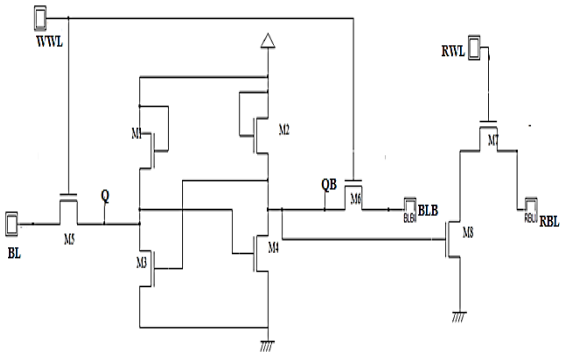

Fig.7 PTL based 8T SRAM cell design

iii. SRAM 10T cell design using PTL logic

The circuit design shown in Fig.8 is same as 10T SRAM cell but the cell is designed only by NMOS pass transistors. It is similar to the conventional 10T SRAM cell. Two more transistors are used in the decoupled read path, which is connected to BL and BLB, will avoid draining of read current to ground. Read and write operations are same as we discussed in conventional 10T SRAM cell design. Corresponding simulation results are shown in Fig. 9&10.

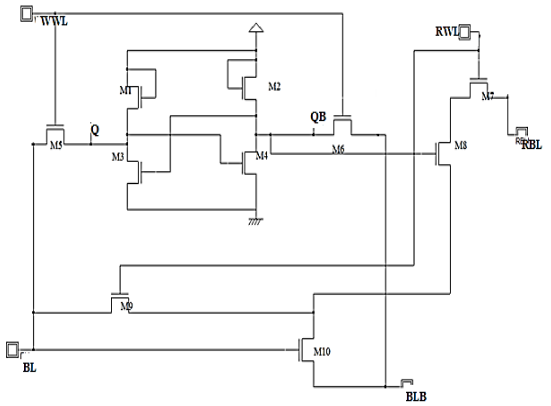

Fig.8 PTL based 10T SRAM cell design

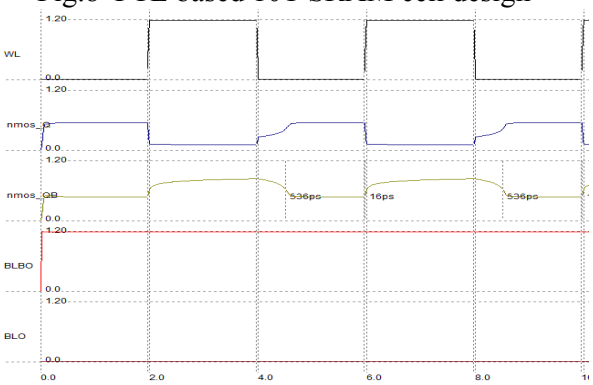

Fig.9 Simulation results for PTL based 6T SRAM cell design for Write '0' operation

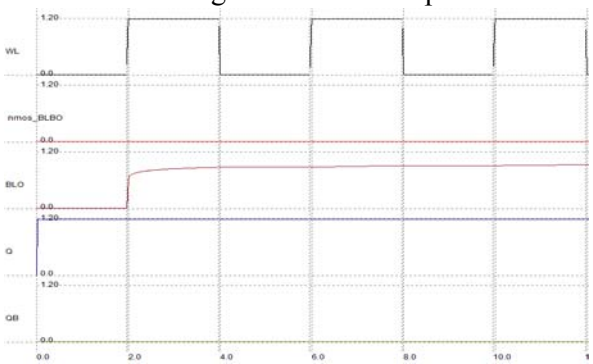

Fig.10 Simulation results for PTL based 6T SRAM cell design for Read '1' operation

C. Adiabatic Logic

Adiabatic logic is one of the design methods for reversible logic in CMOS, in which the energy dissipation due to switching of capacitor is minimized. Basics of Adiabatic Design Two rules must be followed in order to implement adiabatic logic in CMOS. Initially the transistor

must be in turned off as long as the voltage across drain and source are different. Otherwise, energy gets dissipated and loss of information will take place. The second rule is that a nonzero voltage must never be applied across a transistor during any transition. If this occurs, then the internal resistance of the transistor is relatively small, resulting in a very high power spike and consequential energy dissipation. Transistors are used in adiabatic operation, achieved through the application of two rules.

i. Conventional SRAM 6T cell design using adiabatic logic

The circuit shown in Fig.11 consists of two cross-coupled inverters connected back to back were made up of CMOS transistors and Transmission gates were used as access transistors. Structural design is same as conventional design except the access transistors. Write and read operations are same as conventional 6T SRAM design.

ii. SRAM 8T cell design using adiabatic logic

The circuit design shown in Fig.12 is same as 8T conventional SRAM cell but is different in access transistors section as well as coupling section, which are designed with transmission gates. The additional coupling TG transistors are needed to separate the data-holding element and the data output element. In turn, the cell implementation provides a read-disturb-free operation. Read and write operations are same as we discussed in conventional 8T SRAM cell design.

iii. SRAM 10T cell design using adiabatic logic

The circuit design shown in Fig.13 is same as conventional 10T SRAM cell but the cell is designed with TG transistors in access transistor as well coupling sections. Two more TG transistors are used in the decoupled read path, which is connected to BL and BLB, will avoid draining of read current to ground. Read and write operations are same as we discussed in conventional 10T SRAM cell design. Corresponding simulation results are shown in Fig. 14&15.

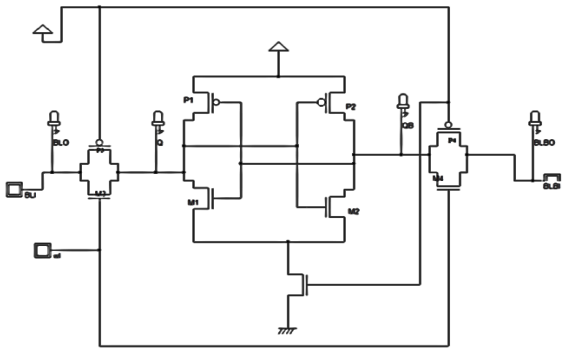

Fig.11 Adiabatic 6T SRAM design

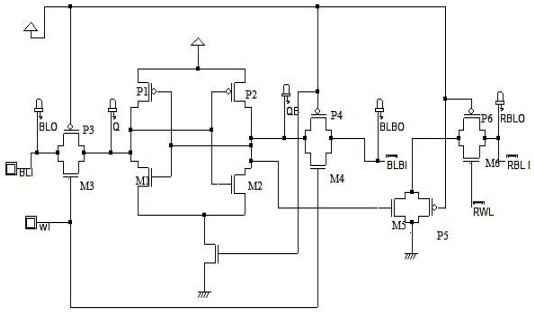

Fig.12 Adiabatic 8T SRAM design

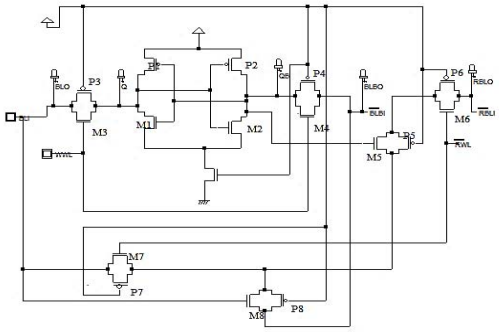

Fig.13 Adiabatic 10T SRAM design

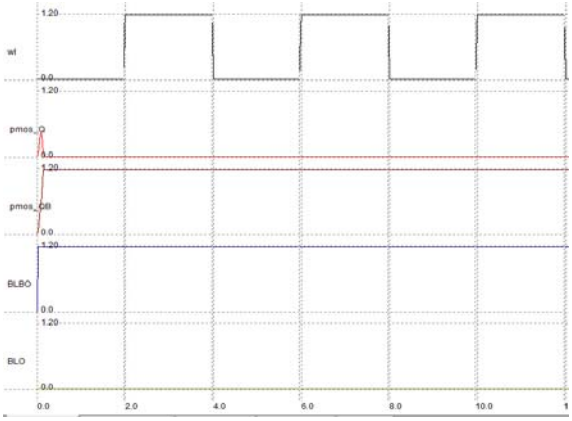

Fig.14 Simulation results for Adiabatic based 6T SRAM cell design for Write '0' operation

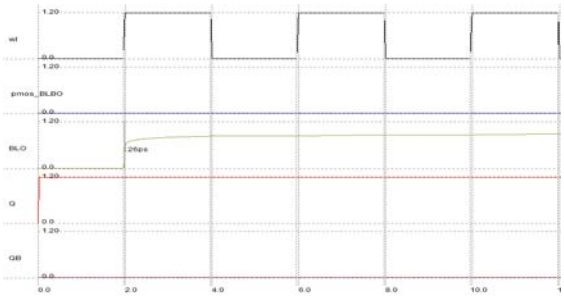

Fig.15 Simulation results for Adiabatic based 6T SRAM cell design for Read '1' operation

IV. PERFORMANCE COMPARISON OF SRAM

A. Outcome of Transistor resizing technique

As discussed in section III, SRAM with 6T, 8T, and 10T are simulated for technologies 120 and 90nm. The simulation parameter chosen in Microwind such that the operating voltages used are 1.5, 1.2, 1 and 0.9 volts. Table 1 & 2 shows the parametric variation observed at typical 1 volt. It is observed that the rise in delay (CPD) compensated the low power dissipation. The sizing of transistors p:n follows 2:1 ratio for both 120 and 90nm technologies.

B. Outcome of logic design techniques

As discussed in section III, SRAM with 6T, 8T, and 10T models were designed using TG, PTL and adiabatic logic styles. Observed their corresponding results and compared in Table 3, 4, & 5.

From Figs. 16,17, & 18, we observed that power dissipation is low in TG and Adiabatic logic SRAM designs compared to PTL and. Regarding $I_{DD\ max}$, is low in Adiabatic logic compared to other two logic designs and is shown in Fig. 19, 20, &21.

Table.1 Results using 120nm for CMOS based 6T, 8T, & 10T

SRAM type	CPD (ns)	P_d(µw)				$I_{dd\ max}$ (mA)				Area (um^2)
		W0	W1	R0	R1	W0	W1	R0	R1	
6T	1.9	0.39	1.45	0.055	0.045	0	0.941	0.033	0.026	81.6
8T	2.04	1.48	0.36	0.008	0.060	0.952	0	0	0.033	115.2
10T	2.04	1.49	0.37	0.008	0.056	0.932	0	0	0.033	145.2

Table.2. Results using 90nm for CMOS based 6T, 8T,& 10T

SRAM type	CPD (ns)	P_d(µw)				I_{dd_max}(mA)				Area (um^2)
		W0	W1	R0	R1	W0	W1	R0	R1	
6T	1.9	0.303	1.417	0.039	0.031	0	0.928	0.034	0.026	56.7
8T	2.8	1.504	0.281	0.001	0.039	0.932	0	0	0.034	80
10T	2.85	1.522	0.285	0.001	0.039	0.932	0	0	0.034	101

Table.3. Results using 120nm for TG based 6T, 8T, & 10T

TG based SRAM	CPD(ns)	P_d(µw)				I_{ddmax}(mA)				Area(um^2)
		W0	W1	R0	R1	W0	W1	R0	R1	
6T	5.5	3.579	3.652	2.890	2.917	0.521	0.521	0.521	0.521	244.3
8T	5.9	3.999	3.847	1.948	2.424	0.520	0.520	0.260	0.453	367.6
10T	6.8	4.506	3.941	3.102	3.564	0.519	0.519	0.518	0.518	563.2

Table.4. Results using 120nm for PTL based 6T, 8T, & 10T

PTL based SRAM	CPD(ns)	P_d(µw)				I_{dd} max(mA)				Area(um^2)
		W0	W1	R0	R1	W0	W1	R0	R1	
6T	0.9	545	545	1470	1470	0.859	0.861	1.273	1.269	63
8T	1	548	520	1470	1297	0.871	0.774	1.234	1.135	99.8
10T	1.3	548	520	1470	1297	0.871	0.774	1.234	1.135	130

Table.5. Results using 120nm for ADB based 6T, 8T, & 10T

Adiabatic SRAM	CPD(ns)	P_d(µw)				I_{dd} max(mA)				Area(um^2)
		W0	W1	R0	R1	W0	W1	R0	R1	
6T	2.25	0.585	2.378	0.128	0.129	0	1.323	0.085	0.086	137.8
8T	2.42	2.644	0.665	0.005	0.211	1.352	0	0	0.140	238.9
10T	3.18	2.658	0.661	0.005	0.216	1.355	0	0	0.146	329.3

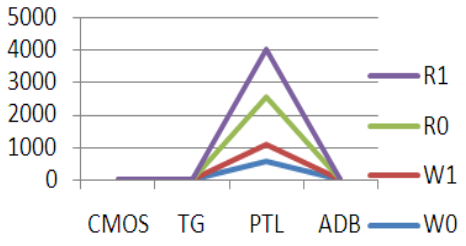

Fig. 16. Comparison of P_d for 6T SRAM using logic design techniques chosen.

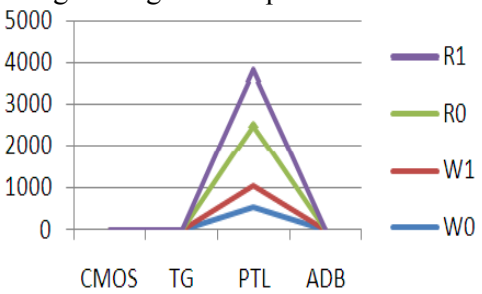

Fig. 17. Comparison of P_d 8T SRAM using logic design techniques chosen

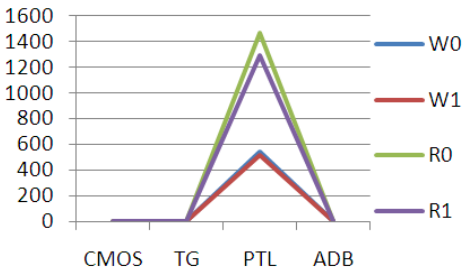

Fig. 18. Comparison of P_d for 10T SRAM using logic design techniques chosen

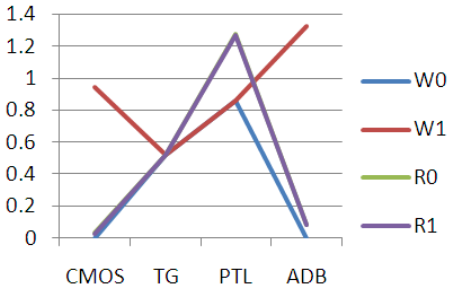

Fig. 19. Comparison of I_{DDmax} for 6T SRAM using logic design techniques chosen

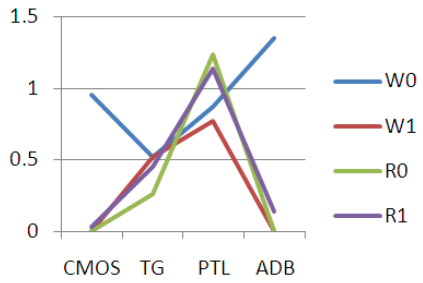

Fig. 20. Comparison of I_{DDmax} for 8T SRAM using logic design techniques chosen.

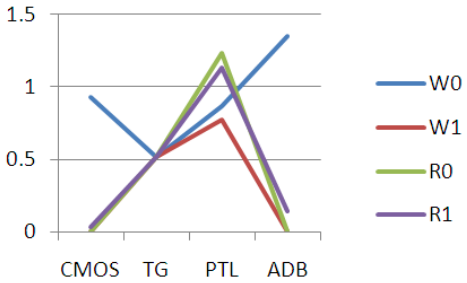

Fig. 21. Comparison of I_{DDmax} for 10T SRAM using logic design techniques chosen.

V. CONCLUSION

We focused on the design of SRAM cell against the variations of technology parameters such as power dissipation, delay, maximum current and area. We have designed the 6T; 8T & 10T SRAM cells using transistor resizing technique with technologies 120nm and 90nm and observed that as technology shrinks area, power dissipation and maximum current required also shrinks but at the penalty of increased delay.

Using transmission gate, pass transistor logic and adiabatic logic, we have designed structural models of 6T, 8T and 10T SRAM cells in 120nm technology and observed the performance of each design in terms of power dissipation, maximum current, critical path delay and area. From the observations it is noted that area and critical path delay are reduced when pass transistor logic is used compared to that of both traditional CMOS logic and transmission gate logic. Power dissipation and area are reduced when traditional CMOS logic used compared to that of transmission gate logic. Comparing to all logics, adiabatic logic results in low power.

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