DESIGN OF AREA EFFICIENT MULTI-BIT FLIP-FLOP USING CLOCK GATING WITH HIGH SPEED

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***Abstract*— For the first time, this Report introduces RF compatibility studies for the next-generation wireless communication processes requiring compatible body systems, in the form of fully integrated CMOS RF integrated circuits, where wireless Communication RFICs are integrated in ultra-thin compact packets. As the test case, the RF properties of a various die substrate thickness CMOS (VCO) chip were determined and the results were analysed. The studied CMOS VCO chip has been developed and manufactured using the RF-CMOS 180 nm method. The reliability of VCO chips efficiency is characterised and the results comparable between 250 and 50, 35 and 25 µm are correlated before and after diet. The study shall take account of critical RF efficiency parameters, such as oscillation frequency, output power and phase ring. All die-cells are positioned face-up in the micro chamber of the probe station to be sampled on a metal chuck with connector. Due to the effects on the diminishing diet, the phase noise degradation is seen significantly when the variations in frequency and output power are ±1% and ±1 dB respectively. The very well fact of phase noise sensitivity to the thickness of the substrate due to leakage supports this and SOI CMOS is commonly debated in order to mitigate this parasite.**

Keywords—radio frequency (RF), complementary metal oxide semiconductor (CMOS), voltage controlled oscillator (VCO), ultra thin flexible packages, frequency of oscillation, output power, phase noise

I. INTRODUCTION

The electronic devices of next century drive the technology sector to include ultra-thin and modular integrated circuits (ICs). Using ultra-thin and compact ICs, efficient and cost-effective technologies have an influence on many applications such as cellular, portable electronics, the Internet of Things and health care surveillance. The impact of die-substrate thinners on the RF efficiency of an IC is one of the key challenges to achieve versatile and ultrathin ICs. There are also problems associated with the implementation of incredibly slim ICs because the ultra-thin ICs need to be handled with great accuracy and because the die-substrata thinning would likely cause electrical efficiency deterioration. Due to ultra-thinning the functional areas of an incredibly thin IC can be weakened and thus the general performance of the ICs can be affected. The various facets of IC substrata are seen to dilute much of the previous work, but only to 40 µm. Much is based on efficiency of electrostatic discharge, thermal characterisation and ultra-thin chip modeling. Although the effects of reduction of the plate thickness on an RF transformer are examined, the total RF output effects of a fully integrated RFIC were not previously studied by the substrate dilution.

This Letter introduces for the very first time in its best understanding RF statistical analyses of integrated RFIC CMOS chips with different die

thicknesses up to 25 μm for ultra thin flexible semiconductor materials. As a test case, the research and review were done with fully integrated VCO chips which were developed and manufactured using the 180-nm CMOS process. Measuring in this work has been carried out to assess the effect of significant VCO parameters including operating frequency, RF output, phase noise and DC efficiency due to dilution in the substratum.

II. VCO CHIPS THINNING AND CHARACTERISE.

On the regular die the die, the phase of CMOS is approximately 250- to 300 μm micrometers. Figure 1 shows a substrate layer thickness of one micrometer in 1-micron CMOS-6-180nm CMOS 180nm technology, which is 1 μm thick. For ultra-thin flexible, ultra-thin electronics, LC-output VCOs were considered stronger. Twenty chips are often used in order to allow for die-to-to-edge difference and calculation error. When working with the same thickness die, die variations are homogenised. In the first step, the input stage of a synthesizer circuit, twenty VCO chips are studied with respect to frequency spectrum, RF output power, RF output amplitude, and phase noise.

In the second stage, 20 thin and dice chips are diced into four separate die-sub tier thicknesses: thin chips with 50-μm substrate, thin chips with 35-μm substrate, thin chips with 16.5-μm, and thin dice chips with a 25-μ thickness. Each thinned die is fixed on a thermal-release wafer, and has a temporary handle for assembly with ultra-thin ICs added for use in a process just in case.

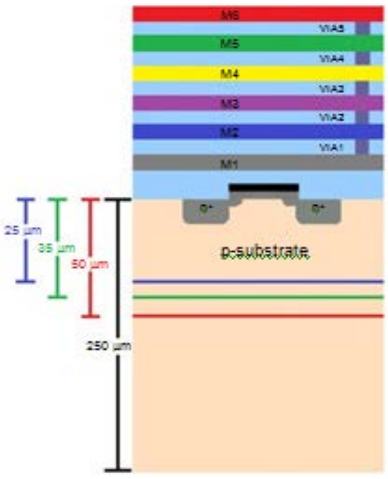

FIG. 1 THE FOLLOWING PICTURE SHOWS THE LAYERED MAP FOR A 1-POLY 6-METAL 180 NM CMOS PROCESSING TECHNOLOGIES (THE FIGURE IS NOT TO SCALE).

The buffer-phase structure of the VCO is shown in Fig. 2 adjusting the frequency with the movable condenser; two NMOS transistors (TN3 and TN4) are used. To provide performance separation required in order to increase control performance of VCO and also for 50 to meet output impedance, a common-source blocker is used.

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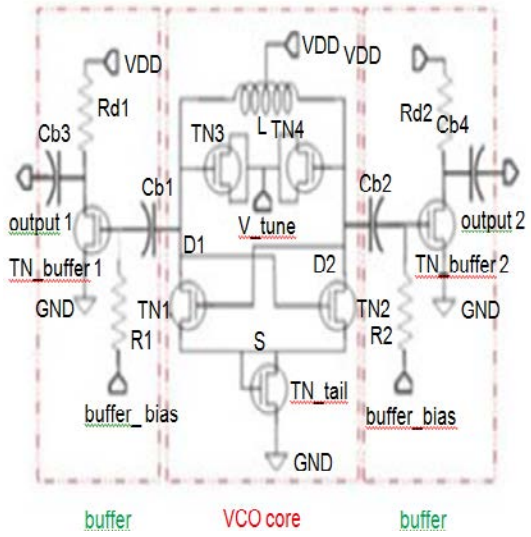

Fig 2 circuit schematic

III. CHARACTERISTICS

The Tektronix RSA3408B spectrum analyser was used to characterise all VCO chips. In terms of higher frequency range, RF output, noise and DC features, 20 VCO chips with the thickness of substrates of around 250 μM were characterised before die-substrate thinning. After

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de-incorporating a cable loss of 1.5 dB, the RF output power was evaluated at 978 MHz. Therefore, for each performance metric, the aggregate of those values is assigned as a reference. In (1), the die-substrate thickness factor (X) is defined so that the effect of a varied die-substrate thickness may be more clearly compared with the RF parameters observed.

$$X = log(T)/log(T0) \quad (1)$$

When T is the diameter substrata in μm, and T0 in μm is the default thickness of 250 μm in die-substrate. Fig. 3 indicate the standard deviation from the die-substrate thickness factor of VCO chips Fig. 3 (X). The VCO chip's working frequency is <1% for die-substratum thicken >25 μm. It is noticed. The different die-substrate thickness ranges, as illustrated in Fig. 4, were examined by applying the tuning voltage of 0–3.5 V. If a substrate thickness is greater than 25 μm, the tuning range for frequency is not much of a help. It is noticed. This figure shows a standardized RF power output deviation of the VCO chips against the X-thickening die-substrate factor. The output rates of the RF are seen to be 0.5 dB higher for the 50 μm, 1 dB higher for 35 μm and 1 dB higher for 25 μm, which shows strong practicality to flexible electronic applications. Fig. 6 shows a phase noise of the various thicknesses of the VCO chips. The divergence from the VCO phase noise with the default die-substrate thickness of 250 μm is found for die-substrate thickness >25 micrometer. This deterioration was considered mostly because the circuit components had a decreased quality factor (Q) as a result of ultra-dilution[6] Phase noise can also be well known to be extremely sensitive to the thickness of the die substrates owing to the leaking of the substrate. Table 1 summarizes the DC characteristics for different die substratum thicknesses for VCO chips. This indicates that for varied substratum thicknesses the DC parameters stay reasonably comparable. For a die-substratum

Relative standard deviation of the VCO and buffer drain currents for 20, 5, 5, and 5 chip samples were recorded at DC parameters of 250, 50, 35, and 25 μm. Five VCO chips were described, with a surface diameter of 15 μm.to reinforce the validity of this reliability study. However, the chips crushed during the characterization during testing, which implies that the thickness of the die substrates is minimal.

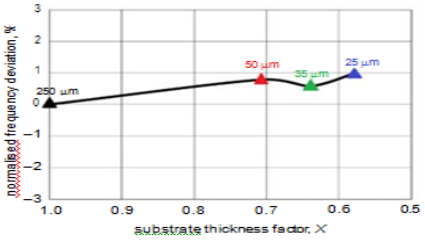

Fig. 3 Standard deviation in frequency of the VCO chips vs the thickness factor of the substrates (X)

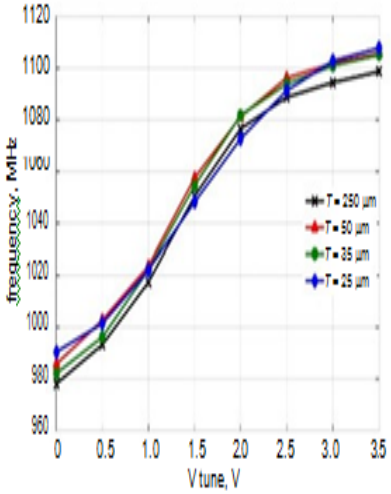

Fig. 4 VCO frequency tuning band of varied die-substrate thicknesses over tuning voltage

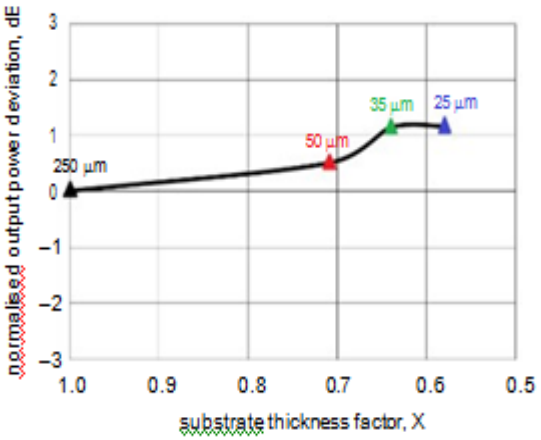

Fig. 5 RF normalised power output divergence from the die-substrate factor of the VCO chips (X)

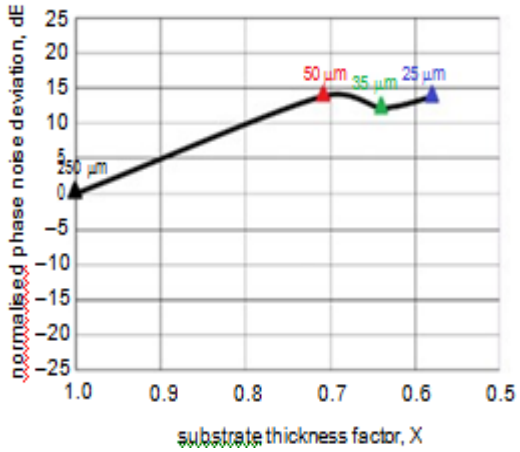

Fig. 6 Standard noise phase differentiation of VCO chips from thickness factor of the die-substrate (X)

TABLE I. CHARACTERIZATION OF DC ATTRIBUTES FOR VCO CHIPS WITH DIFFERENT DIE-SUBSTRATE THICKNESSES

Substrate thickness (µm)	VCO drain current		Buffer drain current	
	Average (mA)	Standard deviation (σ)	Average (mA)	Standard deviation (σ)
250	5.08	0.13	19.47	0.27
50	4.64	0.26	19.73	0.17
35	4.73	0.06	20.30	0.09
25	4.50	0.10	19.70	0.11

IV. RESULTS AND DISCUSSION

Below figure shows the schematic implementation of our vco circuit in tanner s-edit

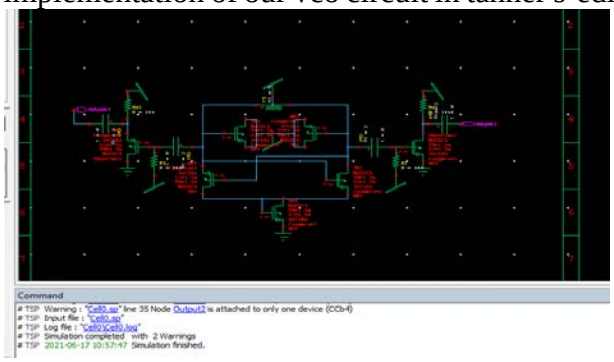

Fig 7 schematic implementation of circuit

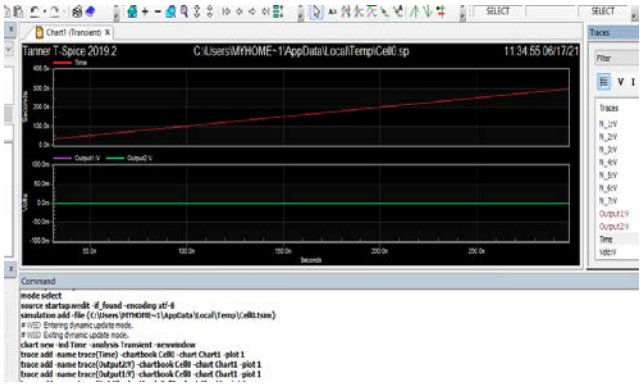

Fig 8 output waveforms of implementation

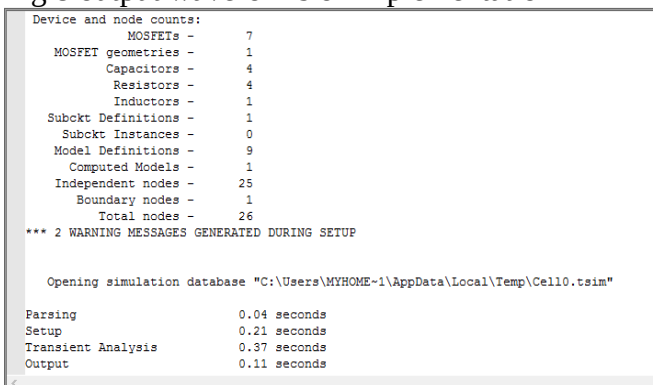

Fig 9 design report

V. CONCLUSION

Implementation of the CMOS RFIC for ultra-thin, scalable technological circuits is for the first time being accompanied by reliability studies for the first time. Studies were conducted and data was collected in order to find out how die-substrate thinning in a CMOS VCO, designed and fabricated in 180 nm CMOS processes, influences RF efficiencies, RF power output fluctuation, phase noise variation, and DC characteristics. Due to the dilution approach, the VCO's efficiency has been lowered, with the result that the oscillatory frequency and power control have been impacted, for most applications in the RFIC, with Wireless Communications. There was major phase noise degradation. At the chip level this must be dealt with either by selecting SOI CMOS where a substratum from the functional circuit isolated or by filling protected dummy metals during RFIC design so that functional structures are more protected against the bulk CMOS substratum.

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