VSI BASED D-STATCOM IN A DISTRIBUTED POWER SYSTEM FOR ENHANCEMENT OF POWER QUALITY

B.Naveen Kumar[1], CH.Anishreddy[2], P.Saicharan Rao[3], M.Pradeep[4]
Geethanajli College of Engineering and Technology,
Cheerayal (V), Keesara (M), R.R.Dist, Telangana (INDIA)

Abstract

This paper proposes a new Voltage controlled distributed static compensator (D-STATCOM) operating in voltage-control operation mode (VCOM). The proposed scheme exhibits several advantages compared to traditional voltage-controlled D-STATCOM where the reference voltage is arbitrarily taken as 1.0p.u. The proposed scheme ensures that more accurate power quality is achieved at the load terminal during nominal operation, which is not possible in the traditional method. Also, the new D-STATCOM injects lower currents and, therefore, improves quality of power in the feeder and voltage-source inverter (VSI). Promote, a more saving in the rating of D-STATCOM is achieved which improves its capacity to mitigate voltage-sag. Nearly UPF is maintained, while regulating voltage at the load end, during change in load. This model of D-STATCOM is incorporated with an advanced PI controller for fast load voltage regulation during voltage sags and swells. With these features, this scheme allows D-STATCOM to deal with power-quality issues by providing harmonic elimination, power factor correction, load balancing and voltage regulation based on the load requirement. Simulation and experimental results are presented to show the efficacy of the proposed algorithm.

Index Terms: Current control operation mode (CCOM), power quality (PQ), voltage-control operation mode(VCOM), voltage-source inverter(VSI).

I.INTRODUCTION

DISTRI voltage-related power-qual BUTION system suffers from current as well as ity (PQ) problems, which include poor power factor, distorted source current, and voltage disturbances [1], [2]. A D-STATCOM, connected at the point of common coupling (PCC), has been utilized to mitigate both types of PQ problems [2]–[12]. When operating in current control mode (CCOM), it injects reactive and harmonic components of load currents to make source currents balanced, sinusoidal, and in phase with the PCC voltages [3]–[7]. In voltage-control mode (VCOM) [2], [8]–[12], the D-STATCOM regulates PCC voltage at a reference value to protect critical loads from voltage disturbances, such as sag, swell, and unbalances. However, the advantages of CCOM and VCOM cannot be achieved. In CCOM, the Static compensator cannot compensate for disturbances in volatage. Hence, CCOM operation of D-STATCOM is not useful under

voltage disturbances, which is a major disadvantage of this mode of operation [13]. Traditionally, in VCOM operation, the D-STATCOM regulates the PCC voltage at 1.0 p.u. [2], [8]–[11]. However, a load works satisfactorily for a permissible voltage range [14]. Hence, it is not necessary to regulate the PCC voltage at 1.0 p.u. While maintaining 1.0-p.u. voltage, D-STATCOM compensates for the voltage drop in feeder. For this, the compensator has to supply additional reactive currents which increases the source currents. This increases losses in the voltage-source inverter (VSI) and feeder. Another important aspect is the rating of the VSI. Due to increased current injection, the VSI is de-rated in steady-state condition. Consequently, its capability to

mitigate deep voltage sag decreases. Also, UPF cannot be achieved when the PCC voltage is 1 p.u. In the literature, so far, the operation of D-STATCOM is not reported where the advantages of both modes are achieved based on load requirements while overcoming their demerits. This paper considers the operation of D-STATCOM in VCOM and proposes a control algorithm to obtain the reference load terminal voltage. This algorithm provides the combined advantages of CCOM and VCOM. The UPF operation at the PCC is achieved at nominal load, whereas fast voltage regulation is provided during voltage disturbances. Also, the reactive and harmonic component of load current is supplied by the compensator at any time of operation. The deadbeat predictive controller [15]–[17] is used to generate switching pulses. The control strategy is tested with a three-phase four-wire distribution system. The effectiveness of the proposed algorithm is validated through detailed simulation and experimental results.

II. DSTATCOM STRUCTURE AND CONTROLLER DESIGN IN CCOM AND VCOM

Fig. 1 shows the power circuit diagram of a DSTATCOM connected at a point of common coupling (PCC). It is realized by a three-phase four-wire VSI with two dc-link capacitors [11]. An LC filter is connected between the VSI and PCC. The shunt capacitor, i.e., Cfc, connected across the PCC helps in

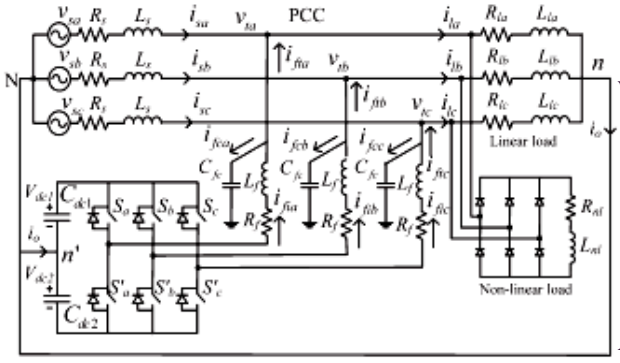

Fig. 1. Three-phase circuit of DSTATCOM in a distribution system.

the elimination of high-switching frequency components and prohibits them from entering the source. Voltages across both the dc capacitors Cdc1 = Cdc2 = Cdc are maintained at a constant value Vdc1 = Vdc2 = Vdc. Source voltages, PCC voltages, load currents, source currents, and filter currents are vsj, vlj, ilj, isj, and iftj, respectively, with j = a, b, c as three phases.

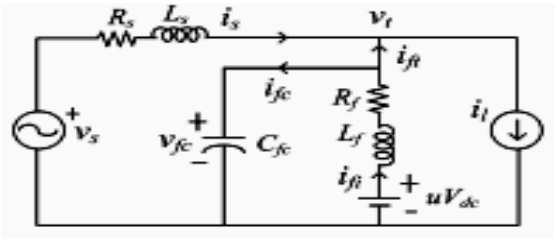

Fig. 2. Single-phase equivalent circuit of DSTATCOM in a distribution system.

A. SYSTEM MODELING AND DEVELOPMENT OF SWITCHING STRATEGY

The VSI topology used in this work provides independent control of each leg of the VSI [17]. This makes modeling of the single-phase circuit shown in Fig. 2 sufficient to explain the operation. The output voltage of the VSI is represented by uVdc. The term u is a switching control variable (with a value of +1 or -1). The state-space equation for this circuit is given as follows:

$$\dot{x} = A\,x + B\,z \qquad (1)$$

where

$$A = \begin{bmatrix} 0 & 1/C_{fc} & 0 \\ -1/L_f & -R_f/L_f & 0 \\ -1/L_s & 0 & -R_s/L_s \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & -1/C_{fc} & 0 \\ V_{dc}/L_f & 0 & 0 \\ 0 & 0 & 1/L_s \end{bmatrix}$$

$x = [v_{fc} \quad i_{fi} \quad i_s]^t$, $z = [u \quad i_{ft} \quad v_s]^t$.

A discrete form of the continuous-state equation is given as follows [2]:

$$x(k+1) = G\,x(k) + H\,z(k) \qquad (2)$$

where G and H are sampled matrices with a sampling time of Td. For small sampling time, matrices G and H are calculated as in the equation shown at the bottom of the page.

$$G = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} = e^{AT_d} \approx I + AT_d + \frac{A^2T_d^2}{2}$$

$$= \begin{bmatrix} 1 - \frac{T_d^2}{2L_fC_{fc}} & \frac{T_d}{C_{fc}} - \frac{T_d^2R_f}{2L_fC_{fc}} & 0 \\ -\frac{T_d}{L_f} + \frac{R_fT_d^2}{2L_f^2} & 1 - \frac{R_fT_d}{L_f} - \frac{T_d^2}{2L_f}\left[\frac{1}{C_{fc}} - \frac{R_f^2}{L_f}\right] & 0 \\ -\frac{T_d}{L_s} + \frac{R_sT_d^2}{2L_s^2} & \frac{T_d^2}{2L_sC_{fc}} & 1 - \frac{R_sT_d}{L_s} - \frac{R_s^2T_d^2}{2L_s^2} \end{bmatrix}$$

$$H = \begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_0^{T_d} e^{A\lambda} B\, d\lambda \approx$$

$$\approx \int_0^{T_d} (I + A\lambda)\, B\, d\lambda = \begin{bmatrix} \frac{T_d^2V_{dc}}{2L_fC_{fc}} & -\frac{T_d}{C_{fc}} & 0 \\ \frac{V_{dc}}{L_f}\left(T_d - \frac{R_fT_d^2}{L_f}\right) & \frac{T_d^2}{2L_fC_{fc}} & 0 \\ 0 & \frac{T_d^2}{2L_sC_{fc}} & \frac{1}{L_s}\left(T_d - \frac{R_sT_d^2}{2L_s}\right) \end{bmatrix}$$

With one switching variable, the VSI can control only one reference at a time. Hence, it is assumed that ui(k) and uv(k) are switching variables for CCM and VCM, respectively, at the kth sampling. These are calculated as follows.

1) Generation of Current Control Law:

The filter current at the (k + 1)th sampling instant, from (2), is given as follows:

$$i_{fi}(k+1) = G_{21}v_{fc}(k)+G_{22}i_{fi}(k)+H_{21}u_i(k)+H_{22}i_{ft}(k). \quad (3)$$

When (3) is implemented, each switching state gives a different current prediction. In other words, each switching strategy requires future current through the insulated-gate bipolar transistor (IGBT), which is unknown at the kth sampling. Therefore, a cost function (J) is defined as follows [11]:

$$J=[i_{fi}(k+1)-i^*_{fi}(k+1)]^2 \quad (4)$$

where $i^*_{fi}(k+1)$ is the reference current at the $(k+1)^{th}$ sampling. To minimize the cost function, it is differentiated with respect to ui(k) and equated to zero. Finally, J is minimum at

$$i_{fi}(k + 1) = i^*_{fi}(k + 1). \quad (5)$$

The reference current control law is obtained after replacing (5) in (3). However, it can be noticed that (3) contains future reference current $i^*_{fi}(k + 1)$, which is unknown. To know the future value of any signal in the discrete domain when sampling time is constant, extrapolation is used, which predicts the future value using known values of previous sampling instants. The order of extrapolation depends upon the sampling period. The lesser the sampling period, the higher the extrapolation will be, and vice versa.

To know $i^*_{fi}(k + 1)$, the following Lagrange's extrapolation formula is used [18]:

$$i^*_{fi}(k+1) = \sum_{l=0}^{n}(-1)^{n-1}\binom{n+1}{l} i^*_{fi}(k+l-n). \quad (6)$$

For second-order extrapolation, n is replaced by 2 in (6), and a linear prediction is given as

$$i^*_{fi}(k + 1) = 3\, i^*_{fi}(k) - 3\, i^*_{fi}(k - 1)+ i^*_{fi}(k - 2) \quad (7)$$

The expression for reference current, i.e., $i^*_{fi}(k + 1)$, is valid for a wide frequency range and, when substituted in (3), yields to one-step-ahead deadbeat current control law. The reference current control law from (3), (5), and (7) is given as

$$u_i^*(k) = \frac{i^*_{fi}(k+1) - G_{21}v_{fc}(k) - G_{22}i_{fi}(k) - H_{21}i_{ft}(k)}{H_{22}}. \quad (8)$$

2) Generation of Voltage Control Law: From (2), the capacitor voltage at the (k + 1)th sampling instant will be

$$v_{fc}(k+1)=G_{11}v_{fc}(k)+G_{12}i_{fi}(k)+H_{11}u_v(k)+H_{12}i_{ft}(k). \quad (9)$$

The procedure for obtaining $u^*_i(k)$ is followed to obtain the reference voltage control law. It is given as

follows:

$$u*v(k) = vfc(k+1) - G11vf\,c(k) - G12if\,i(k) - H12if\,t(k) \quad H11 \quad (10)$$

where

$$vf\,c(k+1) = vt*(k+1)v*t\,(k+1) = 3vt*(k) - 3vt*(k-1) + vt*(k-2). \quad (11)$$

The reference control laws, i.e., $u* i(k)$ and $u* v(k)$, are converted into corresponding VSI switching commands using deadbeat current and voltage controller, respectively [2]. The deadbeat predictive control scheme provides stable and robust operation of the system with excellent dynamic performance [19]–[21]. The stability of the system can be verified by applying the z-transform, where the transfer function of the system in the z-domain is given as follows [22]:

$$x(z)\,u(z) = (zI - G)\text{-}1H. \quad (12)$$

In the above transfer function, all the components of matrices G and H are known. Moreover, the term I represents the unit matrix. Now, the stability of the deadbeat predictive control scheme is found by analyzing the poles of the above transfer function. It is found that all the poles of the transfer function lie within the unit circle. Therefore, the scheme used in this work satisfies the stability criterion.

B. CONTROL OF DC-LINK VOLTAGE

The DSTATCOM remains operational without taking any real power from the source. However, the dc-link voltage continuously decreases due to the losses in the inverter. Therefore, a control loop is required to maintain the capacitor voltage at a reference value by compensating its losses. It is achieved by taking small real power from the source. The capacitor voltage control in CCM and VCM is achieved as follows.

1) Control of DC-Link Voltage in CCM: Let the total losses in the VSI be represented by Ploss. These losses must be supplied by the source for keeping the dc-link voltage constant. These are computed using a proportional–integral (PI) controller at positive zero crossing of phase-a voltage. It helps in maintaining the dc-link voltage (vdc1 + vdc2) at a predefined reference value (2Vdcref) by drawing a set of balanced currents from the source and is given as

$$Ploss = Kpc\,evdc + Kic \int evdc\,dt \quad (13)$$

where Kpc, Kic, and evdc = 2Vdcref - (vdc1 + vdc2) are the proportional gain, the integral gain, and the voltage error of the PI controller, respectively.

2) Control of DC-Link Voltage in VCM: The average real power at the PCC (Ppcc) is the sum of average load power (Plavg) and VSI losses (Ploss). The power, i.e., Ppcc, is taken from the source depending upon the angle between source and load voltages, i.e., load angle δ. The VSI losses arecompensated by taking small real power, i.e., Ploss, from the source. If capacitor voltage is regulated to a reference value, then in a steady-state condition, Ploss is a constant value and forms a fraction of Ppcc. Thus, δ is also a constant value. Once the operation mode of DSTATCOM is transferred to VCM, the dc-link voltage is regulated by generating a suitable value of δ. The total dc-link voltage (vdc1 + vdc2) is compared with a reference voltage, and error is passed through a PI controller. The output of the PI controller, i.e., δ, is given as

$$\delta = K_{pv}\,e_{vdc} + K_{iv} \int e_{vdc}\,dt \quad (14)$$

where Kpv and Kiv are the proportional and integral gains of the PI controller, respectively. For stable operation, the value of δ must lie from 0◦ to 90◦. Consequently, controller gains are quite small and are chosen carefully.

C. GENERATION OF REFERENCE QUANTITIES

1) Generation of Reference Filter Currents: The performance of a DSTATCOM in CCM

mainly depends upon the generation of reference filter currents. In this paper, reference filter currents (i∗ fta, i∗ ftb, and i∗ ftc) are generated using the instantaneous symmetrical component theory, as follows [2]:

$$\begin{aligned} i^*_{fta} &= i_{la} - i^*_{sa} = i_{la} - \frac{v^+_{ta1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \\ i^*_{ftb} &= i_{lb} - i^*_{sb} = i_{lb} - \frac{v^+_{tb1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \\ i^*_{ftc} &= i_{lc} - i^*_{sc} = i_{lc} - \frac{v^+_{tc1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \end{aligned} \quad (15)$$

where Δ+ 1 = j=a,b,c (vtj +1)2. Losses in the inverter, i.e., Ploss, are calculated using the PI controller, as given in (13). The average load power, i.e., Plavg, is calculated using a moving-average filter, as follows:

$$P_{lavg} = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{ta}i_{la} + v_{tb}i_{lb} + v_{tc}i_{lc})\, dt \quad (16)$$

where terms t1 and T are arbitrary time instant and time period, respectively. The voltages vta +1, vtb +1, and vtc +1 are maintained at the PCC and, hence, are reference voltages of shunt capacitors. Reference currents through these capacitors lead their respective terminal voltages by 90◦. Therefore, reference currents through these capacitors are computed as follows:

$$\begin{bmatrix} i^*_{fca} \\ i^*_{fcb} \\ i^*_{fcc} \end{bmatrix} = j\,\omega\, C_{fc} \begin{bmatrix} v^+_{ta1} \\ v^+_{tb1} \\ v^+_{tc1} \end{bmatrix}. \quad (17)$$

Finally, reference currents of the VSI will be given as

$$\begin{bmatrix} i^*_{fia} \\ i^*_{fib} \\ i^*_{fic} \end{bmatrix} = \begin{bmatrix} i^*_{fta} \\ i^*_{ftb} \\ i^*_{ftc} \end{bmatrix} + \begin{bmatrix} i^*_{fca} \\ i^*_{fcb} \\ i^*_{fcc} \end{bmatrix}. \quad (18)$$

Deadbeat current predictive control as given in (8) is used to realize these currents using the VSI.

2) Generation of Reference Load Voltages:

DSTATCOM compensates voltage disturbances by injecting reactive currents. To keep the filter current at a minimum, the load voltages are maintained at 0.9 and 1.1 p.u. during sag and swell, respectively. This improves the voltage regulation capability of DSTATCOM compared with conventional VCM, where the load voltage magnitude is set at 1.0 p.u.
By knowing the zero crossing of phase-a source voltage,
choosing a suitable reference load voltage magnitude (Vt∗), and computing the load angle from (14), the three-phase reference load voltages are given as follows:
v∗ta =√2 Vt∗ sin(ωt - δ)

vtb ∗ =√2 Vt∗ sin(ωt - 2π/3 - δ)

v∗tc =√2 Vt∗ sin(ωt + 2π/3 - δ)
(19)

Where ω is the system frequency. These voltages are realized by the VSI using deadbeat voltage predictive control law given in (10).

III. CONTROL STRATEGY

Generally, loads perform satisfactorily within the ±10% range of the nominal voltage (i.e., 0.9–1.1 p.u.), also called normal operating conditions. In these conditions, current-related PQ problems are of main concern. Therefore, the DSTATCOM is operated in CCM for load harmonic and reactive current compensation (see Fig. 3). It results in balanced and sinusoidal source currents with a unity power factor at the PCC.

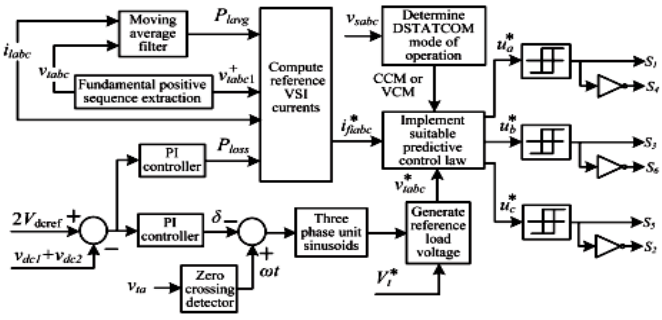

Fig. 3. Control block diagram of the proposed interactive DSTATCOM.

However, the load voltage can change at any time due to voltage disturbances. This will result in performance deterioration of the sensitive loads, making CCM operation of

DSTATCOM redundant. In this case, DSTATCOM must switch to VCM from CCM to protect sensitive loads from these unwanted variations in voltage by maintaining a constant voltage at the load terminal. Here, a control algorithm for flexible mode transfer between CCM to VCM, and vice versa, has been presented. The control block diagram for the proposed system is given in **Fig. 3.**

IV. SIMULATION RESULTS

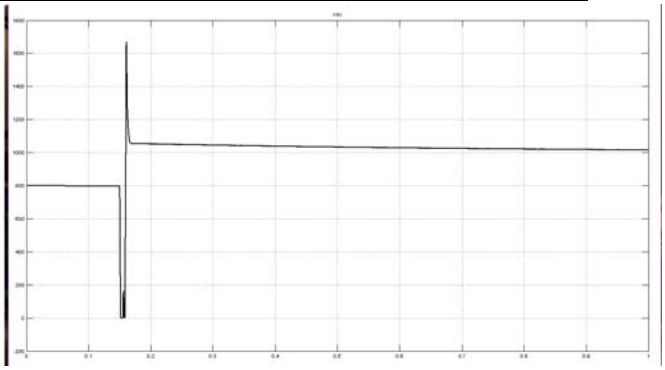

Fig.6.Simulation results of Vdc.

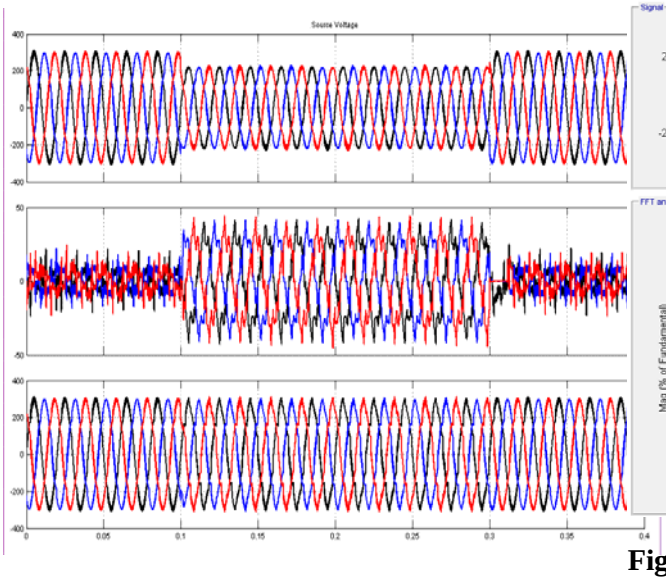

Fig.4.Simulation results of Source Voltage, Injected Voltage and Load voltage during Sag.

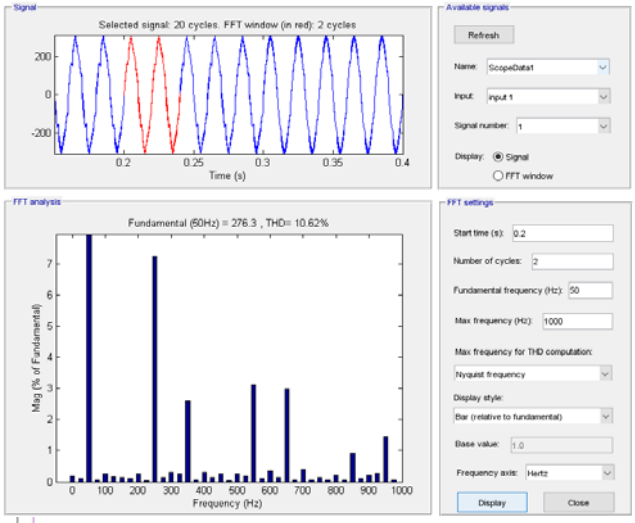

Fig.7.THD for Load Voltage

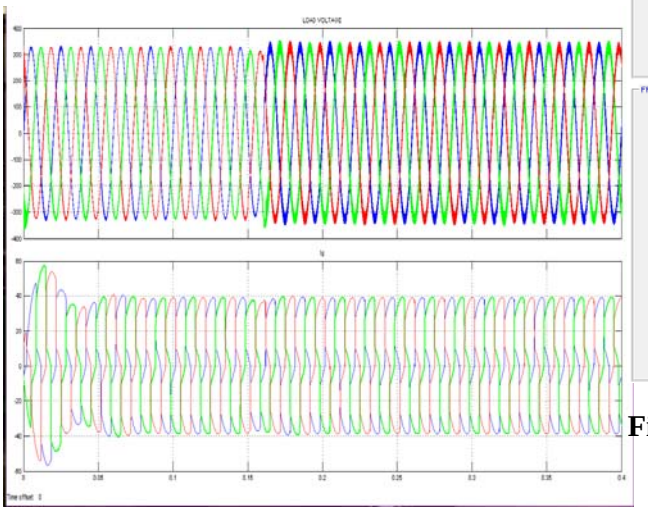

Fig.5.Simulation results of Load voltage during Swell.

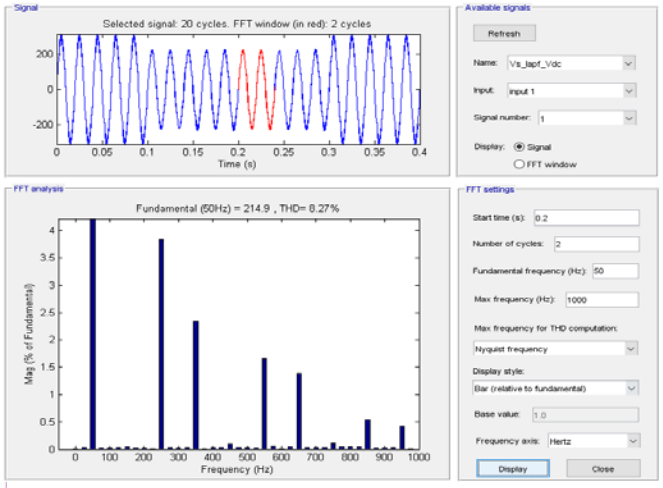

Fig.8.THD for Source Voltage.

CONCLUSION

This paper has presented the Design of VSI STATCOM to improve the power quality in Distributed power system. STATCOM system is an efficient mean for mitigation of PQ

disturbances introduced to the grid. VSI based STATCOM compensator is a flexible device which can operate in current control mode for compensating voltage variation, unbalance and reactive power and in voltage control mode as a voltage stabilizer. The latter feature enables its application for compensation of dips coming from the supplying network. The simulation results show that the performance of STATCOM system has been found to be satisfactory for improving the power quality at the consumer premises. Rectifier-based non-linear loads generated harmonics are eliminated by STATCOM. When single-phase rectifier loads are connected, STATCOM currents balance these unbalanced load currents. Finally, Matlab/Simulink based model is developed and simulation results are
presented.

REFERENCES

[1] A Novel Hysteresis control Technique of VSI based STATCOM , R.A.Kantaria1, Student Member, IEEE, S.K.Joshi2, K.R.Siddhapura3

[2] G.Yalienkaya, M.H.J Bollen, P.A. Crossley, "Characterization of Voltage Sags in Industrial Distribution System", IEEE transactions on industry applications, volume 34, No. 4, July/August, PP.682- 688, 1999.

[3] „A Novel DC voltage Detection Technique CHB- Inverter based STATCOM"Yidan Li and Bin Wu, Fellow, IEEE

[4] Haque, M.H., "Compensation Of Distribution Systems Voltage sags by DVR and D-STATCOM", Power Tech Proceedings, 2001 IEEE Porto, Volume 1, PP.10-13, September 2001.

[5] Anaya-Lara O, Acha E., "Modeling and Analysis Of Custom Power Systems by PSCAD/EMTDC", IEEE Transactions on Power Delivery, Volume 17, Issue: 2002, Pages: 266-272.

[6] Bollen, M.H.J.,"Voltage sags in Three Phase Systems", Power Engineering Review, IEEE, Volume 21, Issue :9, September 2001, PP: 11-15.

[7] M.Madrigal, E.Acha., "Modelling OF Custom Power Equipment Using Harmonics Domain Techniques",IEEE 2000.

[8] R.Meinski, R.Pawelek and I.Wasiak, "Shunt Compensation For Power Quality Improvement Using a STATCOM controller Modelling and Simulation", IEEE Proce, Volume 151, No. 2, March 2004.

[9] J.Nastran , R. Cajhen, M. Seliger, and P.Jereb,"Active Power Filters for Nonlinear AC loads, IEEE Trans.on Power Electronics Volume 9, No.1, PP: 92-96, Jan 2004.

[10] L.A.Moran, J.W. Dixon , and R.Wallace, A Three Phase Active Power Filter with fixed Switching Frequency For Reactive Power and Current Harmonics Compensation, IEEE Trans. On Industrial Electronics. Volume 42, PP:402-8, August 1995.

[11] Cai Rong, Analysis of STATCOM for Voltage Dip Mitigation. Sweden ISSN 1401-6184 M.Sc. No. 1EEE, December 2004

[12] Wahidah AbdulHalim, Aida Fazliana Abdul Kadir, Jurifa Mat Lazi, Steady StatePerformance of Static Synchronous Compensator (STATCOM)

[13] Bhim Singh, Senior Member, IEEE, Alka Adya, A.P.Mittal, Member, IEEE, and J.R.P. Gupt, Modeling, Design and Analysis of Different Controllers for DSTATCOM. 978-1-4244-1762-9/08/$25.00 C2008 IEEE.

[14] Cunping Wang, Xianggen Yin, Minghao Wen, Jian Liu, Qing Xiong, and Bin Zhang, 2010 Structure and Parameters Design of Output LC Filter in D-STATCOM. 97S-1-4244-5940-7110/$26.00©2010 IEE

[15] Hendri Masdi, Norman Mariun1 Senior MIEEE, S.M.Bashi MIEEE, A. Mohamed Senior MIEEE, Sallehhudin Yusuf MIEEE, Design of a prototype D-STATCOM for volstage sag mitigation.

[16] K R Padiyar and A M Kulkarni, Flexible AC transmission systems: A status review

[17] G.Sundar, Digital simulation of dstatcom for voltage fluctuation et. al. / International

[18] Haque, M.H.," Compensation of distribution system voltage sag by DVR and D-STATCOM", Power Tech Proceedings, IEEE Porto, vol.1, pp.10-13, Sept, 2001.