PARALLEL SELF TIMED ADDER USING MACH-ZEHNDER INTERFEROMETER

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Abstract

In digital signal processors and microprocessors, adder circuits plays a crucial role. Due to ultra high speed and less power consumption, optical circuits are used in many telecommunications and computer networks for transmitting information. In this study, the parallel self-timed adder is implemented by using Mach-Zehnder Interferometer technique expected to its fast switching time. Simulation and synthesis of MZI based PASTA adder are done by Xilinx ISE tool.

Index Terms: Beam combiner, Beam splitter, LUT, MZI, PASTA, SOA

I. INTRODUCTION

An asynchronous circuit is also familiar as Self Timed Circuit. This is a successive digital logic circuit that is not supervised by any clock circuit. Instead of the clock, it manages signals that specify completion of commands and operations by easy data transferring protocols. In digital logic design, in asynchronous circuits active areas are researched as they are faster, has low electromagnetic disturbance and effective modularity in an extensive system.

In optical computing, Mach-Zehnder Interferometer is one of the efficient configurable building blocks. By using this MZI, the parallel self-time adder is implemented. In optical computing the primary functions required in computing are as follows:

1. Switching
2. Arithmetic operations
3. Storage.

Looking to the advantages of Mach-Zehnder Interferometer such as small size, thermal stability, fast switching time, ease of fabrication and low power consumption this can be utilized in many applications.

The multiplexer circuit which integrates with many inputs but gives only one output. Multiplexer handle the two types of data i.e.

1. Analog data
2. Digital data

Relays and transistor switches are replaced to build the multiplexer for the analog application. In digital application, these are built to from ideal logic gates.

In this report, multiplexer is designed using Mach Zehnder Interferometer technique is implemented in parallel self-timed adder for fast response.

Verilog Hardware description language is used to write the RTL coding for the schematic [4]. HDL's are utilized to describe the behavior or functionality of the circuit.

The rest of the work is described in the following sections. Section II presents a brief review on the PASTA adder and block diagram of the PASTA adder. The section III presents the proposed MZI technique and its working and then follows the experimental analysis and conclusion.

II PASTA ADDER

The objectives of pasta use half adders and multiplexers for minimum interconnection. In this recursive formulation method is used for binary addition and operation is performed in parallel for the bits that doesn't require any carry chain propagation [1].

A. ARCHITECTURE OF PASTA ADDER

The basic schematic diagram of parallel self-time adder is shown in fig 1.

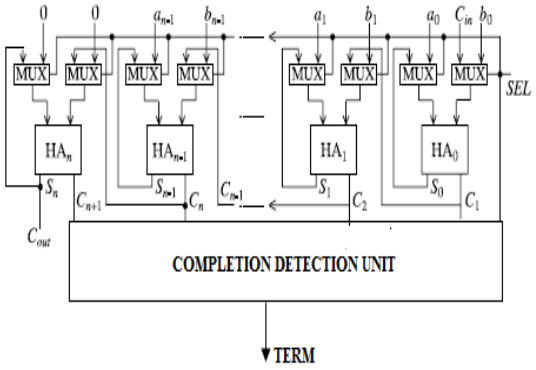


Fig 1: Block Diagram of PASTA Adder

The architecture includes the basic blocks such as

1. Half Adder
2. Multiplexer
3. Completion Detection Circuit

B. DESCRIPTION OF BLOCK DIAGRAM

Initially, the inputs are set to the multiplexer, as the multiplexer works based on the selection line the inputs are selected and output are generated. The generated output from the multiplexer is given to the half adder. Half adder performs the addition between the two bits and it generates sum and carries. The completion detection unit displays the output placed on the carry output bits generated from the half adder. The logic diagram and truth table for half adder are present in fig 2 and table 1.

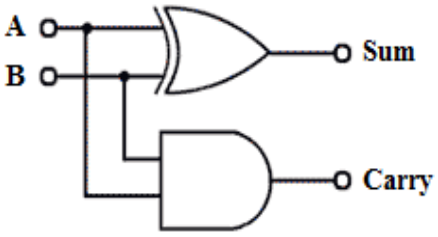


Fig 2: Logic Diagram of Half Adder

Table I: Truth Table of Half Adder

Input		Output	
A	**B**	**Sum**	**Carry**
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	1

III PROPOSED METHOD

In this method, MZI technique has been implemented which based on all-optical's that are designed using semiconductor amplifier (SOA) and two couplers as shown in fig 3. The input A is called an incoming signal and B is called as Control signal.[2].

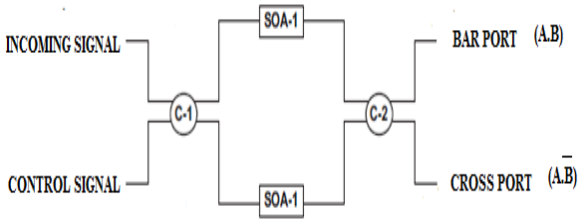


Fig 3: SOA Based MZI

A. WORKING PRINCIPLE OF MZI

Meanwhile, with the existence of incoming signal t port 'A' and control signal at port 'B', where a light would seen at the output bar port and light would not be seen at the output cross port.

When there is a presence of an incoming signal at port 'A' and absence of control signal at input port 'B', the light would be seen at the cross port and light would not seen at the output bar port.

B. MZI SWITCH

The MZI switch consists of two inputs and two outputs one of the output acts as cross port and other acts as bar port. The MZI switch is shown in fig 4.

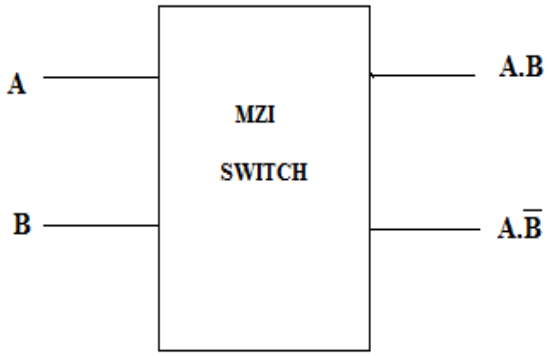


Fig 4: Block Diagram of MZI switch

The functionality of the MZI based optical switch can be written as

$$P=A \,\&\, B \quad (1)$$

$$Q=A \,\&\, (\sim B) \quad (2)$$

Where inputs A and B are incoming and control signals for the MZI switch and outputs P and Q are the bar port and cross ports of MZI. The truth table for the MZI switch is given in below table II.

Table II: Truth Table of MZI Switch

INPUT		OUTPUT	
A	**B**	**Bar Port**	**Cross Port**
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

C. BEAM SPLITTER (BS)

The beam splitter is used at the input side to split a beam of light into a couple of paths.

D. BEAM COUPLER (BC)

Beam coupler is also well known as a beam combiner. Beam combiner combines the two outputs of MZI switch to execute the functionality. Beam coupler performs simple or operation or functionality.

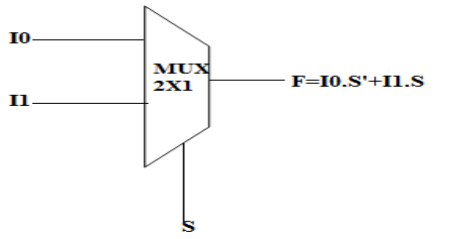
E. MULTIPLEXER DESIGN USING MZI SWITCH

As to the applications of MZI in various fields like quantum computation and quantum cryptography and in many other various fields, MZI technique is an appliance to design multiplexer [3].

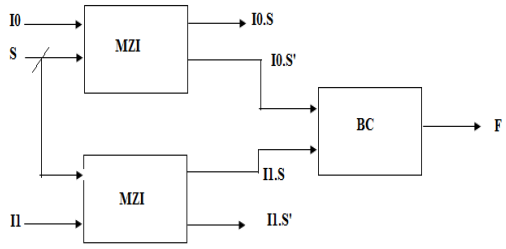
The 2x1 multiplexer truth table is shown in table III and multiplexer schematic diagram all-optical implementation of the multiplexer is shown in fig 5(a) and 5(b). It consists of the (BS) for splitting the select input s and MZI switches are used for generating the output function and the ultimate output F is generated by merging the outputs from the MZI switch using beam combiner.

Table III: Truth table of 2x1 Multiplexer

Selection Input S	Input I0	Input I1	Output F
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1



(a)



(b)

Fig 5: (a) schematic of the 2x1 multiplexer. (b) Optical execution of Multiplexer

F. MZI BASED PASTA ADDER

The block analysis for the MZI based PASTA adder is shown in fig 6. The multiplexer is succeeding with the 2x1 MZI multiplexer. The internal architecture has two MZI switches and one beam coupler to add the signals.

Self-timed circuits use request and acknowledge signal to process the input and output data. In this the selection lines act as the

request signal.

In the early phase when sel='0' the definite operands are firstly selected and when sel='1' it will change to feedback or carry paths to iterative phase. The flow chart for the architecture is shown in fig 7.

The equations for the sum and carry for the initial condition are

$$S = a \wedge b \quad (3)$$

$$C = a \,\&\, b \quad (4)$$

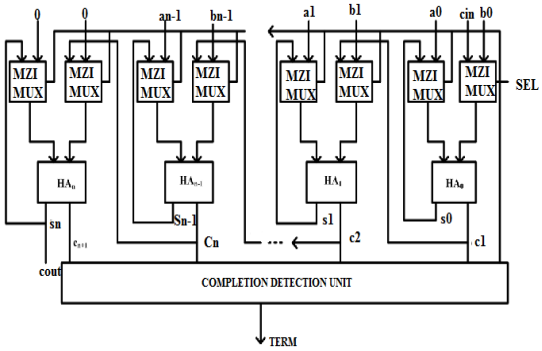


Fig 6: Block diagram of Proposed Architecture

IV. FLOW CHART

The flowchart describes the execution process of the parallel self-timed adder

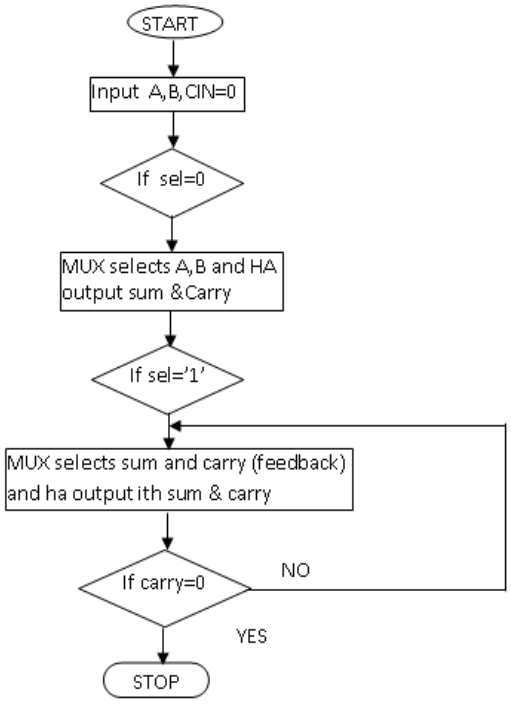


Fig 7: Flowchart of PASTA Adder

V. SIMULATION RESULTS OF PROPOSED METHOD

The results of the MZI based pasta adder are depicted below. The composition and simulation is executed using Xilinx ISE tool and in code implementation using Verilog HDL.

A. RTL SCHEMATIC OF PASTA ADDER USING MZI

The RTL diagrammatical representation for the 4-bit PASTA Adder is depicted in fig 8. RTL schematic can be viewed as a gate-level schematic.

The illustration is originated by the HDL synthesis Process. It displays the design with regards to generic blocks like adders, logic gates individual to the intended Xilinx device.

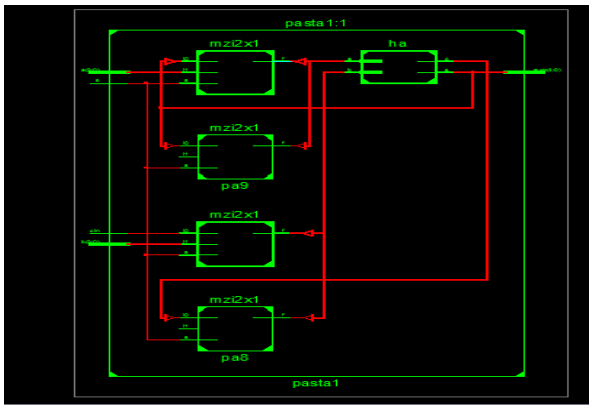


Fig 8: RTL schematic of 4-bit PASTA adder

B.TECHNOLOGY SCHEMATIC OF PASTA ADDER BY MZI

The technology schematic of PASTA adder is shown in fig 9. The architecture-specific schematic is viewed in Technology schematic. This is displayed using LUT, I/O buffers. Look up table (LUT) stores the predefined values in it. Basically, it determines the output for a given input.

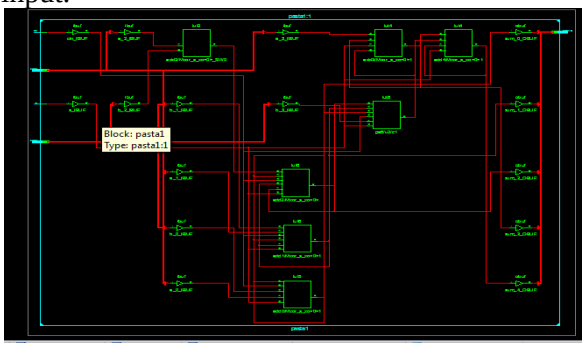


Fig 9: Technology Schematic of PASTA Using MZI

C. SIMULATION RESULTS OF PASTA ADDER USING MZI

The simulation result for the 4-bit adder is shown in figure 10. Here the inputs a and b are having 4-bit width. Consider input

a=0010

b=0100

cin=0 and selection s=0. According to the respective inputs the output sum =00110;

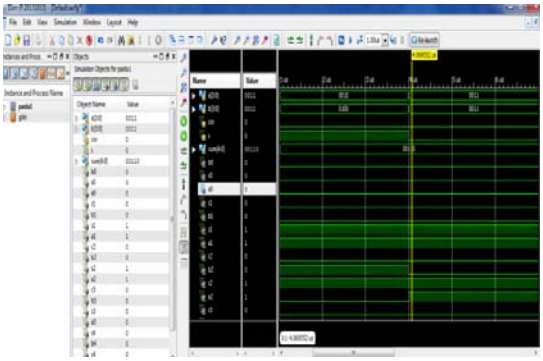


Fig 10: Simulation Results of 4-bit MZI PASTA Adder

D. SYNTHESIS REPORT

The synthesis report for the 4-bit pasta adder is given for in table III. The design properties for the below synthesis report are as follows:

Family Used: SPARTAN 6

Device: XC6SLX45

Package : CSG324

Speed: 2

Table III: Device Utilization Summary

Parameter	Available	Used
No. of slices LUT's	27288	7
No. of IO's	218	15
Delay	12.526 ns	

VI CONCLUSION

The scheme of parallel self-timed adder has been implemented successfully using Mach-Zehnder Interferometer technique using Verilog HDL. The operation is done in a parallel manner for individual carry chains. So this type of adders can be used in any optical computing where the arithmetic operations are performed.

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