# A DESIGN OF EDGE TRIGGERED FLIP FLOP WITH DYNAMIC THRESHOLD LOGIC FOR LOWPOWER VLSI DESIGN APPLICATIONS

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**Abstract**

**In this paper we are designed a Low Voltage and Low Power Master Slave negative edge triggered Flipflop and tested the same for synchronous 4-bit up counter and 4-bit SIPO Shift Register as VLSI applications. The master slave negative edge triggered flip-flop is designed using four transmissions gates and four inverters.. The main objective is to optimize the both circuits in terms of power and area. The circuit is completely implemented with transmission gates and operated at 400mV and the low power is achieved by operating transistors in below threshold level (Sub-Threshold) using Dynamic Threshold logic. The design is implemented using Cadence Virtuoso schematic editor and simulated using Cadence Virtuoso analog design environment at 180nm CMOS process technology. The counter and shifter are designed with 182 and 112 transistors respectively. The power consumed by the counter and shifter is 5.4µW and 1.7uW with power supply 400mV and 100ns rise time and fall time respectively. Both are operated at the frequency range of 0.1Hz – 1MHz**

**Keywords: Low power, Dynamic threshold, Master-slave D flip-flop, Transmission gate, Synchronous counter, Shift Register.**

## 1. INTRODUCTION

CMOS has been the dominant technology for VLSI design. As VLSI circuits continue to grow and Technologies evolve, the level of integration is increased as per Moore's law and higher clock speeds are achieved. Higher clock speeds, increased level of integration and technology scaling are causing unabated increase in power consumption; as a result, low power consumption is becoming a critical issue for modem VLSI circuits So Dynamic logic circuits are widely used in modern low power VLSI circuits. These dynamic circuits are becoming increasingly popular because of the speed advantage over static CMOS logic circuits; hence they are widely used today in high performance and low power circuits.

Flip flops are bistable elements which sample the data continuously whenever enable input occurs and plays major role in generating clock signal delays and processing of it other parts of digital circuit Fig.1 shows a conventional positive edge triggered delay flip flop.

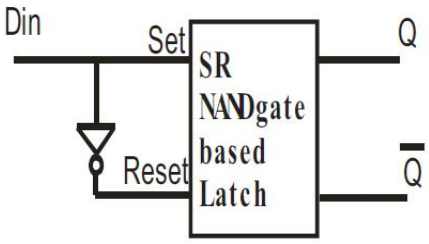


**Fig.1 Conventional positive edge triggered delay flip-flop**

However, current flowing through leaky transistors (OFF state) in the flip flop design may restrict the correct transition of the data input signal from input of the circuit to its output and also consumes large amount of power [2] from the supply as the number of active transistors in the conventional positive edge triggered SR latch based D Flip-Flop are large in number. The cross coupled feedback [2]

portion which is present in flip flops design causes significant amount of delay because of which the operational speed get reduced and incur an increase in power consumption. Power consumption is needed to get reduced significantly for improving flip flops performance [2]

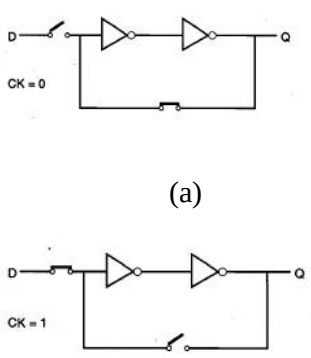


**Fig.2 Inverter based D Latch a) CLK=0 b)CLK=1**

The above fig.2 is another design of inverter based D Latch in which whenever a low pulse is applied to the clock signal (Clk) the output (Q) will hold the previous data. if Clk is high output will starts following the input data (D). But this conventional design consists of switches. In the proposed design all switches are replaced by Transmission gates. It is CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously.

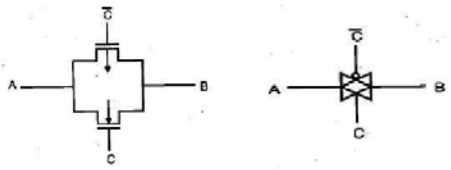


**Fig. 3 Transmission Gate & Symbol**

We will examine 4 bit Synchronous up counter, 4bit SIPO shift register and implement them using negative edge triggered Flip-Flops which is implemented with transmission gates with Dynamic Threshold logic designed in Cadence tool and targeting on design accents such as power, delay and area.

The paper is organized as follows: in section 2, Dynamic Threshold utilization is presented. In section 3, Proposed Master-Slave Flip-Flop and the schematic of all individual blocks with dynamic threshold logics are presented. In section 4, the simulation results are given and discussed. The area, power and delay of the counter and SIPO are estimated. Finally a conclusion will be made in the last section.

## *2.* BODY BIAS TECHNIQUE

### Dynamic Threshold Logic

During the past few years demand for low power and high performance digital systems has grown rapidly. The main approach for reducing power is depends on power supply scaling. Since reduction in power supply below threshold voltage will degrade the speed. However the lower limit for threshold voltage is set by the amount of off state leakage current that can be tolerated. To extend the lower bound of power supply we used a Dynamic Threshold Voltage MOSFET(DTMOS)with highest Vt at zero bias and lowest value at Vgs = Vdd.[9]

### Body Effect:

Body effects means rate of change of transistor threshold voltage resulting from voltage difference between transistor source and body. Generally the transistor body treat as a second gate there we can supply input also, and the supply plays major role to transistor turns ON and OFF. The strength of the substrate is defined by the factor of “gamma”. This strong body effect is a plays a key role in low power circuit operation for deep submicron CMOS technologies. For 65nm process technologies body effect is negligible with transistor scaling so for below 65nm body effect is diminished. Instead, the transistor bodies are generally connected along with the transistor source to either power (VDD) for p-channel or ground (VSS) for n-channel transistor.

### Dynamic Threshold Effect:

In this paper we designed a voltage divider arrangement to generate a forward body bias voltage/reverse body bias voltage as shown in fig. Reverse body bias means applying negative voltage to the body to source of n-type

transistor which increases the threshold voltage and makes the n-type transistor slow. Forward body bias means applying positive voltage to the body to source of n-type transistor which decreases the threshold voltage and makes the n-type transistor fast. The polarities of the applied bias described above are the opposite for a p-channel transistor. The use of dynamic body bias is an important role in mV, low-power circuit operation because it maintains sufficient transistor gate overdrive. At a given body bias, as the power supply voltage is lowered to reduce power consumption the gate overdrive is also reduced: Here we considered VT= 450 mV the gate overdrive is lowered from 600 mV to 400 mV as the power supply is lowered from 1.8 volts to 0.4 volts.

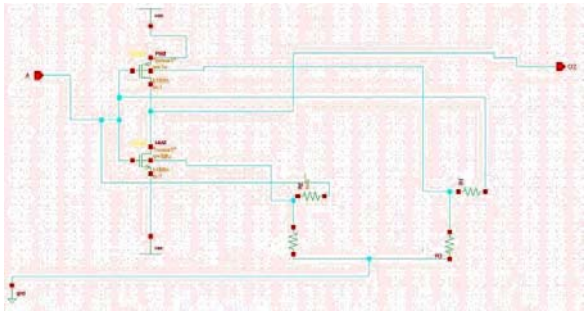

Fig4. GDI Inverter with Dynamic threshold logic

However, if the bulk voltage of the transistor is varied, its dc parameters will also change. This is because by changing the bulk voltage, threshold voltage of the transistor changes according to and the current equation will change from conventional equation

$$V_T = V_{T0} \pm \gamma\left(\sqrt{2|\varphi_F| - V_{BS}}\right) - \sqrt{2|\varphi_F|}$$

If Source to Bulk voltage is equal to zero the current equation becomes

$$I_D = u_0 C_{ox}(W/L)(V_{gs}-V_{th0})^2/2$$

where $V_{th0}$ is the threshold voltage of the transistor when its bulk-source voltage is zero, i.e., $V_{BS}$=0V. So Dynamic Threshold Logic is efficiently used in designing Transmission gates.

## 3. Master-Slave Negative edge triggered Flip-Flop

A master-slave negative edge triggered is proposed with Dynamic threshold logic which discussed above. It is connected with two D latch's in series and inverting the clock input to one of them for better results non overlapping clock generator is suggested. Negative edge triggered means input data is entered on the positive edge of the clock during this phase output doesn't reflect the output it responds at negative edge of the clock. The two stage Master-Slave edge triggered circuit shown in fig.4 which is constructed simply cascading the D latch circuit implemented with back to back GDI Inverter which consumes less power compared to Conventional Inverter

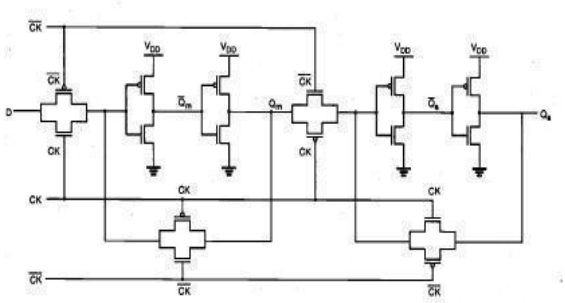

Fig.4 CMOS negative (falling) edge triggered master- slave D Flip-Flop

When the clock changes again from logic 0" to 1," the slave latch locks in the master latch output and the master stage starts sampling the input again. Thus, this circuit is a negative edge-triggered D flip- flop by virtue of the fact that it samples the input at the falling edge of the clock pulse.

The purpose of master-slave flip-flops is to protect a flip-flop's output from unexpected changes caused by glitches on the input. Master-slave flip-flops are used in applications where glitches may be prevalent on inputs. The master-slave configuration has the advantage of being pulse-triggered, making it easier to use in larger circuits.

### 3.1. Synchronous 4-Bit Up Counter

The synchronous 4-bit up counter has 3 AND gates, 4 EX-OR gates and 4 master-slave D flip-flops. Because of Synchronous same clock is given to each flip-flop. So for every clock pulse the counter counts one step up. It is an up counter and starts from 0000 to 1111. Q0 is the LSB and Q3 is the MSB.

The master-slave D flip-flop works at the negative falling edge of the clock. It stores the input at positive edge and it is given to the output at the negative edge of the clock. So change in counter output is observed in the negative edge of the clock. Enable and reset are the additional inputs to the counter.

Proposed Dynamic threshold operated master salve edge triggered D flip flop is used in the design of 4 bit synchronous up counter shown in the fig. 5

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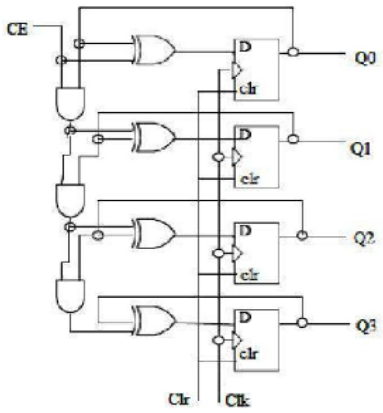



Fig. 5 Synchronous 4- bit Up Counter

### 3.2 SIPO Shift Register

The Shift Register is a type of sequential logic circuit that can be used for the storage or the transfer of data in the form of binary numbers. This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name "shift register".

A shift register basically consists of several single bit Flip flops, one for each data bit, either a logic "0" or a "1", connected together in a serial arrangement so that the output from one data latch becomes the input of the next latch and so on. Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration. The individual data latches that make up a single shift register are all driven by a common clock ( Clk ) signal making them synchronous devices.

Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required.

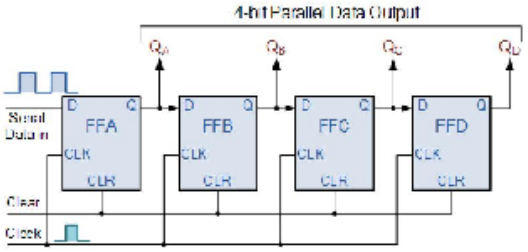
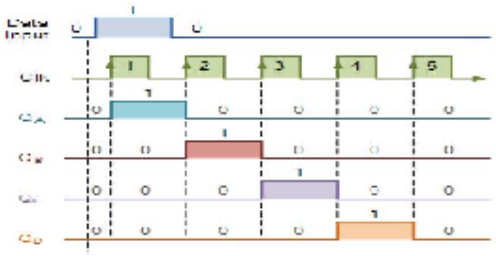



**Fig.6 SIPO 4-Bit Shift Register**
**Fig.7 Basic Data Movement through a Shift Register**

### 3.3 SCHEMATICS

The Synchronous 4-bit up counter and 4-bit SIPO shift register is designed in Cadence gpdk180 tool. The transistor level diagram is designed using Cadence Virtuoso schematic editor [2].

The design of the synchronous 4-bit up counter will be performed by implementing and creating instances of the components of the counter using Transmission gate based AND, EXOR and GDI Inverter and Dynamic threshold based Master slave negative edge triggered Flip-Flop.



The schematic diagram of all the components are designed using PMOS and NMOS transistors with Dynamic Threshold logic The schematic diagram of inverter, AND gate and EXOR gate are as shown in fig.8.

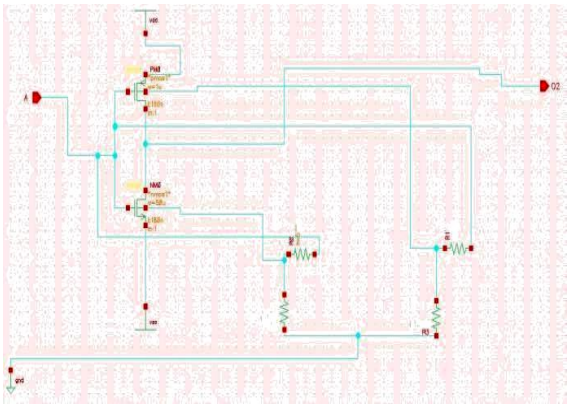


**Fig-8(a):** Inverter schematic with dynamic threshold diagram

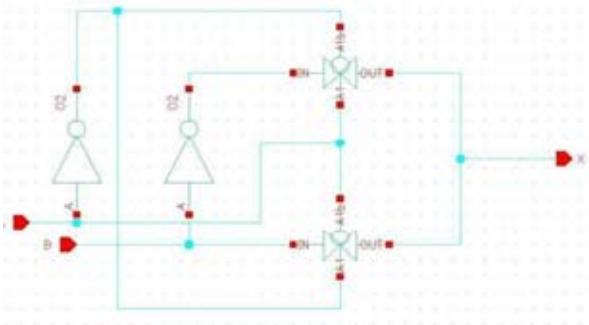


**Fig-8(b): AND gate schematic diagram**

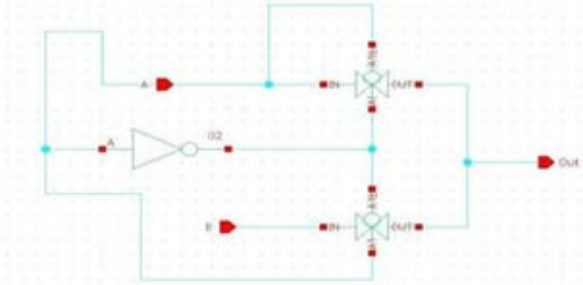


**Fig-8(c): XOR gate schematic diagram**

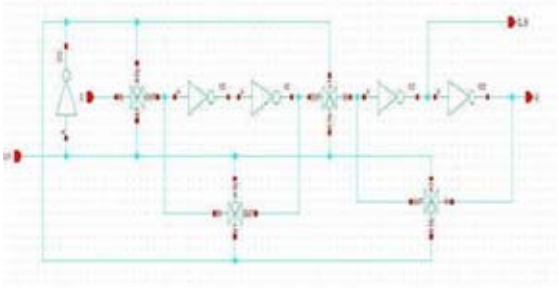


**Fig-8(d): Master slave D flip-flop schematic diagram**

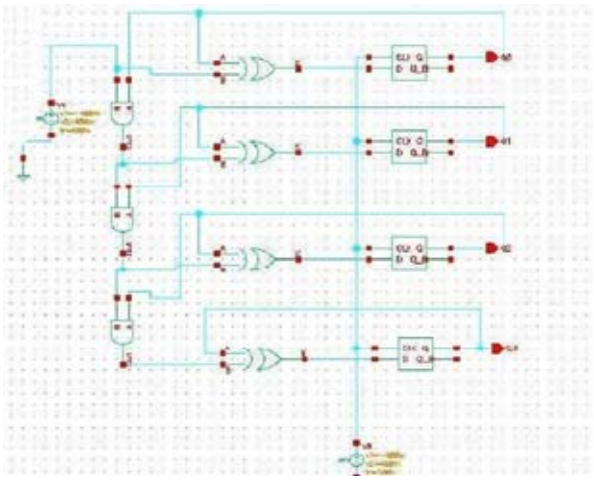


**Fig. 8(e): Synchronous 4-bit up counter schematic diagram**

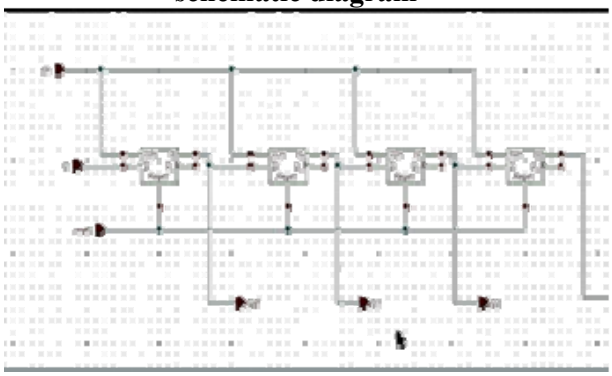


**Fig. 8(f): SIPO 4-bit Shift Register schematicdiagram**

## 4. SIMULATION RESULTS

The schematics of Transmission gate, inverter, AND, EXOR Gates, master-slave negative edge triggered D flip-flop and synchronous 4-bit up counter and 4 bit SIPO Shift register are simulated and the transient responses are analyzed using Cadence analog design environment. 4bit SIPO shift register is tested at different frequency levels 100,100K and 1MHz.

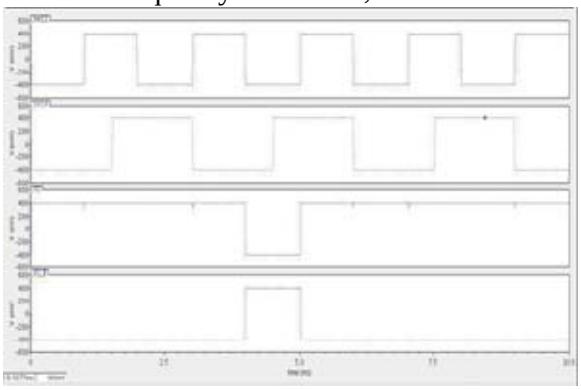


Fig-9(a): Transient response of D-Flip Flop

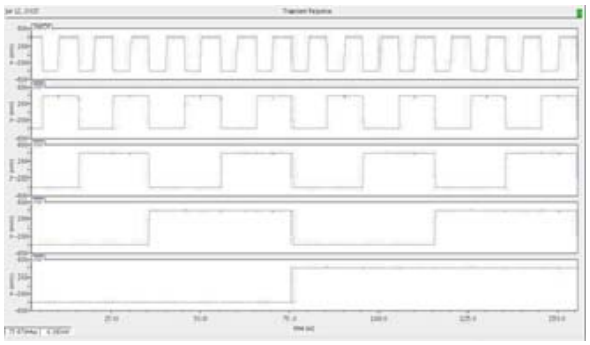


Fig-9(b): Transient response of 4 bit Synchronous counter

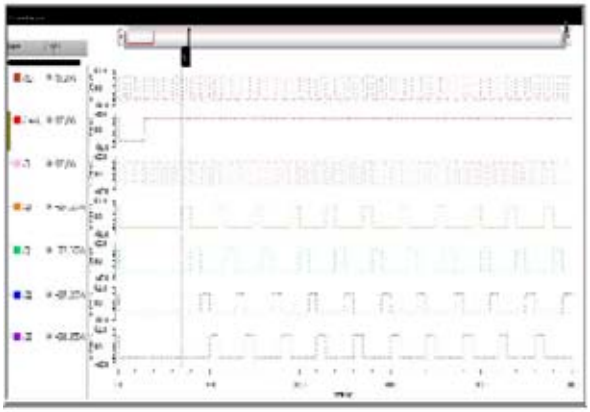


Fig-9(d): Transient response of SIPO 4-Bit Shift Register at 100KHz

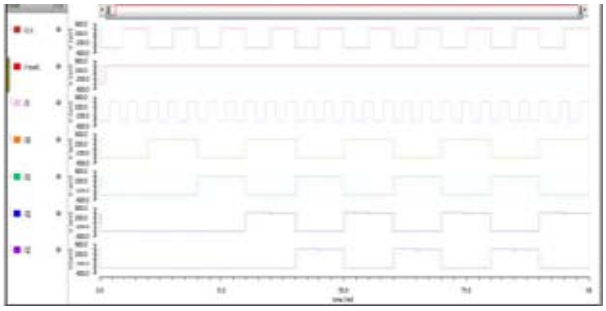


Fig-9(e): Transient response of SIPO4-Bit Shift Register at 1 MHz

Table.2 Transistor Count and Power estimation of the gates, Flip-flop, Counter and SIPO

| Circuit | No of Transistors | Power Consumption |
|---|---|---|
| Inverter | 2 | 66.8nW |
| AND | 10 | 73.7nW |
| XOR | 12 | 166.1nW |
| Flip-Flop | 26 | 819.7nW |
| Counter | 182 | 5.4uW |
| SIPO | 112 | 1.7uW |

## 5. CONCLUSION

In this paper, Master Slave negative edge triggered D Flip-Flop has been implemented, simulated and analyzed with 4 bit synchronous counter and SIPO as VLSI Apllications. The performance of these is assessed in terms of area, delay and power consumption. The main goal to optimize the power consumption is met satisfactorily using Cadence tool. The logic and characteristics of the master-slave D flip-flop, synchronous 4-bit up counter and SIPO are easily verified with the simulation results.

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