A 93DB GAIN AND LOW POWER OPERATIONAL TRANS CONDUCTANCE AMPLIFIER FOR DATA CONVERTERS

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Abstract

This paper presents a design to achieve Low power and High gain of an Operational Transcondcutance Amplifier simultaneously. The small-signal voltage gain, unity gain bandwidth of the conventional operational amplifier are improved in this proposed design. This proposed design uses a positive feedback technique, which is not usually preferred due its uncontrollability. The simulated results of the circuit show DC gain of 92.8 dB, unity gain bandwidth of 93.3MHz, phase margin of 71.6º, power supply of the proposed operational amplifier is 1.8 V (rail-to-rail ±700 mV), and power consumption is 266µWatts. This circuit specification has encountered the requirements of A/D Converter.

Keywords: Gain enhancement, positive feedback, differential amplifier, OTA(Operational Trans conductance Amplifier), small-signal Analysis

I. INTRODUCTION

In CMOS technology, the size for the gate channel length of complementary MOS transistors has been reduced from micrometres to submicron, which is known as short channel. One of the most problematic issues with integrated circuit (IC) is scaling down the gate channel length of the transistor devices for low-voltage, which poses a significant problem for Analog circuits. Scaling down devices to submicron or smaller levels means lowering the output resistance of the MOSFET; as a result, the small-signal gain of the differential pair is reduced.

To recover that small-signal gain, the output resistance is increased by arranging the MOSFET devices vertically, which this is known as cascode. Cascoding increases the differential gain significantly, but it also causes a reduction in the overhead voltage. Consequently, this reduces the output signal swings of the differential amplifiers.

This paper addresses the problems of gain decrease and unity gain bandwidth reduction by providing a positive feedback to the cross-coupled differential pair. The laterally configured amplifier circuit increases the small-signal voltage gain and also preserves the higher output voltage swings.

II.CMOS OPERATIONAL AMPLIFIER

The circuit in Fig. 1 shows the conventional CMOS operational amplifier(Op-amp) which provides a very high gain practically. The gain of the amplifier depends on the output resistance of PMOS and NMOS transistors and the transconductance of the circuit. The output resistance in turn depends on the channel length of the MOSFET's.

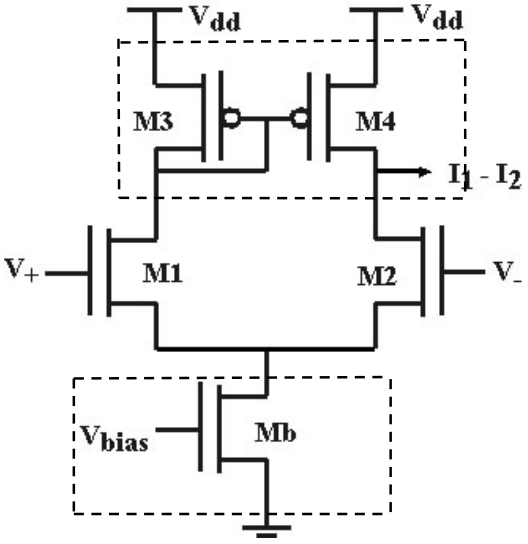

Figure 1 A Conventional Differential amplifier

The biasing circuit and current mirror are highlighted which make work the differential pair. The gain of the above Op-amp can be written as

$$A_V \square g_{m1,2} \square\square r_{on} \| r_{op} \square$$

□□□□□□□□□□

From [1], the relationship between output resistance and channel length (L) of a MOSFET device operating in saturation region is

$$r_o \propto \frac{L^2}{V_{DS,sat}^2} \qquad (2)$$

We can observe that when the length is reduced, the total output resistance of the circuit reduces and the gain follows.

III.POSITIVE FEEDBACK SYSTEM

Positive feedback technique is not preferred over the negative feedback technique due its unstable and uncontrollable nature. When designed properly, a positive feedback gives more yields when compared to negative feedback. Positive feedback enhances the gain of the circuit overcoming the degradation due to down-scaled technologies.

The positive feedback system is shown in Figure 2. The quantity A shows the feed forward amplifier network with a gain of A(s) where as B shows the positive feedback circuit with a gain of β(s).

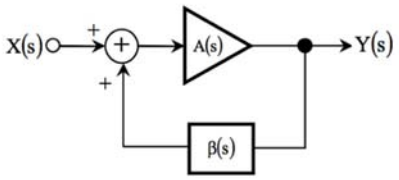

Figure 2 Positive feedback system

The closed loop transfer function is given as

$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1 - A(s) \cdot \beta(s)} \qquad (3)$$

The A(s).β(s) term is the "loop gain" of the system. The loop gain values must be greater than zero but less than one to ensure the feedback is positive.When the loop gainA(s).β(s) is equal to one, the denominator of (3) becomes zero; thus, the value of the transfer function Y(s)/X(s)becomes infinity. At this point, the pole is moved to the right-half plane, and the circuit becomes unstable. Also, designing too close to the origin of the axes is not recommended because of the instability concern.

IV.GAIN ENHANCEMENT CROSS COUPLED DIFFERENTIAL AMPLIFIER

The proposed circuit for gain enhancement using positive feedback concept is shown in Figure 3. The proposed circuit is fully-symmetric differential amplifier, which had MOS transistors cross-coupled in "horizontal" way rather than "vertical", and it generates a negative transconductance, -gm. This negative gm cancels out the already existing transconductance due to PMOS load transistors and NMOS differential pair. A very high DC gain is assured due to this.

To analyse the small-signal gain of the proposed circuit, let us focus on the differential pair with positive feedback circuit as shown in Figure 3.

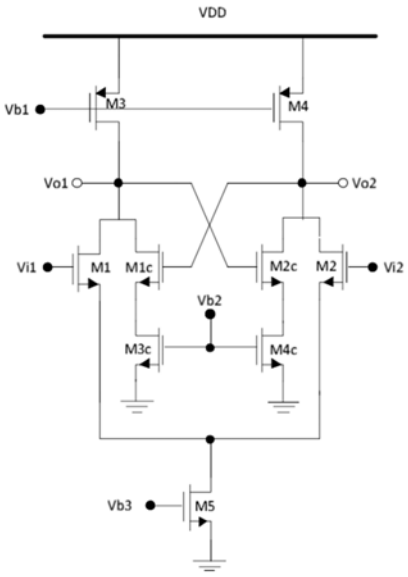

Figure 3 Cross-coupled diff amp with positive feedback

The total transconductance of the circuit is given by

$$G_m = \frac{I_o}{V_{g1c}} = \frac{I_o}{V_{o2}} \quad (4)$$

The output resistance of the given circuit can be calculated as

$$R = \frac{v_{o1}}{I_o} = \frac{v_{o1}}{G_m v_{o2}} = \frac{-v_{o2}}{G_m v_{o2}} = -\frac{1}{G_m} \quad (5)$$

The small-signal gain is given by

$$A_d = \frac{V_{o2} - V_{o1}}{V_{id}} = g_{m1} \cdot (r_{o1} \parallel r_{o3} \parallel R_o \parallel R) \quad (6)$$

V.COMMONSOURCE AS THE OUTPUT STAGE

To increase the output resistance of the entire system, common source amplifier is used as the output stage. This increase in outputs resistance increases the overall gain further and increases the sustainability of the circuit.

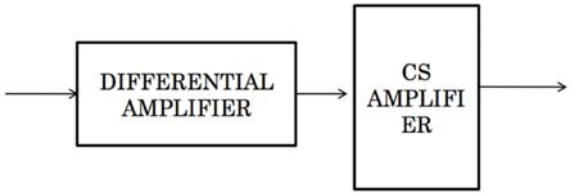

Figure 4 Blocked diagram of proposed design

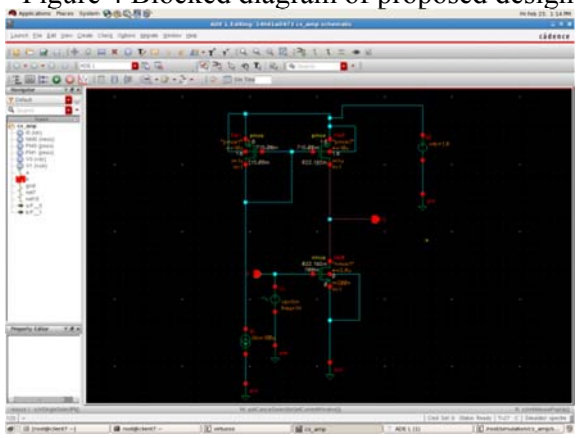

Figure 5 Common source Amplifier

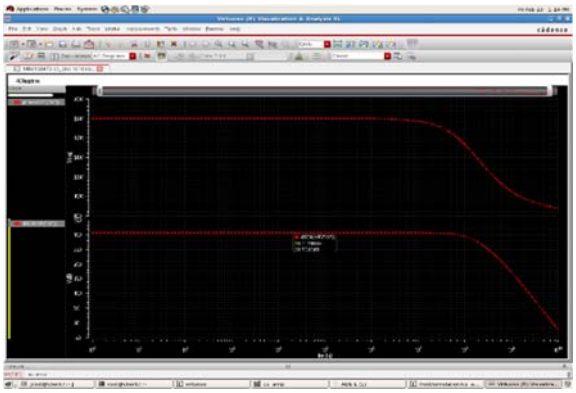

Figure 6 AC response of CS amplifier

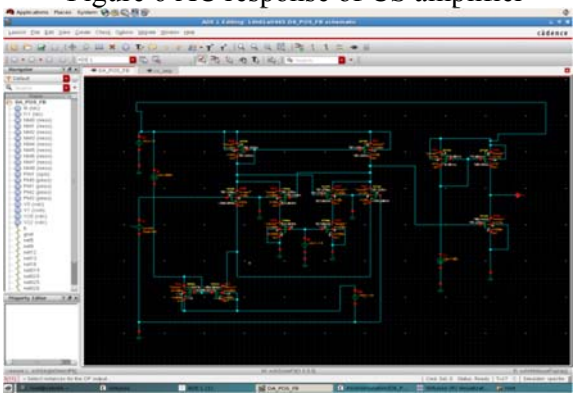

Figure 7 Schematic of Operational Transconductance Amplifier

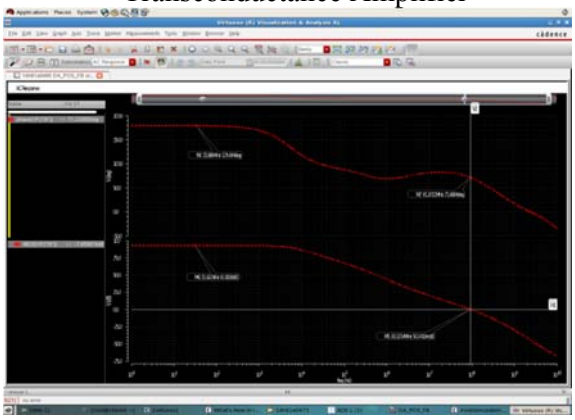

Figure 8 Gain and Phase plot of operational Transconductane Amplifier

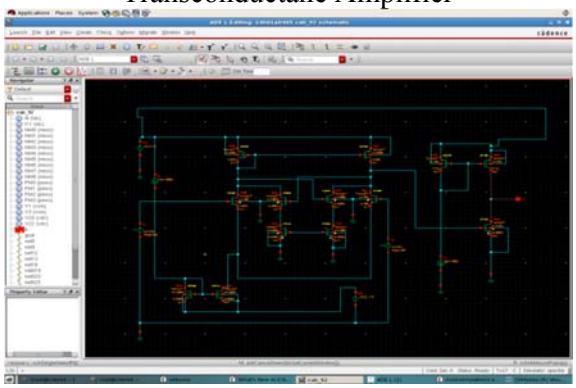

Figure 9 Schematic of the OTA design in common mode

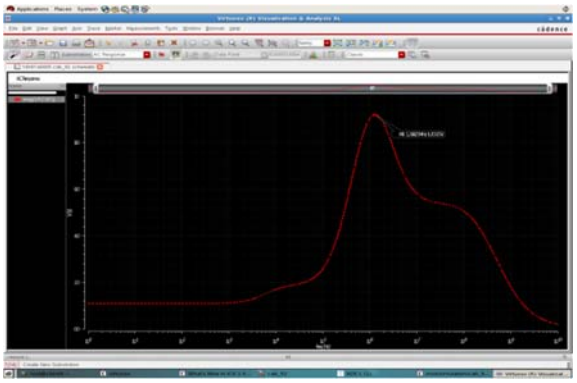

Figure10 AC response of the circuit in common mode

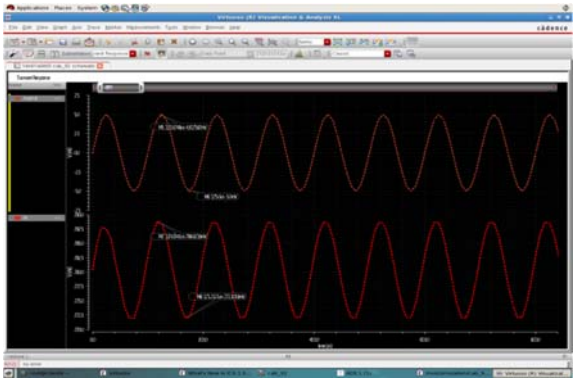

Figure11 Transient response of the circuit in common mode

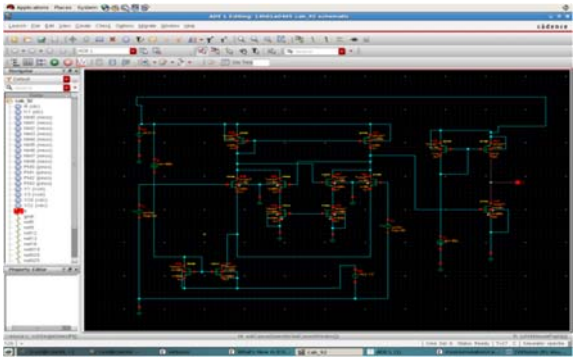

Figure 12 Schematic of the differential mode of the circuit

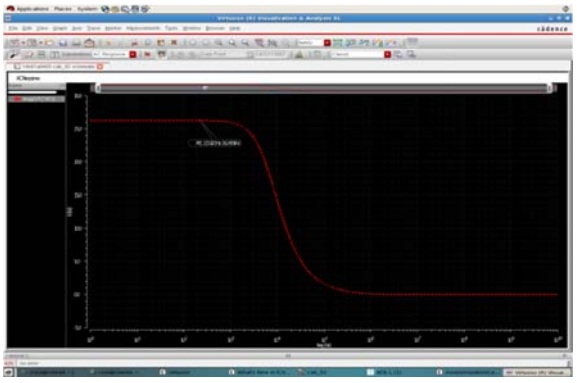

Figure 13 AC response in differential mode

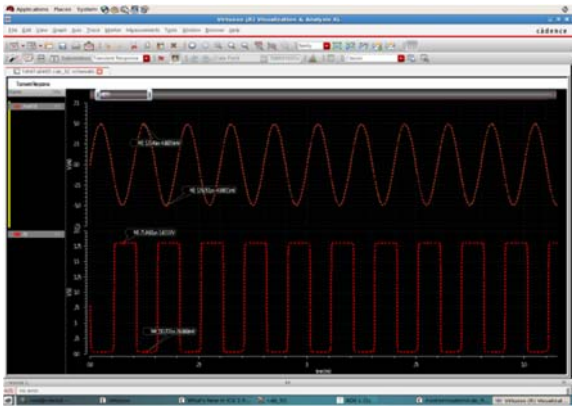

Figure 14 Transient response of the OTA circuit

Table 1:Comparison of desired specifications Vs Results

Parameters	Desired Specifications	Results
Power supply	±1.8v	±1.8v
Technology	180nm	180nm
Gain	>= 90dB	92.8dB
UGF	100MHz	93.3MHz
CMRR	>= 80dB	96.06dB
Power consumption	>100µWatts	266µWatts
Phase Margin	60º	71.6º

V.CONCLUSION

The Operational Transconductance Amplifier has been designed and its behavior is analyzed. Simulation results confirm that the proposed design procedure can be utilized to design op amp. The simulation is done with cadence virtuoso Software. The design is on 0.18µ CMOS Technology. The Op amp is designed with low power of 266µw and gain of 92.8dB and gain bandwidth of 93.3MHz. Design of accurate A/D converters and filters are challenging work for present applications. So this work can be extended further for communication applications with improved slew rate .For the mixed integrated circuit unity gain bandwidth can be further increased.

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