DESIGN OF LOW POWER COMPARATOR FOR DATA CONVERTERS

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Abstract

This paper describes the design of CMOS comparator for low power for data converters in 180nm technology. This paper illustrates the comparison between the proposed comparator and the existing comparator. This comparator incorporates differential amplifier cascaded with power amplifier. We are designing op-amp as comparator. Feedback loop is not required for op-amp as comparator. This comparator has a low power consumption which is achieved by using sleep transistor technique. This comparator requires only one clock cycle to trigger its transition from one phase to another. The comparator is designed and its functionality is verified in the cadence design environment. It is implemented in 180nm technology.

Amplifiers are essential building blocks of both analog and digital systems. An amplifier is an electronic device that increases the voltage, current, or power of a signal. The amount of amplification provided by an amplifier is measured by its gain: the ratio of output to input. We need to consider different parameters for designing op-amp like gain, offset voltage, input resolution, slew rate, propagation delay, speed. Sleep transistor method uses sleep transistors. Sleep Transistors are High threshold voltage transistors connected in series with low threshold voltage logic as shown below. When the main circuit consisting of Low threshold voltage devices are ON the sleep transistors are also ON resulting in normal operation of the circuit. When the circuit is in Standby mode even High threshold voltage transistors are OFF.

Since High threshold voltage devices appear in series with Low threshold voltage circuit the leakage current is determined by High threshold voltage devices and is very low. So the net static power dissipation is reduced

Keywords: Data converters, Low power, Sleep Transistor, Op-amp.

1. INTRODUCTION

Operational amplifiers (Op-Amps) are basic building blocks of a wide range of analogue and mixed signal systems. Basically, Op-Amps are voltage amplifiers being used for achieving high gain by applying differential inputs. The gain is typically between 60 to 70 decibels. This means that even very small voltage difference between the input terminals drives the output voltage to the supply voltage. In the case of using 180nm CMOS technology, this small voltage difference can be around tens of milli volts. As new generations of CMOS technology tend to have shorter transistor channel length and scaled down supply voltage, the design of Op-Amps stays a challenge for designers. An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations.

Operational Amplifiers was used describe amplifiers that performed various mathematical operations in the computing field. It was found that the application of negative feedback around a high gain DC amplifier would produce a circuit with a precise gain characteristic that depended only on the feedback used. By the proper selection of

feedback components, operational amplifier circuits could be used to add, subtract average, integrate, and differentiate. Operational Amplifiers was used describe amplifiers that performed various mathematical operations in the computing field.

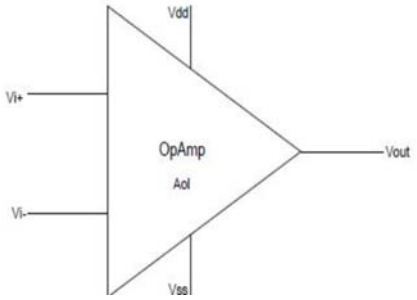


Figure 1: Op-Amp Symbol

It was found that the application of negative feedback around a high gain DC amplifier would produce a circuit with a precise gain characteristic that depended only on the feedback used. By the proper selection of feedback components, operational amplifier circuits could be used to add, subtract average, integrate, and differentiate. The designing of Op-Amps puts new challenges in low power applications with reduced channel length devices. Advancements which have appeared recently through new techniques and technologies, give us multiple alternatives in implementations. In two stage CMOS Op–Amps because of two dominant poles the phase margin could easily reach to less than the amount which is just enough for stable operation.

This serious problem should be taken care of by designers, otherwise there is a good possibility that the Op-amp output will oscillate and instead of an amplifier it will become an oscillator. In some applications the gain and/or the output swings provided by cascade op-amps are not adequate. In such cases, we resort to "two stage" Op-Amps, with the first stage providing a high gain and the second, large swing. In contrast to cascode Op-Amps, a two-stage configuration isolates the gain and swing requirements as well. To provide more gain and swing two-stage Op-Amps are used. About 5-15 dB gain is provided by the second stage which is not very high. Also the higher output swing is provided by the second stage which is crucial to some applications, especially in today's technologies with lower supply voltages. So, the second stage is a simple amplifier like a CS stage.

2. OP-AMP ARCHITECTURE

Amplification is an essential function in most analog (and many digital) circuit. The block diagram of two stage Op-Amp is

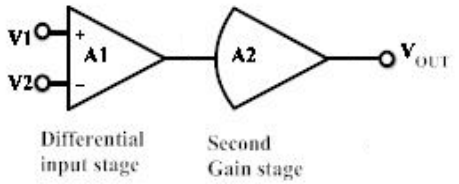


Figure 2**:** Op-Amp architecture

It consists of two stages in which first is differential stage and second is the gain stage. Output buffer is also used. In CMOS Op-Amp compensation network is used to which a feedback network is applied around the amplifier in virtually all Op-Amp applications. It consists of differential amplifier and CS amplifier. It consists of 10 transistors. The n-channel transistors *M*1 and *M*2 form the input differential pair, and the p-channel transistors *M*3 and *M*4 form the active load. The diff-amp input stage is biased by the current mirror *M*9 and *M*10, in which the reference current is supplied by I_{Bias} which is 30uA. The second stage, which is also the output stage, consists of the common-source connected transistors *M6* and *M*7. An internal compensation capacitor of 1Pf is included to provide stability.

3. OP-AMP DESIGN

This design procedure assumes that the gain at dc (*Av*), unity gain bandwidth (*GB*), input common mode range (*Vin*(min) and *Vin*(max)), load capacitance (*CL*), slew rate (*SR*), settling time (*Ts*), output voltage swing (*Vout*(max) and *Vout*(min)), and power dissipation (*Pdiss*) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for *Cc*, i.e. for a 60° phase margin we use the following relationship.

This assumes that z □□□□10GB.

CC > (2.2/10) CL

2. Determine the minimum value for the "tail current" ($I5$) from

$I5$ □□SR .Cc

3. Design for $S3$ from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$$

4. Verify that the pole of M3 due to $Cgs3$ and $Cgs4$ (□□0.67W3L3Cox) will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

5. Design for $S1$ ($S2$) to achieve the desired GB.

$$g_{m1} = GB \cdot C_c \rightarrow S_2 = \frac{g_{m1}^2}{K'_1 I_5}$$

6. Design for $S5$ from the minimum input voltage. First calculate $VDS5$(sat) then find $S5$.

$$V_{DS5}(\text{sat}) = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100\ \text{mV}$$

$$S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

7. Find $S6$ by letting the second pole ($p2$) be equal to 2.2 times GB and assuming that $VSG4 = VSG6$.

$$g_{m6} = 2.2g_{m2}(C_L/C_c)$$

$$\frac{g_{m6}}{g_{m4}} = \frac{\sqrt{2K_P'S_6I_6}}{\sqrt{2K_P'S_4I_4}} = \sqrt{\frac{S_6I_6}{S_4I_4}} = \frac{S_6}{S_4}$$

$$S_6 = \frac{g_{m6}}{g_{m4}}S_4$$

8. Calculate $I6$ from

$$I_6 = \frac{g_{m6}^2}{2K'_6S_6}$$

Check to make sure that $S6$ satisfies the $Vout$(max) requirement and adjust as necessary.

9. Design $S7$ to achieve the desired current ratios between $I5$ and $I6$.

$S7$ □□($I6$/$I5$)$S5$

(Check the minimum output voltage requirements)

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(l_2 + l_4)I_6(l_6 + l_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, $I5$ and $I6$, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents $I5$ and $I6$. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

Table 1: achieved result summary of compartor

PARAMETERS	DESIRED VALUES
Gain	62dB
Bandwidth	70MHz
Phase margin	175degree
CMRR	75dB
Slew rate	40v/us
Power dissipation	45uw

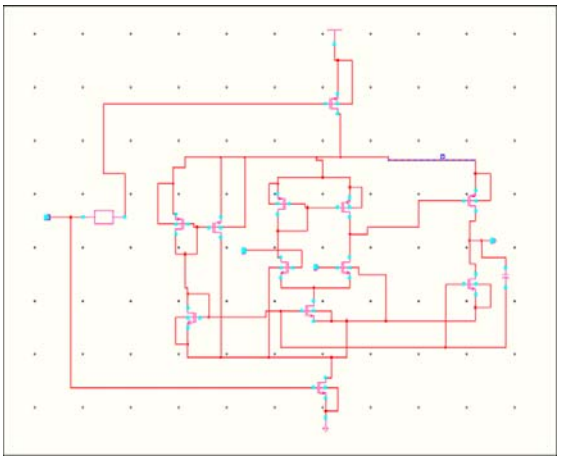


Figure 3: Schematic with low power technique

4. LOW POWER TECHNIQUE

Sleep transistor technique:

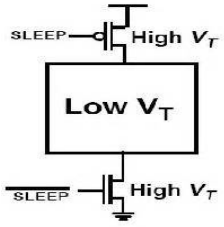
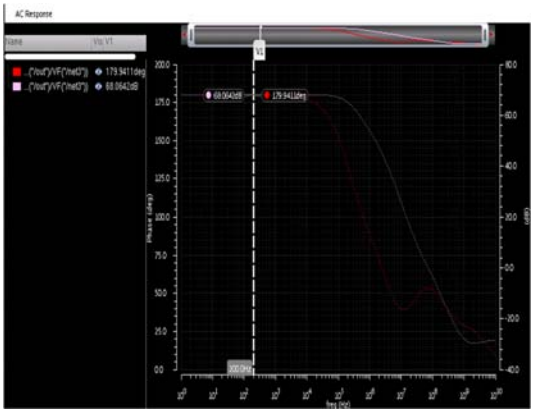


Figure 4: Sleep transistor method

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors as shown in figure 4. This technique is MTCMOS, which adds high-Vth sleep transistors between pull-up networks and Vdd and pull-down networks and gnd while for fast switching speeds, low-Vth transistors are used in logic circuits. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

5. AC ANALYSIS OF OP-AMP



6. CMOS OP-AMP AS COMPARATOR

The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison. The comparator is basically a 1-bit analog-to-digital converter.

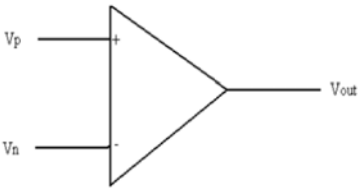


Figure 5: Comparator Symbol

The output of comparator is high (VDD) when the difference between the non-inverting and inverting input is positive, and low (VSS) when this difference is negative.

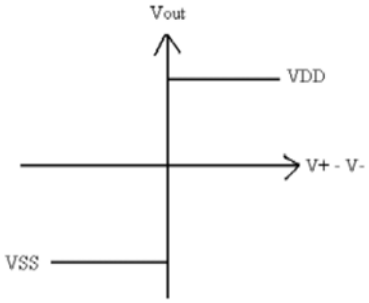


Figure 6: Output of comparator

The comparator is a critical part of almost all kind of analog-to-digital (ADC) converters Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of the target application. The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range. Ideally the gain of the comparator is infinite and the offset voltage is zero volts. But practically the gain of the comparator is finite.

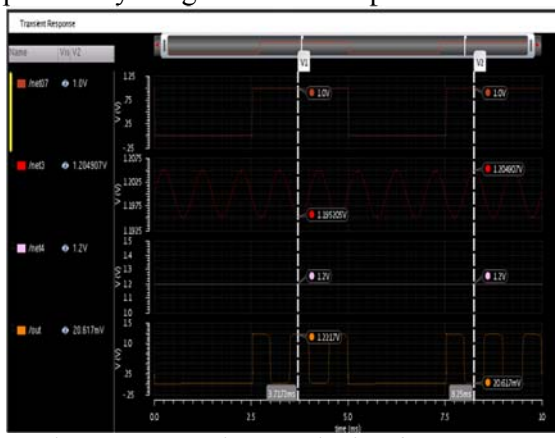


Figure 7: Transient analysis of Comparator

7. CONCLUSION

The amplifier presented in this paper operates in saturation mode and regulates its bias current. When a signal is applied the current in the amplifier increases so that these amplifiers have very high driving current. The op-amp has low power as well as low voltage. Its slew rate is higher than reported. Low power low voltage amplifier is designed at 180nm technology whose gain is 70dB and phase margin 179 degrees. The unity gain bandwidth is obtained 70MHz. Power dissipation is reduced from 163uW to 44uW by using sleep transistor technique.

8. REFERENCES

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