A SURVEY ON LOW-POWER AND AREA-EFFICIENT MODIFIED BOOTH MULTIPLIER

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Abstract
Reversible logic plays an important role in low power CMOS technology, nanotechnology and optical computing. Reversible logic is used to carry computation in quantum technology. Reversible gate as well as reversible circuits including universal logic gates are constructed to design a multiplier. The various arithmetic operations such as computer arithmetic unit are performed through multipliers. Reversible logic is used in many applications due to low power dissipation. Instead of booth recoding multiplier, signed multiplication is performed through k-algorithm where hardware complexity is reduced. The design parameters are optimised in this design.
Key words: K-Algorithm; Booth's recoding; multiplier architecture; reversible circuits.

1. Introduction

Reversible logic is mainly used because of its ability to reduce power dissipation which is very important in low power VLSI design. Reversible logic finds its applications in various fields such as low power CMOS and optical information processing, DNA computing and nanotechnology. The use of irreversible circuits leads to loss of information which inturn dissipates more power. More power dissipation leads to heat generation on top of the chip which cause damage to the chip. Reversible circuits have equal number of inputs and outputs. In reversible circuits there is one-to-one mapping which means from output , input can be recovered. Energy dissipation will be zero when there is no loss of information. Fan-outs and loops are not allowed in reversible logic circuits.

Related Work

In 1961, Rolf Landauer[1] said that heat dissipation occurs when there is a loss of information. Loss of each bit of information leads to KTln2 joules of heat dissipation, where K is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. Heat dissipation is zero for reversible circuits at ideal conditions. The heat dissipation leads to low performance and reduction of lifetime of components.

Bennette[2] showed that the heat lost by reversible circuits is zero at ideal conditions. Reversible circuits cause less loss of information. Moore's law states that "the number of transistor on a chip increases every 12 to 18 months".

Himanshu thapliyal and M.B Srinivas[3] Proposed TSG gate which works as a single reversible full adder. TSG gate used here is a 4*4 reversible gate. 4*4 architecture is designed using existing reversible multiplier. TSG gate used in proposed multiplier architecture is better and optimised compared to other architecture such as number of reversible gates and garbage outputs.

H R Bhagyalakshmi and M K Venkatesha[4] proposed BVPPG gate which is a 5*5 reversible gate which has been designed to generate partial products which performs multiplication and operand bits duplication is obtained. BVPP gate is used to design the 4 bit architecture.The proposed multiplier is designed using Toffoli

gate which most flexible and universal reversible gate. The proposed multiplier architecture reduces the overall cost of the circuit. Toffoli gates and constant inputs effects the quantum cost.

H.R.Bhagyalakshmi et.al.[5] Improved multiplier design is constructed using reversible logic gates. The design requires DPG gate and BVF gate which is a 4*4 reversible gate. Reducing the number of reversible circuits lead to the low quantum cost. Multipliers are useful in construction of arithmetic units of quantum computers.

Maryam Ehsanpour et.al.[6] MFA(modified full adder) is used to construct a novel reversible 4-bit binary multiplier. MFA adder alone works as a reversible full adder. The hardware complexity is less and requirement of garbage outputs and constant input are low which leads to the increased speed of the multiplier circuit. N*N bit multiplication can be designed using 4-bit binary multiplier.

Rakshith TR. Et.al.[7] The number of multiplications performed decides the performance of microcontrollers and digital signal processors. Vedic multiplier is used to perform complex multiplication. Power dissipation is less when Vedic multiplier is used along with reversible logic. In embedded system, the power dissipation is another drawback which needs to be looked after. “Urdhva Tiryakbhayam” is used in applications such as Fast Fourier Transform, imaging, software defined radios and wireless communications.

Rakshith Saligram et.al.[8] Speed and power is effective in Urdhva Tiryakbhayam Vedic multiplier. The design is evaluated using Total Reversible Logic Implementation Cost (TRLIC). The reversible circuits still need to be optimised.

Sumit Vaidya et.al.[9] “Urdhva Tiryakbhyam” is used in multiplication which improves the speed, area and other parameters. “Nikhilam Sutra” uses more than one equation to reduce the number of repetition which results in increase in speed. More delay is obtained in this multiplier design.

Michael Nachtigal et.al.[10] Single precision floating point multiplier using operand decomposition method is designed. 8*8 bit Wallace tree multiplier is designed which reduces quantum cost, delay and garbage outputs. 24*24 bit multiplier is constructed using 8*8 bit reversible Wallace tree multiplier.

M.Jenath, V.Nagarajan[11] The reversible single precision floating point multiplier(RSPFPM) is designed. Peres gate is used to construct the multiplier whose quantum cost is low. Based on operand decomposition method, operand bits is divided into 3 parts which has 8 bits in each partition. Using nine 8*8 bit multipliers,24*24 bit reversed multiplier is performed addition is done at the output to reduce the quantum cost and garbage outputs. The drawback of this architecture is that garbage outputs are more.

H. P. Sinha, Nidhi Syal[12] a novel 4x4 bit reversible fault tolerant multiplier circuit is designed which is used to multiply two 4-bit numbers. The proposed design has high speed and complexity of hardware is less. The partial product is generated in parallel using Fredkin gates and the addition is performed using reversible parallel adder where IG gates are used. Drawback is more power dissipation.

Md. Belayet Ali et.al.[13] The Modified HNG (MHNG) is a 4*4 reversible gate which functions as a reversible full adder. The reversible fault-tolerant multiplier is constructed using pere gate and MHNG gate. The 4*4 multiplier circuits offers low hardware complexity and number of reversible logic gates, garbage output are reduced.

Majid Haghparast et.al.[14] The 4*4 bit reversible multiplier circuit is proposed which is faster and low hardware complexity. “HNG” gate is used which is 4*4 reversible gate is capable of multiplying two 4-bit numbers for the proposed reversible multiplier. More complex systems can be constructed using 4*4 reversible multiplier design. Optical logic implementations are not yet available.

Sukhmeet Kaur et.al.[15] implemented radix-4 Modified Booth Multiplier and this

implementation is compared with Radix-2 Booth Multiplier. The method of implementing the Parallel MAC with the smallest possible delay is investigated. MAC is implemented By combining multiplication with accumulation and carry-look-ahead adder (CLA) is devised. The speed is increased and less circuit complexity. Parallel MAC is used DSP and video applications.

Kartikeya Bhardwaj et.al.[16] Signed multiplication is performed using k-algorithm which is an improved version of Booth's recoding multiplier. The implementation of k-algorithm is designed using an efficient multiplier architecture. Fault-tolerance and non fault-tolerance 4-bit reversible multipliers is designed. The reduction in quantum cost and design metrics is observed.

Comparison of Different Papers

Reversible multipliers	Gate count	Number of garbage output	Quantum cost	Constant input
Existing circuit[3]	1	2	-	-
Existing circuit[4]	20	28	144	28
Existing circuit[5]	40	52	152	52
Existing circuit[6]	-	36	-	20
Existing circuit[7]	37	62	162	29
Existing circuit[8]	33	43	164	33
Existing circuit [10]	-	4	12	-
Existing circuit [11]	-	179	171	-
Existing circuit [12]	44	56	128	56
Existing circuit [13]	28	22		28
Existing circuit [14]	28	52		28
Existing circuit [16]	-	34	126	30

Conclusion

Multipliers are widely used digital components. Multiplication speed must be high to speed up the processor. In order to increase speed of the multiplication the basic multipliers are replaced with fault-tolerant reversible multiplier which is more efficient and less complex and it consumes less power. In recent days as the technology increases, the critical issue is the power dissipation so the reversible logic area reduce the power dissipation which is main constraint of low power dissipation. K-Algorithm is useful in optimizing the reversible as well as conventional multiplier designs with equal number of merits.

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