DESIGN AND IMPLEMENTATION HIGH PERFORMANCE 5T SRAM - RESULT

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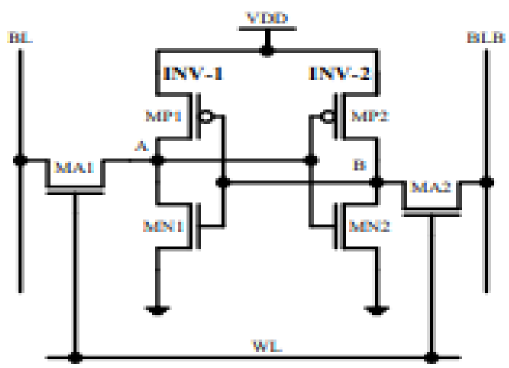
Abstract
Semiconductor memories are most important subsystem of modern digital systems. In new area the scaling of silicon technology has been ongoing, due to scaling large memory can be fabricated on a single chip as results memories are capable to store and retrieve large amount of information at high speed. SRAM is a memory component and is used in various VLSI chips due to its unique capability to retain data. This memory cell has become a subject of research to meet the demands for future communication systems. In this paper 5T and 6T SRAM cell is designed by using Tanner EDA tool in CMOS technology. Its performance characteristics such as power dissipation, Transistor count are analyzed in terms of 5t AND 6T.
Keywords: SRAM, 5T, 6T.

1. Introduction

Static random access memory (SRAM) is a static memory cell which is widely used in various electronic systems. It is faster and consumes less power as compared to other memory cells [1-2]. It does not require refreshing periodically. Because of this, SRAM is the most popular memory cell among VLSI designers. Hence continuous evolution is going on for better performance of SRAM cells. Due to this, different types of SRAM cells are available in the literature like 6T SRAM cell, 7T SRAM cell, 8T SRAM cell, 9T SRAM cell etc. Most common SRAM cells used in digital system is the 6T SRAM cell. This cell can store 1-bit of data. The bit remains in the cell as long as power is supplied. In this paper, design and performance analysis of a 6T SRAM cell is discussed. Recently, Static random access memory (SRAM) is used in a large variety of consumer electronics, such as computers and cellular phones. SRAM requires no refreshing and will maintain its information as long as it has sufficient power supplied. This is due to the fact that the SRAM cell includes flip-flop circuitry internally that does not require refreshing. However, it is apparent that SRAM suffers from the disadvantage of relying on too many transistors. Accordingly, there is an important need to have an SRAM cell that requires fewer than six transistors. An SRAM cell has three modes of operation, namely read, write and standby [1]. The data stored in the cells may be corrupted when the cells are read. This problem arises from the fact that a higher voltage on the bit line is coupled to a lower voltage in the cell, causing the bit line voltage to drop and the cell voltage to rise. Further, a concern associated with the write operation is that it is relatively difficult to write a logic ‘1’ to the cell if the cell currently stores a logic ‘0’. Accordingly, the SRAM cell should provide less likely to be corrupted when the cell is read and more reliable when the cell is written [2]. As integrated circuits become smaller and denser and as power consumption specifications for battery powered integrated circuits decrease, along with power supply voltages, the present SRAM cell designs are increasingly inefficient in both silicon area used and power consumed. Memories take up 80% of the die area in high performance processors [3]. Therefore, there is a crucial need for a low leakage and highly robust SRAM design. Leakage current from a memory cell can cause unnecessary power consumption, especially during a standby mode. Recent research has shown that the leakage current will become even greater than the dynamic current in the overall power consumption [4]. Typically, there are three major sources of leakage in a MOS transistor, namely sub threshold leakage, gate leakage, and reverse bias junction leakage [5]. Amongst them, Gate-Induced drain leakage (GIDL) is an unwanted short-channel effect that occurs at higher drain biases in an overdriven off state of a MOS transistor. The GIDL is the result of a deep depletion region that forms in the drain at high drain-to-gate biases. However, Drain induced barrier lowering (DIBL) is a short-channel effect in MOS transistors referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. With scaling down of the MOS transistor, each of the leakage sources may increase accordingly, thus resulting in the increase of the total leakage current. As CMOS technology scales down to 90 nm and below, the power consumption caused by leakage currents is becoming a significant part of the global power consumption [6]. Therefore, it would clearly be desirable to provide a design for an SRAM cell that has less leakage current than traditional designs when the cell in standby.

2. Existing 6T and 5T SRAM Cell Topologies:

The standard 6T SRAM is built up of two cross-coupled inverters (INV-1 and INV-2) and two access transistors (MA1 and MA2), connecting the cell to the bit lines (BL and BLB), as shown in Fig. 1 [7]. The pair of cross coupled inverters is formed by a pair of load transistors (MP1 and MP2) and a pair of driver transistors (MN1 and MN2) that are stronger than the access transistors. More specifically, the cross-coupled inverters of the memory cell have two storage nodes A and B functioning to store either logic ‘1’ or logic ‘0’. The gates of access transistors are connected to a word line WL, and a rising transition on the word line to assert the access transistors during a read or a write operation. At the end of the read and write operations, the word line WL is de-asserted to allow the cross-coupled inverters to function normally and hold the logic state of the storage nodes. A concern associated with the read operation is that because of the back-to-back connection of cross-coupled inverters, a regenerative action develops and node A is pulled high resulting in the destruction of contents in the bit cell. Especially, when a logic ‘0’ stored initially, the voltage rise in the cell may corrupt the data stored. Therefore, it is desirable to keep the voltage at the storage node which has a logic ‘0’ stored from rising above the trip-voltage of the inverter. To provide a non-destructive read operation, the cell ratio (CR) was conventionally varied from 1 to 2.5 [2], where the W/L ratio of the driver transistor to the access transistor is referred to as the cell ratio. Similarly, for a successful write operation, both access transistors must be stronger than the load transistors. The ratio of the load transistor to the access transistor is referred to as the pull-up ratio (PR). To improve the readability of an SRAM cell, cell ratio can be increased, while a lower pull-up ratio is desirable to improve the cell write ability. Figure 2 is a circuit diagram of a traditional 5T SRAM cell [8]. As shown in Fig. 2, the access transistor MA2 and bit line BLB in Fig. 1 have been removed to provide a five transistor configuration. The removal of such access transistor allows for an area savings up to 20-30% compared to the standard 6T SRAM cell, while its power consumption is substantially reduced by one half [9]. Although the traditional 5T SRAM cells offer such significant reductions in power consumption, a serious drawback is presented in that it is difficult to write ‘1’ to the cells. In detail, when the bit line BL is set high and the word line WL is asserted, the transistors MA1 and MN1 fight one another. To guarantee a correct write operation will occur, it is important to note that the storage node A must be pulled up (or down) above (or below) the tripvoltage of INV-2 within the word line WL is logic high, otherwise a write failure will occur. In more detail, writing a logic ‘1’ to a cell when initially a logic ‘0’ is stored, the low storage node A of the cell must be pulled up by the pre-charged bit line BL above the trip-voltage of INV-2. Undoubtedly, to properly write the wanted bit in the cell, it may be necessary that the access transistor should be very conductive to force the cross-coupled inverters to change its equilibrium condition. However, the access transistor should have a reduced conductivity for good stability in reading and standby operations. These two requirements impose contradicting requirements on cell transistor sizing.



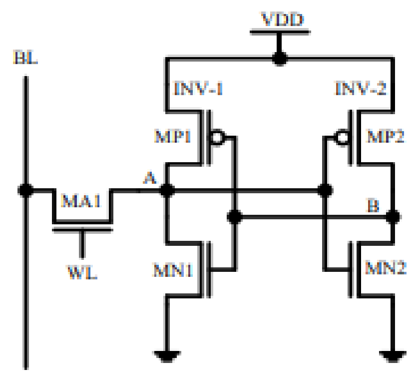


Fig. 1. Circuit diagram of standard 6T SRAM cell. Fig. 2 Circuit diagram of traditional 5T SRAM cell.

As mentioned above, it is difficult to write '1' to a memory cell that is storing a '0'. In order to resolve the write '1' issue of the traditional 5T SRAM cells, several techniques have been developed. Some of these techniques rely on boosted word line voltage [10-12], reducing the supply voltage VDD [8-9], [13-14], sizing cell transistors [15-17], reduced bit line voltage [18-19], and raising the source voltage VSS [20-22]. However, each of these techniques may cause a reduction in the drive current of the transistors and in the operating speed of the cell, or has increased memory cell area and a degradation in the manufacturing accuracy, or requires generation of a voltage above the operating voltage, or requires a more complicated circuit design and more complicated device process. Hence, there is a need for an effective technique to improve the writeability of 5T SRAM cells which suffer from inability to write '1'. As

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II. Design of A 6T SRAM CELL

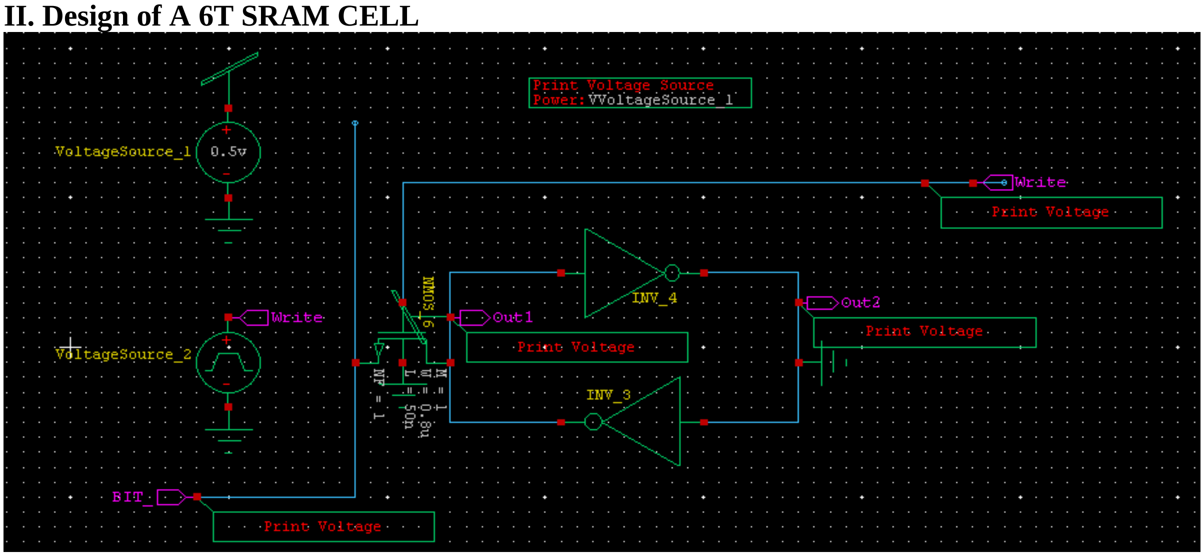

Fig. 3.5T Ram Read operation

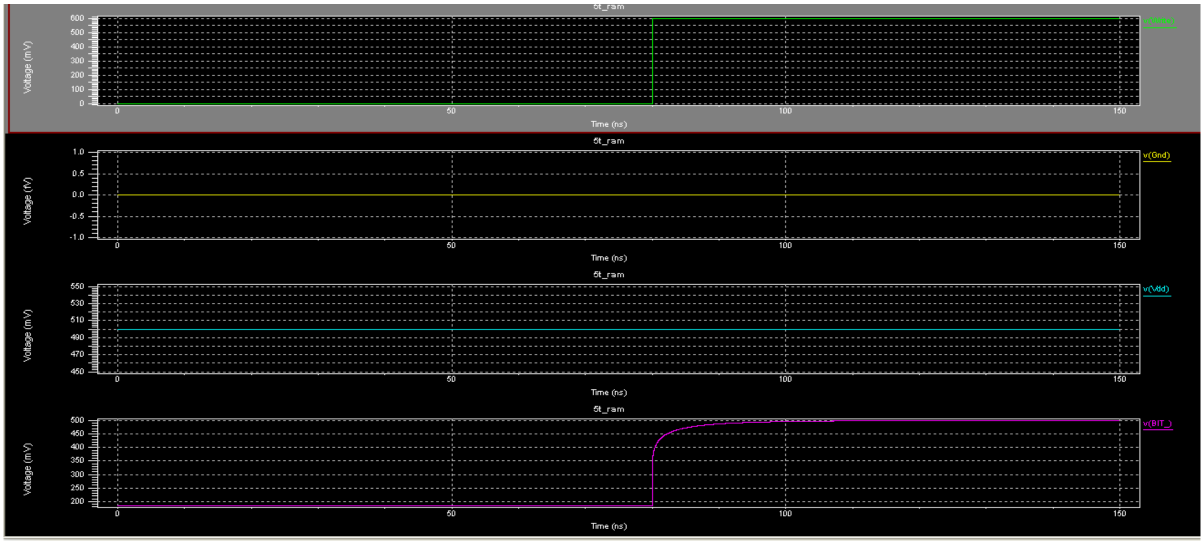

Fig.4.5T Ram Read operation waveform

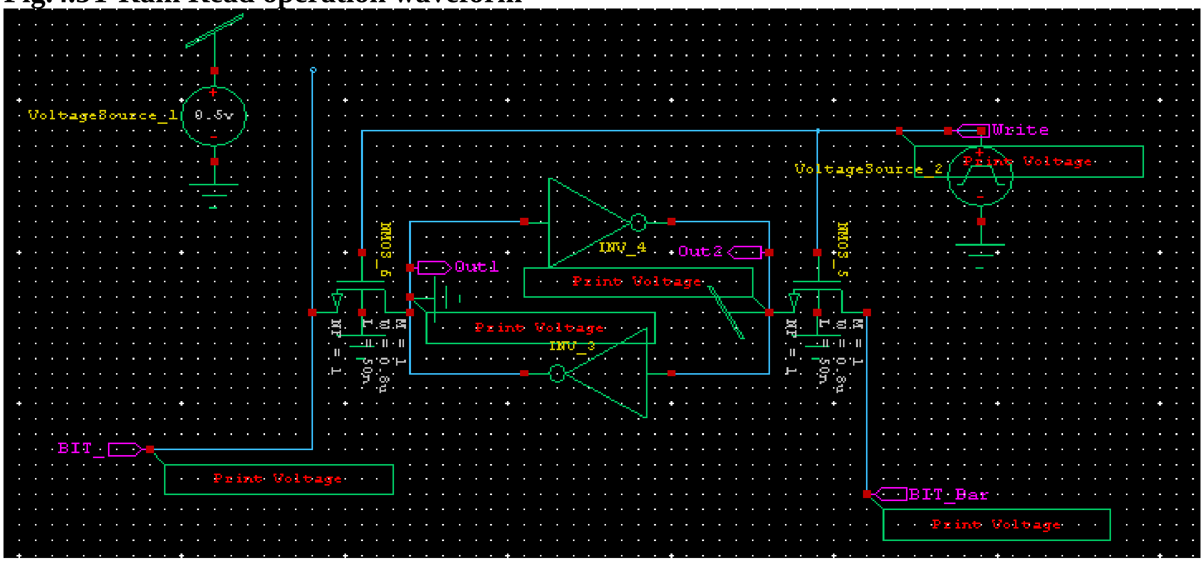

Fig .5.6T RAM Read

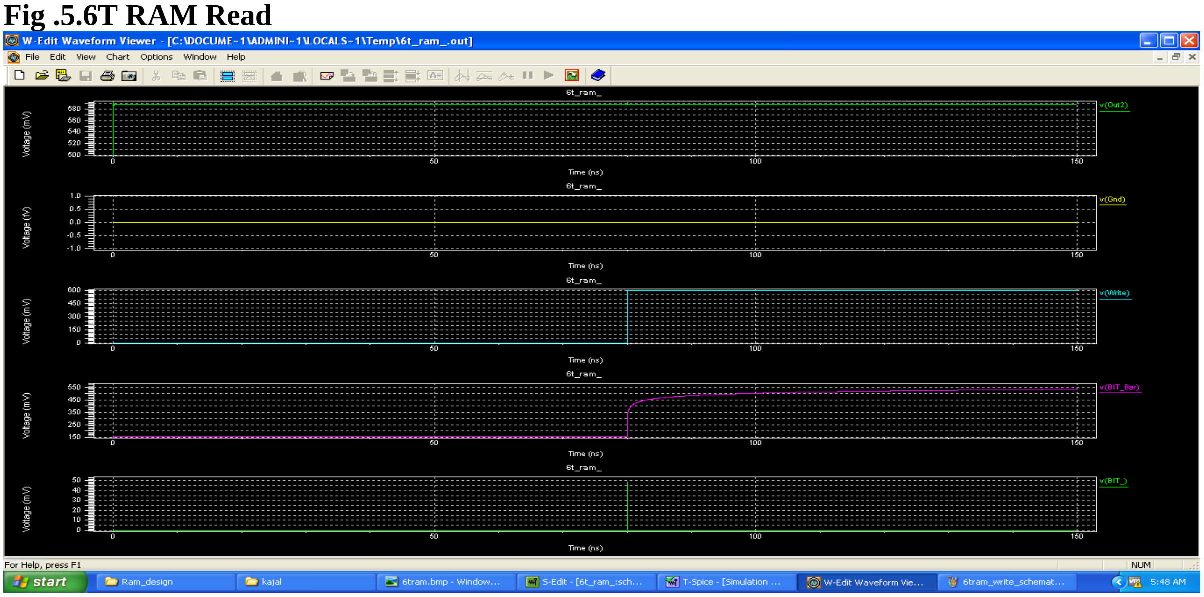

Fig.6. 6T RAM Read operation Waveform

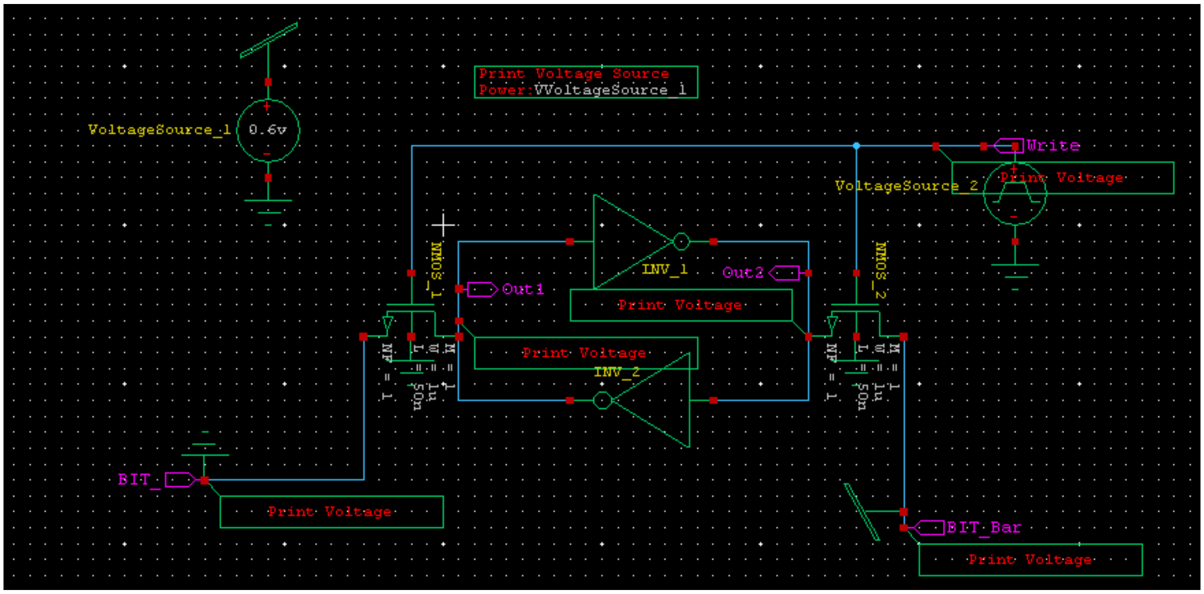

Fig 7.6T RAM Schematic during write mode

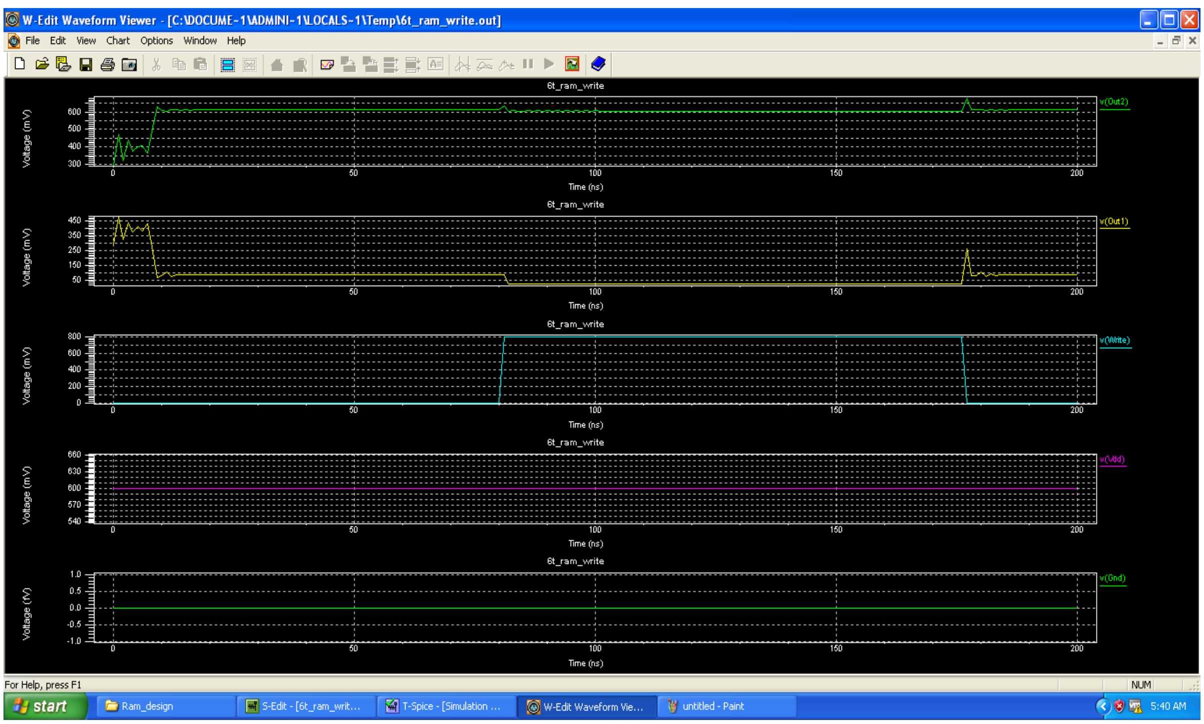

Fig.8. 6T RAM write operation Waveform

Result analysis:

Sr. No.	Parameters	5T	6T
1	Average Power	2.5 x10^-6 W	1.8x10^-6 W
2	Transistor count	5	6

Conclusion:

Thus the study of 5T and 6T SRAM which perform read and write operation .During the read operation bit line wok as output. Whereas during write operation bitline work as input. The total number of transistor required is less in 5T which reduces size and average power consumption is 2.5u watt where as for the 6T RAM the average power is 1.8 watt.

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