TRAFFIC LIGHT CONTROL SYSTEM USING VERILOG DESIGNING.

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ABSTRACT

Verilog designing is hardware descriptive language, the name itself suggest that it deals with the hardware designing and simulation. Basically, it becomes very difficult to mount the various electronic component on breadboard or PCB circuit. It also takes too much time for the simulation and sometimes many errors occur because of improper connection of components onto the circuit. And thus, to overcome this factor hardware descriptive language comes into conclusion. we can code the process using Verilog and we can mount it on a circuit or just upload it to the circuit accordingly so that particular circuit will work as according to the code we have written. HDL language is often used for sequential circuits like shift register, combinational logic circuit like adder, subtractor etc. basically it describes the digital systems like microprocessor or a memory. Whatever design that is describe in HDL are independent, it has its unique state of work, very much easy to simulate, designing and debugging, and very useful than schematics, especially for large circuits thus, to overcome difficulties or problems to design the circuits manually with breadboard and PCB, use of Verilog designing in this complex world is increasing a way better.

Keywords: HDL, Verilog, PCB, Combinational logic circuit, microprocessor, simulation, register.

I.INTRODUCTION

Traffic light signal controlling is most important and essential thing for any country to protect the people from heavy load of traffic. before this kind of invention there was much difficult for traffic police to handle the heavy traffic (particular direction given manually). thus, traffic signal controlling technology made much easier to handle the heavy loads of traffic. Safe movement of vehicles without any type of collision, accidents. Apart from the traffic it is very necessary for the people to cross the roads at particular time interval. And this is only possible by controlling the traffic by giving some kind of signal. Analysing the traffic, estimating the delays to the areas is crucial part.

Population can be predicted using GPS trekking and thus we can easily estimate the amount of time to be taken for delay. a perfect aligning of cars, bikes, cycles, trucks with orderly flow by giving right of way, this makes the processes very systematic and even in the presence of heavy traffic accident rate goes down which is one of the biggest advantage. Timing and the delays of particular signal plays a vital role because it is very necessary for us to keep information about the amount of traffic which present in the local area. This gives us an idea about timing and delay requirement of every signal in the local area. As we now the timing depends on traffic volume and its not necessary for us to have same traffic volume at each day so for that we can estimate average volume of traffic around the local area. Average can be made with consideration of 20 days for example we will analyse the traffic of 20 days then we will take an average of it and estimate delays and timings of it. It is very necessary factor for us to have adaptive mechanism. Apart from that we can estimate the traffic volume using GPS, which can give you volume prediction every day. For this we no need to take an average of particular days. GPS give us more correct prediction of volume of traffic than calculating an average of traffic of particular days. Thus, coordinating

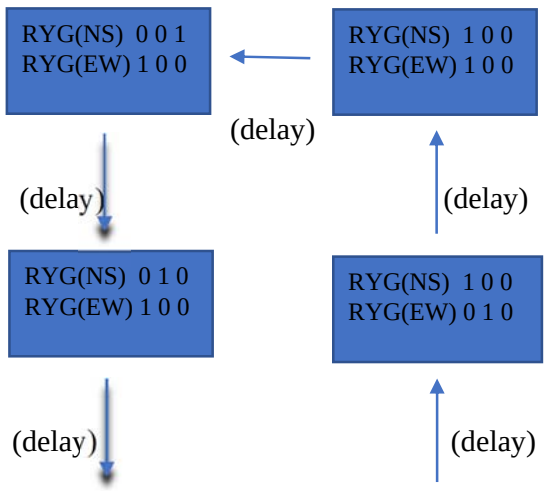
signal timing minimizes stating and stopping of vehicles in the traffic to avoid the traffic jam.

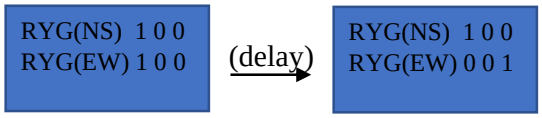
II. METHODLOGY

Verilog is hardware descriptive language (HDL) which is generally used to model electronic system. that is, we can design a circuit and the function of circuit can be control by Verilog coding. Thus, design and verification can be done using Verilog designing. Similarly, traffic light signal controlling can be done using Verilog (hardware descriptive language). so now we have design the traffic light signal system with Verilog using sequence detector method. We have considered area where there are two highways one from north-south and other from east-west. And heavy load of traffic present over these highways where we have to control these highways using traffic signal. If we want to keep flow of traffic at north-south end for particular time interval and simultaneously we allowed the traffic flow at east-west end.

STAGES	SIGNAL BIT
1	001100 (Binary)
2	010100 (Binary)
3	100100 (Binary)
4	100001 (Binary)
5	100010 (Binary)
6	100100 (Binary)

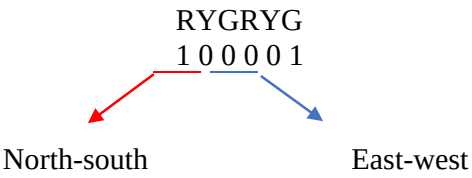
Flow chart of traffic light controller systems





Above blocks are the various stages of signalling mode. At each block has different pattern. RYG denotes (RED YELLOW GREEN). (NS) and (EW) denotes (NORTH-SOUTH END) and (EAST-WEST END). At each stage it has six-bit sequence as it can be observed through blocks. for example, at any stage if we have a sequence 100001 that means

1).



So, at very 1st stage we have kept the traffic flow at north south end thus, bit signal for north-south will be 001(RYG) and simultaneously east-west end will have bit signal 100(RYG)

Transition from red light to green light requires delay more. That means amount of time for the delay is more. Similarly transition from green light to yellow light requires moderate delay.

State	North-South	East-West	Delay
1	RED	GREEN	Long delay
2	RED	YELLOW	Small delay
3	RED	RED	Small delay
4	GREEN	RED	Long delay
5	YELLOW	RED	Small delay
6	RED	RED	Small delay
1	RED	GREEN	Long delay

Transition of yellow light to red light requires very small delay as compared to other delays.

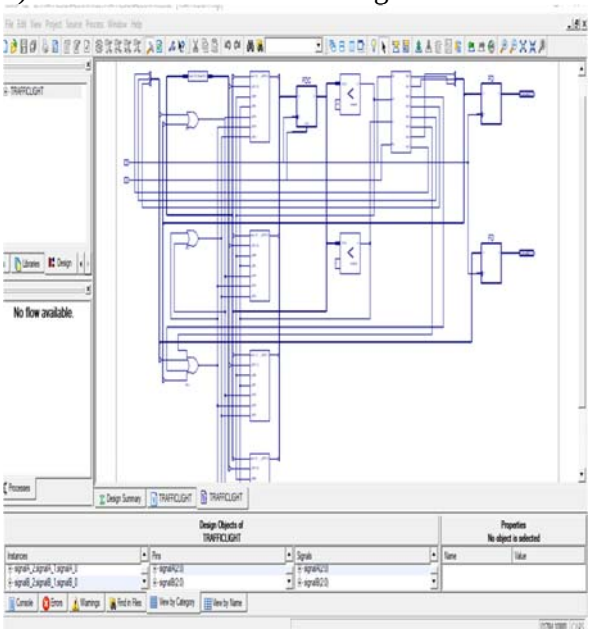
In order to approach this project using Verilog we have to generate clock pulse and reset. For every positive clock pulse different stage will perform its operation. Generation of clock produces the synchronisation between all the signals. working

process of any operation performs more efficiently if clock pulse is used. Then reset is used to rest the signal whenever reset vector is high. As our signalling bit is stored in 6-bit vector. As shown in above mention table. Next step is writing a testbench, which is most important parameter in Verilog. Whatever the task is performed in Verilog is group a set of repetitive or commands that is mentioned in always block while writing a testbench. In the testbench we can try up various possible inputs, outputs and in-outs so that it can be checked whether our tasks give correct or desired output or not. Output can be displayed using $display command in Verilog. in testbench we have to separately generate clock pulse. And we have to create UUT in which configuration of clock, reset, inputs, outputs used must be done. UUT is unit under test which is used for instance naming for a module.at the send of the testbench we have to give $stop command to terminate the process. After the successful execution processes of Verilog code and testbench, behavioural simulation, RTL simulation is also obtained which will give you an exact behaviour of the model.

III. DESCRIPTION OF IMPLEMENTED FUNCTION

Including this RTL Schematic, technology schematic, behavioural waveform is most important factor for any Verilog designing.

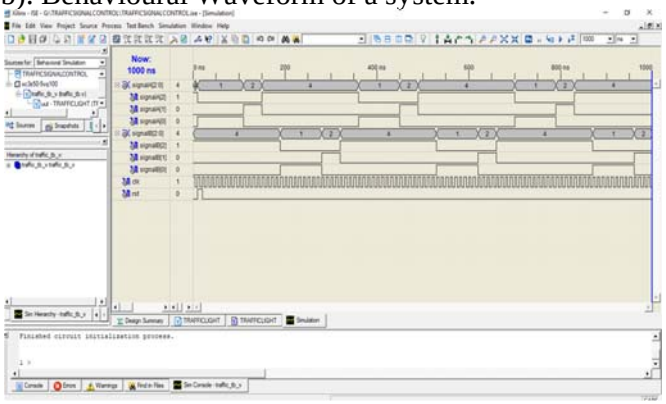
a). RTL Schematic of traffic signal device.



RTL is register-transfer level(RTL) is a design model which gives a description of synchronous digital circuit in terms of the flow digital circuit signals between register which used in hardware combinational logical circuits.

Register-transfer level design is used in hardware descriptive language like VHDL and Verilog to obtain high-level representation from low-level type. It describes how signal transferring is done, types of circuits used.

b). Behavioural Waveform of a system.



Behavioural waveform gives very exact simulation of any hardware description. We can actually observe our output whether it goes right or wrong. From the above given waveform, we can observe that signals which manipulate in perfect coordination as per the code is synthesis.

North-south end	East-west end
Stage 1-Red	stage 1- Green
Stage 2-Red	stage 2- Yellow
Stage 3-Green	stage 3-Red

The above process repeats every cycle which you can observe from above diagram.

c). Technology Schematic

Overview of State diagram of traffic light system

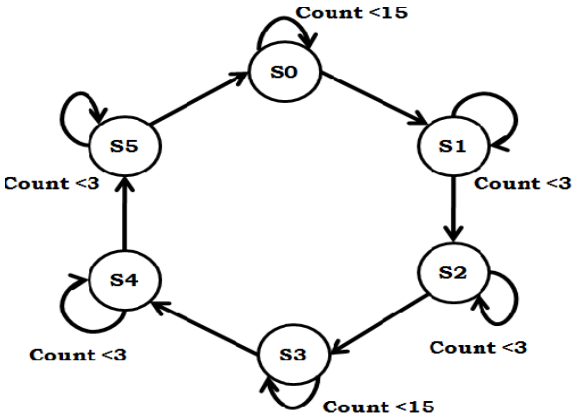


Fig.1. State Diagram

IV. RESULT

In this working model we have observed various stages which describes about every signals. At first stage (north-south end) signals gives some indication. Consider the signal is red that means signal at east-west side gives a green indication and traffic moves to their respective direction. Then after some delay yellow signal is obtain at east-west side and after the red signal arrives at the same time at the north-south end red signal goes off and green signal gets on and traffic moves to their particular direction. In this way process continues in the loop every day.

V. CONCLUSION

Thus, traffic light control system helps to conduct orderly flow of vehicles. There are lot many issues of obstacles, high level accidents which occurs every day. So, traffic signal controller prevents such occurrences. Still many areas or small towns don't have the traffic light control facilities. And thus, many accident problems occur at those areas. Therefore, it is a primary purpose to have such facility in order to control and maintain the area

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