AN EFFICIENT FFT PROCESSOR USING MDC

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Abstract
MIMO-OFDM will represents the multi input and multi output orthogonal frequency division multiplexing as it dominated over 4G and 5G wireless-communications. The meaning of multi input with multi output defines that it able to send multiple signals over multi antennas and the radio channels that again divided into largely spaced sub channels which are divided b y orthogonal-frequency-division multiplexing. That's why the data can be used in communication system without loss in reliability. At present MIMO was used along with a combination of time division multiple access, code division multiple access, but MIMO along OFDM was famous to its high data rate, high message deliver capacity, and high throughput. For such reasons the wires LANs are used in MIMO with OFDM. And also used in some standard networks in mobile communications. If the data size is increases then memory size also increases correspondingly in MDC based upon MIMO-OFDM, but in commutator data flow would be controlled in simplest manner by using multipath delay. This Project presents a multipath delay-commutator (MDC)-based architecture and memory scheduling, for implementing fast Fourier transform (FFT) processors at multiple input multiple output-orthogonal-frequency-division multiplexing (MIMO-OFDM) systems with various lengths. Here it implements a FFT / IFFT processor based MIMO-OFDM system based on the MDC architecture. This design will be used a XILINX ISE12.3i software toll and shows delay values are reduced, we designed RAM, FIFO, input buffer and output sorting buffer, the functionality verification and the synthesis.

Keywords: Fast Fourier Transform (FFT), Memory-Scheduling, Multiple-Input And Multiple-Output (MIMO), Orthogonal-Frequency-Division-Multiplexing (OFDM), Output Sorting, Pipeline Based Multipath-Delay-Commutator (MDC), WiMAX.

I. INTRODUCTION

The multiple frequencies was the popular scheme which is used commonly in orthogonal frequency-division- multiplexing when the required data to encoded. In wideband digital communication this type of method is famous. Whether it may be wired or wireless such as television, broadcasting of audio, internet accessing, wireless networks and is widely used in latest technology like 4G mobile communication. Digital multi carrier modulation technique is used for OFDM, When we require to carry parallel streaming of data, a large spaced orthogonal sub-carrier signals are used in which each sub-carrier undergo convolution modulation like quadrature amplitude modulation or phase shift keying. It uses slowly modulated narrow band signals instead of using one highly modulated wide band signal because of OFDM have capability of channel equalization. We implemented without loss in efficiency we are using OFDM,FFT. Narrow band co channel interfacing becomes very robust using OFDM .it is very less sensitive over time synchronization errors. These type of OFDM signals have broad range of usage in WLAN under the standard of 802.11a,and digital radio systems standards like DAB/ERUKA 147,Terristial Digital TV

systems(DVB-T)and Terrestrial Digital mobile systems(DVB-T). In previous DFT is existed.

In which the fastness drawback has overcome by FFT,OFDM uses reverse FFT and transmitter side and FFT and the receiver side to perform modulation and demodulation efficiently. FFT with of FFDM is used CPU like Intel Pentium at 1.26GHZ frequency and is able to calculate a 8 192 FFT with in 576µs using FFTW, and in CPU called Intel Pentium M AT 1.6 GHZ frequency and able to within 387 µs. a compared to earlier generation CPU,a wide range of FFT-OFDM based CPU named Intel core 2 duo which operates at3 GHz frequency and able to perform the operations at 96. MIMO-OFDM means multi input and multi output orthogonal frequency division multiplexing which is dominated over 4G & 5G wireless communication. The capable of sending multiple signals over multi antennas and orthogonal frequency division multiple communication system without loss in reliability called multiple input and multiple output . In earlier MIMO is used with a combination of time division multiple access ,code division multiple access ,but MIMO with OFDM is much famous for its high data rate ,high message deliver capacity ,high throughput .for these reasons only it is familiar at wires LAN and some standard networks at mobile communications . In MDC based MIMO-OFDM as the data size increases the memory size also increases rapidly . The data flow will be controlled in simplest manner by using multipath delay commutator. For its simplicity and which makes the user data in to a closely spaced narrow sub channels in such to eliminates bigger obstacles to increase reliability, we are using implementing MIMO based OFDM.

II. FFT PROCESSORS

Fast Fourier Transform and Inverse Fast Fourier Transform are the most efficient and fast algorithms to calculate the Discrete Fourier Transform and Inverse Discrete Fourier Transform respectively. Fast Fourier Transform/ Inverse Fast Fourier Transform is mostly used in many communication applications, like Digital Signal Processing and the implementation of this is a growing research. From the last years, OFDM became an important one to implement FFT algorithms . and it is efficient multiple access method for Bandwidth in digital communications is OFDM (Engels, 2002; Nee & Prasad, 2000). Many of nowadays OFDM technique can be used in most important wireless communication systems: Digital Audio Broadcasting (DAB) (World DAB Forum, n.d.), Digital Video Broadcasting (DVB) , Wireless Local Area Network (WLAN) , Wireless Metropolitan Area Network (WMAN) and Multi Band – OFDM Ultra Wide Band (MB–OFDM UWB). Moreover, this method is also utilized in important wired applications like Asymmetric Digital Subscriber Line (ADSL) or Power Line Communication (PLC). Every communication system must have both Transmitter and Receiver. At the Transmitter side, IFFT is used for modulating signal, which depends on the OFDM system and at the Receiver side, FFT is used for demodulating signal.

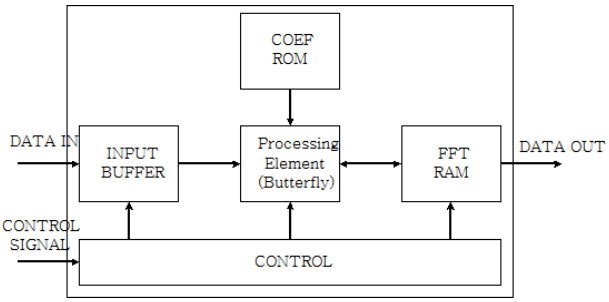

Fig1. Internal Architecture of FFT/IFFT Processors

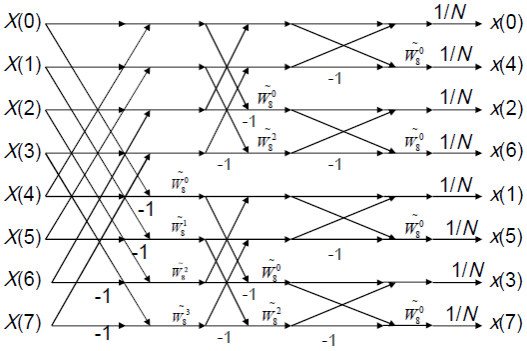

Fig2. Inverse Fourier Transform.

In OFDM transceivers the most important modules are FFT/IFFT. From this we can say that, the most parts of OFDM systems are, IFFT can be used at the transmitter side where as viterbi decoder can be used at the receiver side (Maharatna et al., 2004). The second calculative huge part in the receiver is FFT. Therefore, the

implementation of the FFT and IFFT must be designed to achieve the required throughput with the reduced area and delay. The demanding requirements of modern OFDM transceivers lead, in many cases, to the implementation of special–purpose hardware for the most critical parts of the transceiver. Thus, it is common to find the FFT/IFFT implemented as a Very Large Scale Integrated (VLSI) circuit. The techniques applied to the FFT can be applied to the IFFT as well. Moreover, the IFFT can be easily obtained by manipulating the output of a FFT processor. Therefore, the discussion in this chapter concentrates on the FFT without loss of generality. The inverse discrete Fourier transform can be found using Which can be expressed as Where is called the twiddled factor , the twiddle factor is defined as difference between the inverse discrete Fourier and forward Fourier transform and the division by 1/N is called the twiddled factor.

Wireless technologies have evolved remarkably since Guglielmo Marconi said that the ability of radio can provide good contact with the ships sailing in the English Channel in 1894.Since hundreds and thousands of scientists and engineers through the world, new theories and applications of wireless technologies have been developed by hundreds. Wireless communications can be regarded as the most important development that has an extremely wide range of applications from TV remote control and cordless phones to cellular phones and satellite-based TV systems. It changed people's life style in every aspect. Especially during the last decade, the industry of mobile radio communication is growing exponentially with increasing rate, fueled by the digital and RF (radio frequency) circuits design, fabrication and integration techniques and more computing power in chips. This trend will continue with an even greater pace in the near future.

The advances and developments in the technique have partially helped to realize our dreams on fast and reliable communicating \any time anywhere". But we are expecting to have more experience in this wireless world such as wireless Internet surfing and interactive multimedia messaging so on. One natural question is: how can we put high-rate data streams over radio links to satisfy our needs? New wireless broadband access techniques are anticipated to answer this question .For example, the coming 3G (third generation) cellular technology can provide us with up to 2Mbps(bits per second) data service. But that still does not meet the data rate required by multimedia media communications like HDTV (high-definition television) and video conference. Clearly all the performance improvement and capacity increase are based on accurate channel state information.

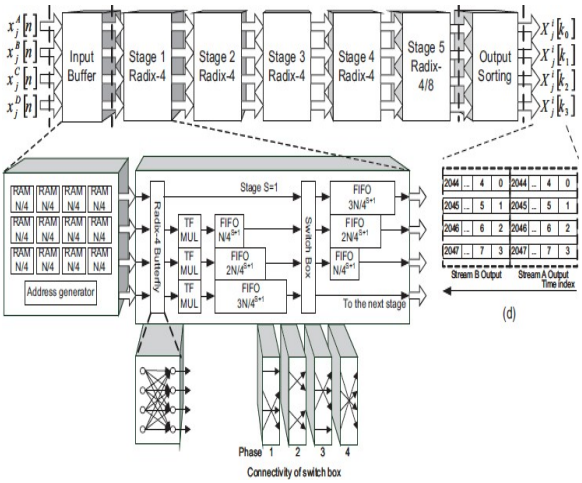

Fig3. Proposed MIMO FFT/IFFT processor.

In wireless communication systems combination of MIMO and OFDM system provides efficient data rate and reliability. IEEE 802.16 WIMAX (Worldwide Interoperability for Microwave Access) is a wireless communications standard, which can provide a data rates from 30 to 40 megabit/sec. 3GPP (3rd Generation Partnership Project) is the recent evaluation in IEEE 802.16 WiMAX. The 3rd Generation Partnership Project initiative evolved from a strategic one, which is between Nortel Networks and AT&T Wireless. AT&T Wireless was operated an IS-136 (TDMA) wireless network in the United States in 1998. To reduce the run time memory by using the memory scheduling technique the RAM is changed to DRAM where 12 memory blocks are sufficient instead of 16.Nortel Networks Wireless, which is an R&D center in Richardson, Texas, the wireless division of Bell Northern Research developed a vision for "an all Internet Protocol (IP)" wireless network that is having the internal name "Cell Web" .In the proposed design the ram is replaced by dynamic

ram. Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.The multiple output Boolean function F(x1; x2; :::; xn) of n Boolean variables is called reversible if the number of outputs is equal to the number of inputs and any output pattern has a unique pre-image. The reversible HNG gate can work singly as a reversible full adder. If the input vector IV = (A, B, Cin, 0), then the output vector becomes OV = (P=A, Q=Cin, R=Sum, S=Cout). If we consider d = 0,then " R"is taken as SUM and "S" is considered as CARRY.

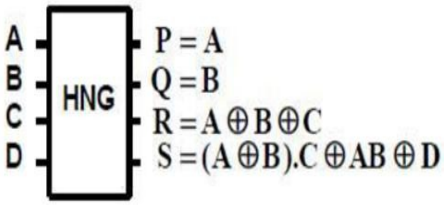

Fig4. Block diagram of HNG gate.

Addition, subtraction, multiplication, division are basic arithmetical operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers.

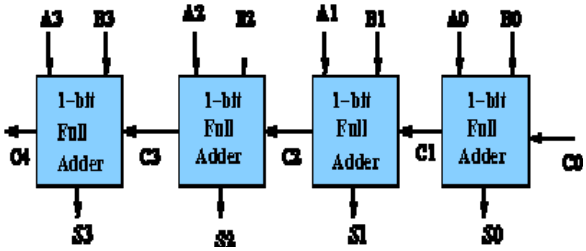

Fig5. Ripple carry adder.

Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder, since each carry bit "ripples" to the next full adder. The half adder was replaced by the first full adder .The block diagram of 4-bit Ripple Carry Adder is given below.

III. FFT PROCESSOR METHODS

An algorithm proposed by Cooley and Tukey to compute Discrete Fourier transform (DFT) from efficient Fast fourier transform which converts time to frequency and reduces the time complexity to O(N log 2N), where N denotes the size of FFT. When considering the alternate implementations, the FFT/IFFT algorithm should be chosen to consider the execution speed, hardware complexity, and flexibility and precision. Nevertheless, for real time systems the execution speed is the main concern. Several architectures have been proposed over the last 3 decades like: single memory architecture, dual-memory architecture, cached memory architecture, array architecture, and pipelined architecture for the purpose of hardware implementation, various FFT processors have been used mainly two types of architectures which are Memory based architecture and Pipeline based architecture. Memory based architecture cannot be parallelized where as the pipeline architecture can overcome the disadvantages of the former architecture. Pipelined architectures characterized by real time, non-stopping processing and present smaller latency with low power consumption which makes them suitable for most application. Generally, the pipeline FFT processors are classified in two design- architectures. They are Single-path delay feedback (SDF) pipeline architecture and Multiple-path delay Commutator (MDC) pipeline architecture.

To reduces amount of multipliers to use single path delay feedback(SDF) but it complicates the control mechanism and uses more memory resources whereas Multipath Delay Commutator saves more area,[5] and thus MDC is adopted as the hardware architecture. Multipath Delay Commutator (MDC) makes the feedback paths in to feed forward streams using switch boxes along with memory. In this paper to implement fast Fourier transform for multiple input multiple output orthogonal frequency division with variable length multipath delay commutator and memory is used. The observation made on the listed architectures reveals that the delay feedback architecture is more efficient than the

corresponding delay commutator in terms of memory utilization. For computation of FFT we need to use twiddle factor to multiply with input signals to obtain output, and for this a huge size of ROM is required to store twiddle factors which in turn increases the cost. Thus for further improvement, eliminates ROM s are hide twiddle factor when there is ROM-less FFT/IFFT processor . The purpose and they perform shift-and-add operations, the complex multiplexers are used thus the processor uses a digital multiplier with 2 inputs and does not require any storage element like ROM, to store twiddle factor. Thus the target architecture also contains a reconfigurable complex constant multiplier to store twiddle factor in case of using ROM"s.

IV. RESULTS

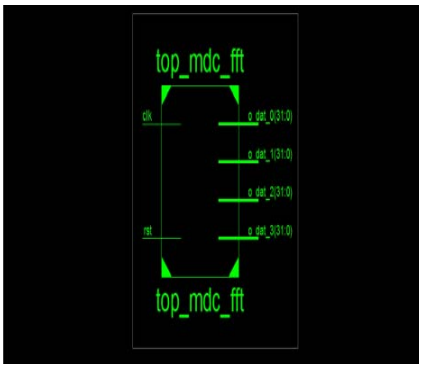

Fig6. RTL Schematic.

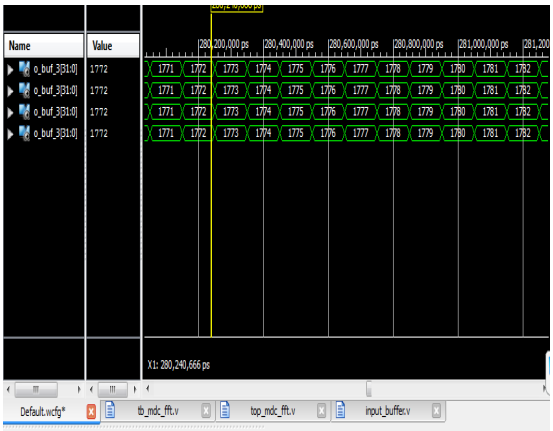

Fig7. Simulation Results.

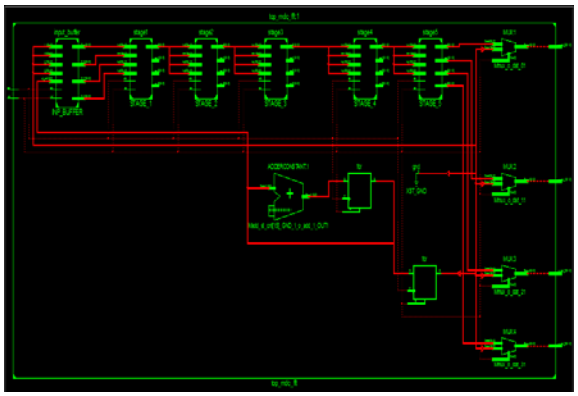

Fig8. RTL Internal Schematic.

Design Summary:

DEVICE

USED:XC6VSX475TL-1LFF1156

PROPOSED : NO OF LUT'S = 7850.

EXISTING : NO OF LUT'S = 7906.

Table1. Proposed Results

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1798	595200	0%
Number of Slice LUTs	7850	297600	2%
Number of fully used LUT-FF pairs	1308	8340	15%
Number of bonded IOBs	130	600	21%
Number of Block RAM/FIFO	6	1064	0%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	228	2016	11%

Table2. Existing Results.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1930	595200	0%
Number of Slice LUTs	7906	297600	2%
Number of fully used LUT-FF pairs	1398	8438	16%
Number of bonded IOBs	130	600	21%
Number of Block RAM/FIFO	5	1064	0%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	228	2016	11%

V. CONCLUSIONS

In this paper, we determined a radix-*r* based MDC MIMO FFT/IFFT processor for processing *Ns* streams of concurrent inputs, where $r = Ns$ for reaching a 100% utilization rate. The intend approach is comfortable for MIMO-OFDM baseband processor that is WiMAX or LTE applications. where $Ns = 4$ and *N* can be configured as 2048, 512, 256, and 128. Additionally, we proposed additional

memory scheduling to fully utilize memory. The memory requirement usually dominates the chip area in an FFT/IFFT processor when area of chip decreases. It is worth emphasizing that the proposed design is based on an MDC architecture, due to its low utilization rate in memory and computational elements such as adders and multipliers MDC architecture is not preferred. Whatever, in MIMO-OFDM systems MDC architecture is proved suitable for FFT/IFFT processors for using proposed memory scheduling because the butterflies and multipliers are able to reach a 100% utilization rate, meanwhile, the characteristics MDC is maintained in the proposed design provides simple control. The reduce in memory usage also leads to enhancing power saving, which is important for mobile devices. For applications applying for large number *Ns* of data streams those are gigabit passive optical network, *Ns* can be as high as 64. In this case, the proposed radix-*Ns* MDC scheme and memory scheduling may also be applied to reach a 100% utilization rate with simple control mechanism. so, we conclude that the proposed designs gives a good balance among circuit complexity, energy saving, and area of chip, for the MIMO-OFDM systems.

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