



COEFFICIENT ORDERING BASED LOW POWER FFT FOR WIRELESS LAN APPLICATIONS

A.Jeyapaul Murugan

Assistant Professor, Department of ECE,
Dr.Sivanthi Aditanar College of Engineering

ABSTRACT

In a world of increasing mobility, there is a growing need for people to communicate with each other without latency and at less power consumption. Power dissipation can be reduced by reducing the arithmetic complexity. In orthogonal frequency division multiplexing (OFDM), Inverse Fast Fourier Transform (IFFT) converts the modulated information from frequency domain to time domain for transmission of radio signals, while FFT gathers samples from the time domain, transforming them to the frequency domain.

In this project, two different VLSI architectures of FFT using radix 2 DIF and radix 2 DIT for 8-point is designed and compared. The result shows that the radix 2 DIT FFT dissipates less power than the radix-2 DIF FFT

I. INTRODUCTION

VLSI (very large-scale integration) is the current level of computer microchip miniaturization and refers to microchips containing in the hundreds of thousands of transistors. Power consumption, operation speed and occupied area are still the main requirement of VLSI. Speed is an important consideration in VLSI.

Modern applications are demanding high speed computations. Technology is coming close to the theoretical limits on how fast computation can be done on a single chip. Multiple processors operating in parallel performing different functions of a process and comparing them at the end is the solution to this. Fourier transform is the

basis of many signal processing and communication application. It is the tool for analysis of the signal in its frequency domain. Fourier Transform has many application in fact any field of physical science that uses varying signals, such as engineering, physics, applied mathematics and chemistry, will make use of Fourier series and Fourier transforms. Most of these fields nowadays make use of digital and discrete data. Thus the determination of Fourier transform of discrete signal is of prime importance and such a transformer is called Discrete Fourier transform (DFT). Fast Fourier Transform (FFT) is an efficient algorithm to evaluate DFT. FFT computation involves addition and multiplication of operation. As multipliers are slow performing hardware units their performance that affects the performance of the FFT hardware. FFT are extensively used in communication, data compressions, filtering signals, signal spectral analysis, image processing, etc. In communication, as a result of advancing VLSI technology, OFDM has received a great deal of attention and been adopted in many new generation wideband data communication systems such as IEEE 802.11a, HiPerLAN/2 digital audio video broadcasting and asymmetric digital subscriber line interface(ADSL). FFT and IFFT is the main arithmetic kernel in the OFDM system. They are important and complex blocks in OFDM system which consumes lots of resources. Thus the FFT with less power dissipation must be used for efficient functioning of OFDM system.

A. ADDERS AND MULTIPLIERS IN VLSI

Adders and multipliers are the main building blocks of the computing architectures like IIR filter, FIR filters, etc. Multiplication is

one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction. In fact, 8.72% of all the instruction in typical processing units is multiplication.

Multiplication is an important fundamental function in arithmetic logic operation. Computational performance of a DSP system is limited by its multiplication performance since, multiplication dominates the execution time of most of the DSP algorithms therefore high-speed multiplier is much desired. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

B.DIRECT FFT COMPUTATION

The time domain information is not available in continuous form, it is sampled that is the information is presented as a stream of discrete samples taken at regular intervals in time and hence DFT is extremely important in the area of frequency (spectrum) analysis because it takes a discrete signal in the time domain and transforms that signal into discrete frequency domain representation.

To calculate all frequency outputs of an N-point DFT requires $(N-1)2$ complex multiplications and $N(N-1)$ complex additions.

C.FAST FOURIER TRANSFORM

A Fast Fourier Transform (FFT) algorithm computes the discrete Fourier transform (DFT) of a sequence, or its inverse. Fourier analysis converts a signal from its original domain (often time or space) to a representation in the frequency domain and vice versa (S. He.1996). The FFT utilizes clever algorithms that do the same things as the DFT, but in much less time. FFTs are of great importance to a wide variety of applications, from digital signal processing to solving partial differential equations to algorithms for quickly multiplying large integers. Evaluating these sums directly would take $O(N^2)$ arithmetic operations. An FFT is an algorithm to compute the same result in only $O(N \log N)$ operations. In general, such algorithms depend upon the factorization of n but there are FFTs with complexity of $O(N \log N)$ for all N even for prime N . Many FFT algorithms only depend on the fact that 1 is a primitive root of unity. Since the inverse DFT is

the same as the DFT, but with the opposite sign in the exponent and a $1/N$ factor, any FFT algorithm can easily be adapted for it as well.

FFTs perform exactly the same task as the DFT, but are able to dramatically reduce the amount of complex arithmetic calculation required to do so by taking advantage of some of the symmetries, repetitions and redundancies within the transform. There are many different forms of FFT algorithms, all with their advantages and disadvantages.

D.BASIC CONCEPTS OF FFT ALGORITHMS-DIVIDE AND CONQUER

The algorithm is based on the fundamental principle of decomposing the computation of the Discrete Fourier Transform (DFT) of a sequence of length N into successively smaller DFTs. The manner in which this principle is implemented leads to a variety of different algorithms, all with comparable improvements in computational speed.

The three major steps of the divide-and-conquer paradigm are

1. Divide the sequence of data into two or more subsequence of smaller size.
2. Solve each subsequence recursively by the same algorithm. Apply the boundary condition to terminate the recursion when the sizes of the subsequences are small enough.
3. Obtain the solution for the original problem by combining the solutions to the subsequence

E.BASIC OFDM SYSTEM

OFDM transmission is emerging as a predominant multicarrier modulation technique because of its capability of ensuring high-level robustness against interference. OFDM modulation technique is extensively used in numerous high speed mobile and wireless communication systems as Wi-Fi system, WiMax system, asymmetric digital subscriber line mobile WiMax system and wireless local area network. It provides high bandwidth efficiency because the carriers are orthogonal to each other and multiple carriers share the data among themselves. (Akash Mecwan et al. 2013) Fast Fourier Transform is one of the key components of the OFDM system nowadays. Several communication systems require high point FFT and the highest symbol rate. This requirement establishes challenges for low

power high speed FFT designs with large number of points FFT algorithm eliminates the calculation which is needed

Orthogonal frequency-division multiplexing (OFDM), is identical to Discrete multi tone modulation (DMT), is a frequency-division multiplexing (FDM) scheme utilized as a digital multi-carrier modulation method. Many of closely-spaced orthogonal sub-carriers are used to carry data. The data are divided into several parallel data streams or channels, one for each sub-carrier. Each sub-carrier is modulated with a conventional modulation scheme (such as quadrature amplitude modulation or phase shift keying) at a low symbol rate, keeping the total data rates similar to conventional single-carrier modulation schemes in the same bandwidth.

The primary advantage of OFDM over single-carrier schemes is its ability to cope with severe channel conditions, for example, attenuation of high frequencies in a long copper wire, narrowband interference and frequency-selective fading due to multipath, without complex equalization filters.

The OFDM signal is in time domain, IFFT is the appropriate choice to use in the transmitter, for converting frequency domain samples to time domain samples. In its classical definition, an IFFT takes a frequency-domain signal and converts it back to time domain. In an OFDM signal, we take a data signal, and map it to very many harmonics (frequencies), so we have sort of taken a time domain-signal and turned it into a frequency domain signal. This task is performed by the IFFT for an OFDM signal. This conversion process eliminates the individual sinusoidal multipliers required in the transmitter/receiver side. FFT is used to demodulate the data.

TRANSMITTER OF OFDM:

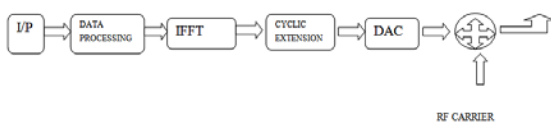


Figure 1 Transmitter of OFDM

RECEIVER OF OFDM:

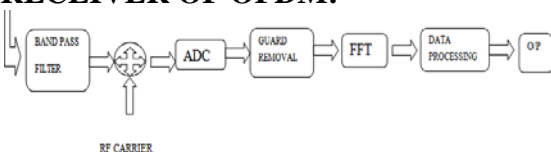


Figure 2 Receiver of OFDM

II. PROPOSED WORK

A. INTRODUCTION

Fast Fourier Transform algorithms are mathematical simplifications of the Discrete Fourier Transform (DFT). They exploit symmetries and periodicity in the transform in order to reduce the number of mathematical computations. There have since been many variations of this algorithm aimed at reducing the complexity of DFT calculations. These families of fast algorithms for computing the DFT are commonly called as FFT algorithms. FFT computations can be classified as decimation in time (DIT) FFT and decimation in frequency (DIF) FFT.

B. DECIMATION IN TIME FFT

DIT FFT algorithm, first twiddle factor is multiplied and later it is summed up. DIT FFT algorithm the input sequence $x(n)$ appears in bit reversed order while the output $X(k)$ appears in the bit normal order. The basic butterfly diagram for DIT FFT is shown in figure

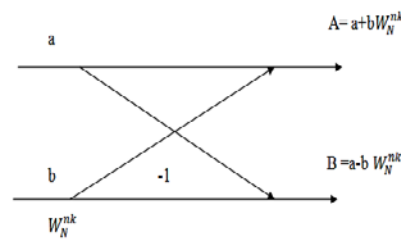


Figure 3 Basic butterfly of DIT FFT

C. DECIMATION IN FREQUENCY FFT

DIF FFT algorithm first the input is summed up and then the twiddle factor is multiplied. DIF FFT algorithm $x(n)$ appears in normal order while the output $X(k)$ appears in the bit reversed order. Bit reversed order corresponding to the normal order is shown in table 3.1. The basic butterfly diagram for DIF FFT is shown in figure 3.2

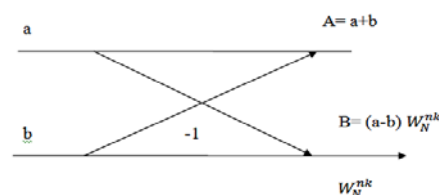


Figure 4 Basic butterfly of DIF FFT

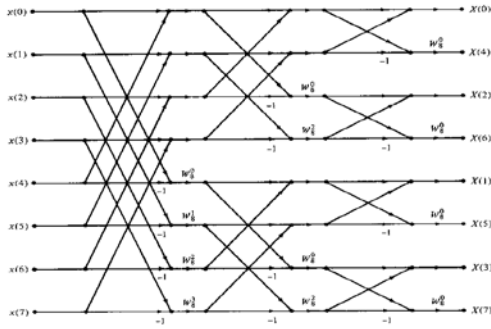
D. RADIX-2 DIF FFT

For radix-2, the DIF decomposition separates the output sequence $X[k]$ into even and odd samples.

The N -point DFT is transformed into two $N/2$ point DFTs. Applying the procedure iteratively leads to decomposition into 2-point DFTs. Fig. 2.1 shows the flow graph of 8-point radix-2 DIF FFT

E. 8-POINT RADIX 2 DIF FFT

The 8-point DIF FFT has 8 input signals in normal order and 8 output signals in bit reversed order.



F. TWIDDLE FACTOR

A twiddle factor, in fast Fourier transform (FFT) algorithms, is any of the trigonometric constant coefficients that are multiplied by the data in the course of the algorithm.

More specifically, "twiddle factors" originally referred to the root-of-unit complex multiplicative constants in the butterfly operations of the Cooley–Tukey FFT algorithm, used to recursively combine smaller discrete Fourier transforms. This remains the term's most common meaning, but it may also be used for any data-independent multiplicative constant in an FFT. The twiddle factor is represented in IEEE 754 format representation. The real and imaginary parts of twiddle factor values in IEEE 754 format is given as

- $w_0r=8'b1$; $w_0i=8'b0$;
- $w_1r=8'b10110101$; $w_1i=8'b01001011$;
- $w_2r=8'b0$; $w_2i=8'b11111111$;
- $w_3r=8'b01001011$; $w_3i=8'b01001011$.

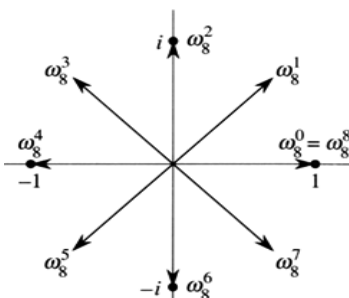


Figure 5 Twiddle Factor

G. FLOATING POINT ARITHMETIC

In computing, Floating Point Arithmetic is arithmetic using formulaic representation of real numbers as an approximation so as to support a trade-off between range and precision. A number is, in general, represented approximately to a fixed number of significant digits (the significant) and scaled using an exponent in some fixed base; the base for the scaling is normally two, ten or sixteen. A number that can be represented exactly is of the following form:
Significant x base^{exponent}.

H. FLOATING POINT REPRESENTATION

The IEEE-754 Single precision and Double precision format is used to represent the floating point numbers. The floating point number can support wide range of values. It is represented using three fields: sign, exponent and mantissa.

III. SIMULATION RESULTS

A. SIMULATION RESULTS OF DIF FFT

The simulated results of 8-point radix 2 DIF FFT in ModelSim is as follows

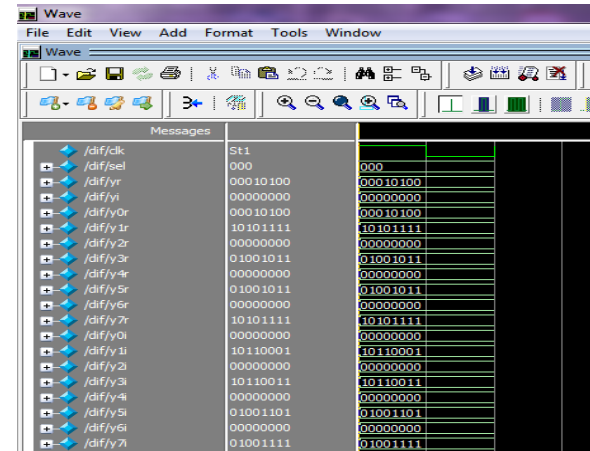


Figure 6 Simulation output waveform of DIF FFT

The power dissipation of 8-point radix-2 DIF FFT obtained from Quartus 9.1 shows that the thermal static power dissipation is 2.71 Mw

Block Type	Total Thermal Power By Block Type	Block Thermal Dynamic Power	Block Thermal Static Power (T)	Routing Thermal Dynamic Power	Block Average Toggle Rate (millions of transitions / sec)
1 I/O	2.71 mW	0.00 mW	2.71 mW	0.00 mW	0.000
2 Combinational cell	0.00 mW	0.00 mW	-	0.00 mW	0.000
3 Register cell	0.00 mW	0.00 mW	-	0.00 mW	0.000
4 Clock control block	0.00 mW	0.00 mW	-	0.00 mW	0.000

Figure 7 Power Dissipation report of DIF FFT

4.5 SIMULATION RESULTS OF DIT FFT

The simulation results of DIT FFT are as follows

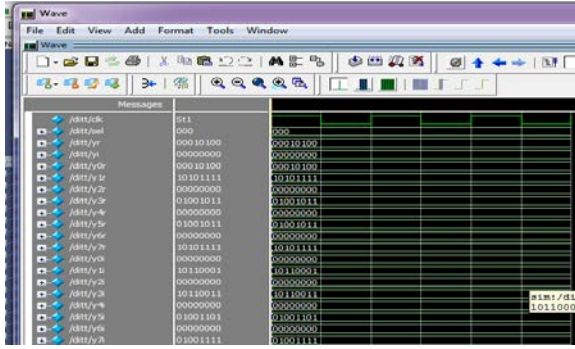


Figure 8 Simulation output waveform of DIF FFT

The input for the DIF FFT are given in binary values for the decimal number {1,2,3,4,4,3,2,1}, and the output are obtained as binary for {20, -5.828-j2.414, 0, 0.172-j0.414,0,-0.172+j0.414,0,-5.828+j2.414}.

The power dissipation of 8-point radix-2 DIT FFT obtained from Quartus 9.1 shows that the thermal static power dissipation is 2.62 mW.

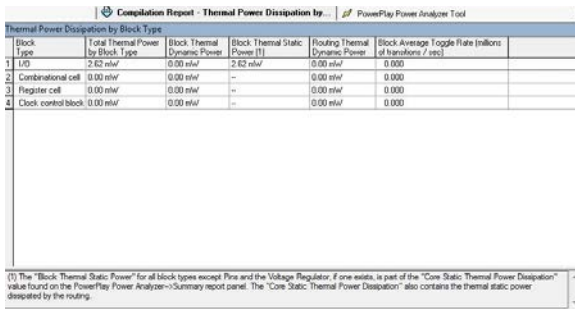


Figure 9 Power Dissipation report of DIT FFT

CONCLUSION

This project deals with the implementation of 8-point radix 2 DIF FFT and 8-point radix 2 DIT FFT. The simulation outputs, power report and delay report of the both architecture of 8-point radix 2 DIT FFT and 8-point radix 2 DIF FFT are analyzed. The power dissipation, gate delay and number of slice LUTs used the DIT is found to have lesser value than DIF. The power dissipation of 8-point radix 2 DIT FFT is 2.62mW and DIF FFT is 2.71mw. Thus it is concluded that that 8-point radix 2 DIT FFT is efficient.

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